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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128bfc100-10n

...and More Features

- System-level features
 - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
 - Programmable power-saving mode for 50% or greater power reduction in each macrocell
 - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
 - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
 - Bus-hold option on I/O pins
 - PCI compatible
 - Bus-friendly architecture including programmable slew-rate control
 - Open-drain output option
 - Programmable security bit for protection of proprietary designs
 - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
 - Supports hot-socketing operation
 - Programmable ground pins
- Advanced architecture features
 - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
 - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
 - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
 - Two global clock signals with optional inversion
 - Programmable power-up states for macrocell registers
 - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
 - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
 - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
 - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf)-capable in-circuit tester

General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See [Table 2](#).

Table 2. MAX 7000B Speed Grades <i>Note (1)</i>					
Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

Notes:

- (1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See [Table 3](#).

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000B architecture includes the following elements:

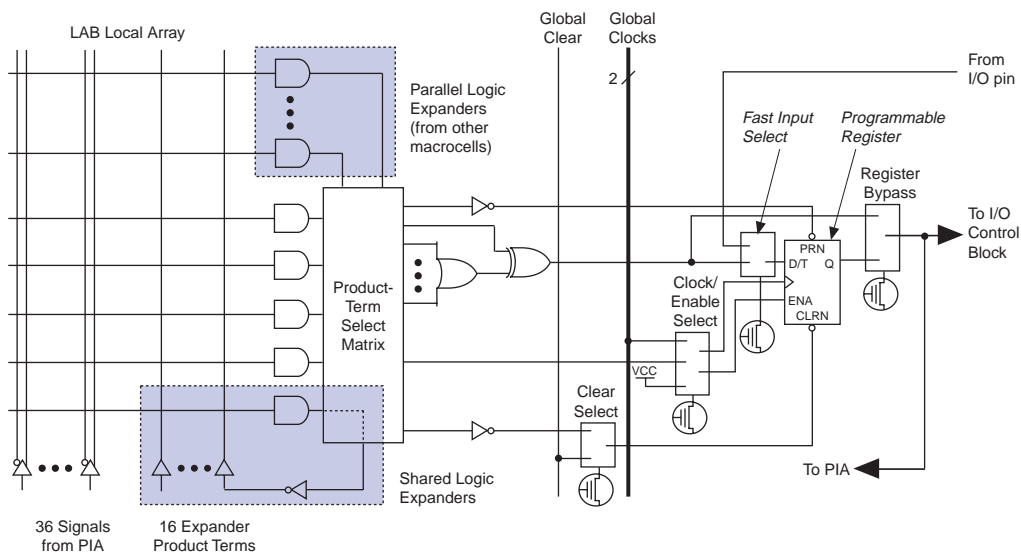
- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000B devices.

Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

Figure 2. MAX 7000B Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

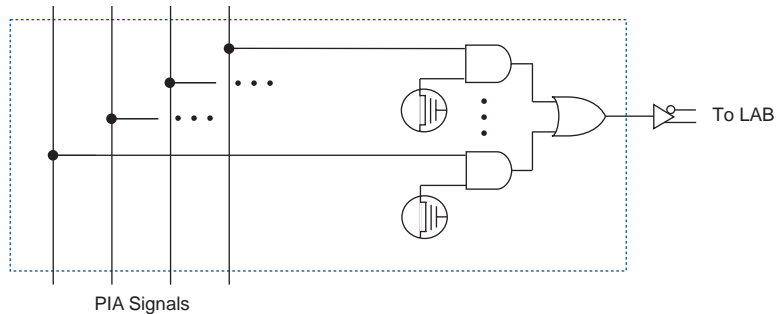
- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 5. MAX 7000B PIA Routing

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

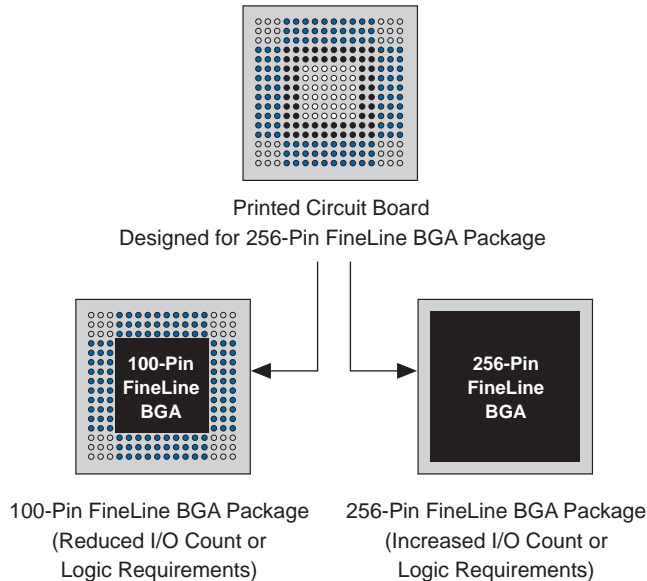
The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see [Figure 7](#)).

Figure 7. SameFrame Pin-Out Example



Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000B device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Table 15. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(10)	2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	(3)	−0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	°C
		For industrial use (11)	−40	85	°C
T_J	Junction temperature	For commercial use	0	90	°C
		For industrial use (11)	−40	105	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 16. MAX 7000B Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage for 3.3-V TTL/CMOS		2.0	3.9	V
	High-level input voltage for 2.5-V TTL/CMOS		1.7	3.9	V
	High-level input voltage for 1.8-V TTL/CMOS		$0.65 \times V_{CCIO}$	3.9	V
V_{IL}	Low-level input voltage for 3.3-V TTL/CMOS and PCI compliance		-0.5	0.8	V
	Low-level input voltage for 2.5-V TTL/CMOS		-0.5	0.7	V
	Low-level input voltage for 1.8-V TTL/CMOS		-0.5	$0.35 \times V_{CCIO}$	
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (5)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (5)	$V_{CCIO} - 0.2$		V
	2.5-V high-level output voltage	$I_{OH} = -100 \text{ } \mu\text{A DC}$, $V_{CCIO} = 2.30 \text{ V}$ (5)	2.1		V
		$I_{OH} = -1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (5)	2.0		V
		$I_{OH} = -2 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (5)	1.7		V
	1.8-V high-level output voltage	$I_{OH} = -2 \text{ mA DC}$, $V_{CCIO} = 1.65 \text{ V}$ (5)	1.2		V
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 8 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (6)		0.4	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (6)		0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100 \text{ } \mu\text{A DC}$, $V_{CCIO} = 2.30 \text{ V}$ (6)		0.2	V
		$I_{OL} = 1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (6)		0.4	V
		$I_{OL} = 2 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (6)		0.7	V
	1.8-V low-level output voltage	$I_{OL} = 2 \text{ mA DC}$, $V_{CCIO} = 1.7 \text{ V}$ (6)		0.4	V
I_I	Input leakage current	$V_I = -0.5 \text{ to } 3.9 \text{ V}$ (7)	-10	10	μA
I_{OZ}	Tri-state output off-state current	$V_I = -0.5 \text{ to } 3.9 \text{ V}$ (7)	-10	10	μA
R_{ISP}	Value of I/O pin pull-up resistor during in-system programming or during power up	$V_{CCIO} = 1.7 \text{ to } 3.6 \text{ V}$ (8)	20	74	$k\Omega$

Table 17. MAX 7000B Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF

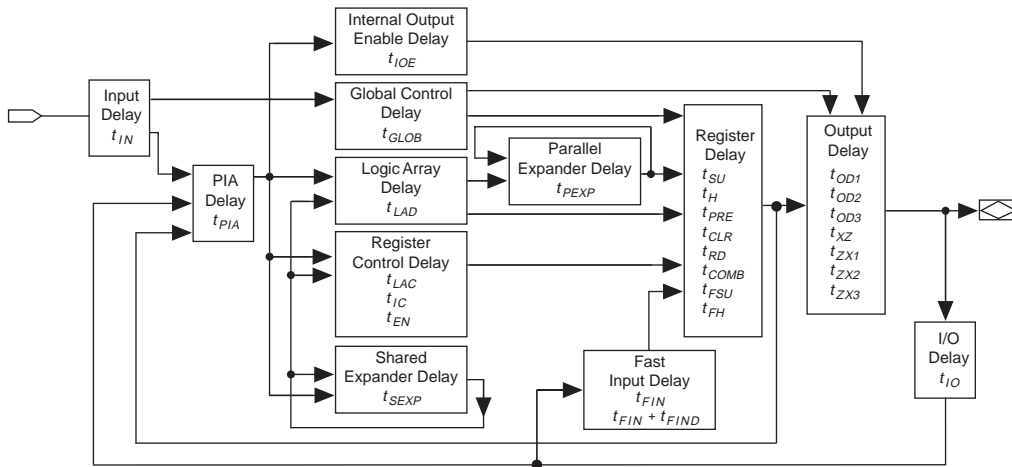
Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.5 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns .
- (3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (4) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#).
- (5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
- (7) This value is specified for normal device operation. During power-up, the maximum leakage current is $\pm 300\text{ }\mu\text{A}$.
- (8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V_{CCIO} .
- (9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (OE1 and GCLRN) have a maximum capacitance of 15 pF .
- (10) The POR time for all 7000B devices does not exceed $100\text{ }\mu\text{s}$. The sufficient V_{CCINT} voltage level for POR is 2.375 V . The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
- (11) These devices support in-system programming for -40° to 100° C . For in-system programming support between -40° and 0° C , contact Altera Applications.

Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

Tables 18 through 32 show MAX 7000B device timing parameters.

Table 18. EPM7032B External Timing Parameters

Notes (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{SU}	Global clock setup time	(2)	2.1		3.0		4.5		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t _{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t _{CH}	Global clock high time		1.5		2.0		3.0		ns
t _{CL}	Global clock low time		1.5		2.0		3.0		ns
t _{ASU}	Array clock setup time	(2)	0.9		1.3		1.9		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.6		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t _{ACH}	Array clock high time		1.5		2.0		3.0		ns
t _{ACL}	Array clock low time		1.5		2.0		3.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t _{CNT}	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t _{ACNT}	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

Table 19. EPM7032B Internal Timing Parameters

Notes (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_H	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	(2)		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	(4)		1.5		2.1		3.2	ns

Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.7		1.1	ns
	Input to global clock and clear		0.5		0.7		1.1	ns
	Input to fast input register		0.4		0.6		0.9	ns
	All outputs		1.2		1.7		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.6		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

Table 28. EPM7256B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.6		0.8	ns
t_{FIN}	Fast input delay			1.5		2.5		3.1	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.3		3.0	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.8	ns
t_{LAD}	Logic array delay			1.7		2.5		3.3	ns
t_{LAC}	Logic control array delay			1.5		2.2		2.9	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.4		1.9	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.4		6.9	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.2		3.3		4.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		7.2		8.3		9.5	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		2.2		3.3		4.5	ns
t_{SU}	Register setup time		1.2		1.8		2.5		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.7		1.0		1.3	ns
t_{COMB}	Combinatorial delay			0.3		0.4		0.5	ns
t_{IC}	Array clock delay			1.5		2.3		3.0	ns
t_{EN}	Register enable time			1.5		2.2		2.9	ns
t_{GLOB}	Global control delay			1.3		2.1		2.7	ns
t_{PRE}	Register preset time			1.0		1.6		2.1	ns
t_{CLR}	Register clear time			1.0		1.6		2.1	ns
t_{PIA}	PIA delay	(2)		1.7		2.6		3.3	ns
t_{LPA}	Low-power adder	(4)		2.0		3.0		4.0	ns

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \log_{LC})$$

The parameters in this equation are:

- MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (.rpt)
 MC_{DEV} = Number of macrocells in the device
 MC_{USED} = Total number of macrocells in the design, as reported in the Report File
 f_{MAX} = Highest clock frequency to the device
 \log_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)
 A, B, C = Constants, shown in [Table 33](#)

Table 33. MAX 7000B I_{CC} Equation Constants			
Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 27. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.

