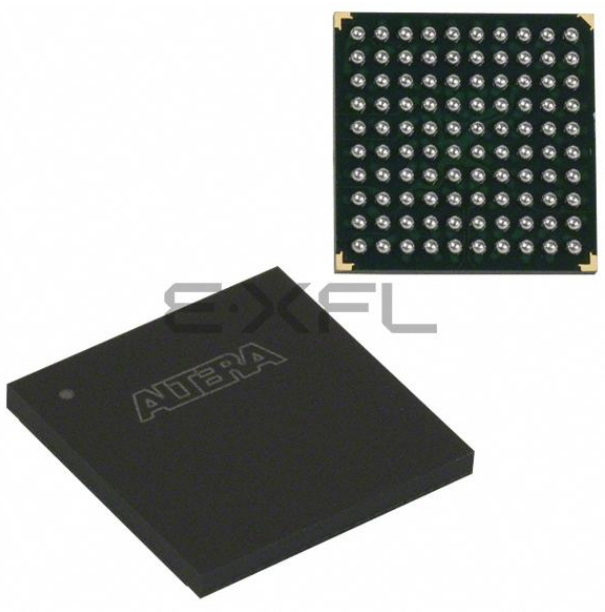


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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 4 ns |
| Voltage Supply - Internal | 2.375V ~ 2.625V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 128 |
| Number of Gates | 2500 |
| Number of I/O | 84 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LBGA |
| Supplier Device Package | 100-FBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7128bfc100-4 |

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

## General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See Table 2.

*Table 2. MAX 7000B Speed Grades* *Note (1)*

| Device | Speed Grade | | | | |
|---|---|---|---|---|---|
| | -3 | -4 | -5 | -7 | -10 |
| EPM7032B | ✓ | | ✓ | ✓ | |
| EPM7064B | ✓ | | ✓ | ✓ | |
| EPM7128B | | ✓ | | ✓ | ✓ |
| EPM7256B | | | ✓ | ✓ | ✓ |
| EPM7512B | | | ✓ | ✓ | ✓ |

*Notes:*
(1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See Table 3.

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

## Expander Product Terms

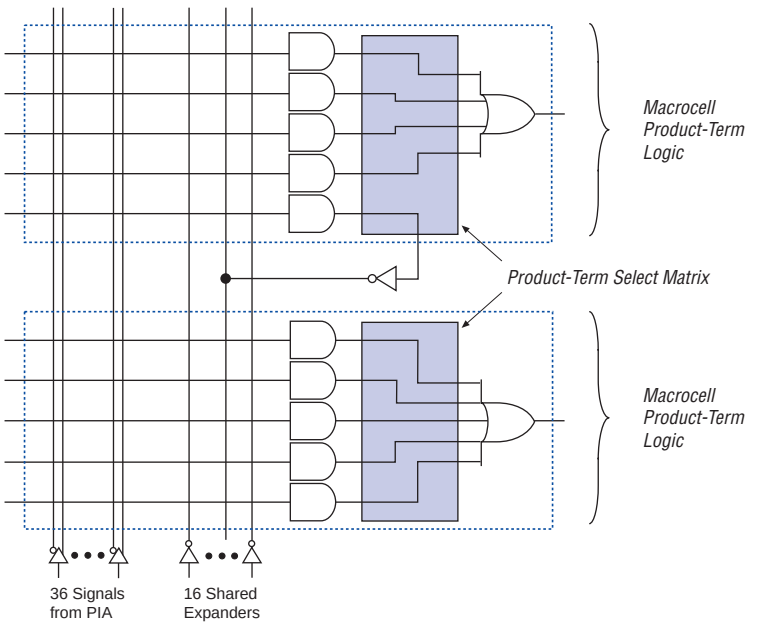
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### *Shareable Expanders*

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{SEXP}$) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

***Figure 3. MAX 7000B Shareable Expanders***

*Shareable expanders can be shared by any or all macrocells in an LAB.*



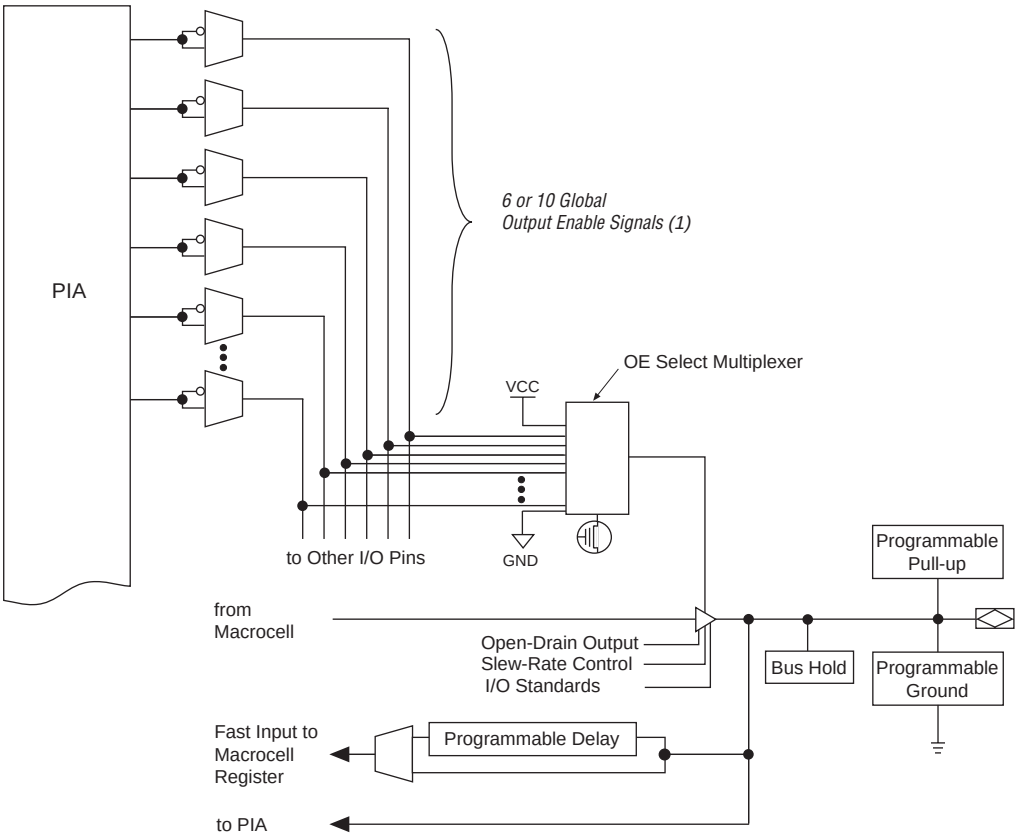
### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

*Figure 6. I/O Control Block of MAX 7000B Devices*




*Note:*

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to $V_{CC}$, the output is enabled.

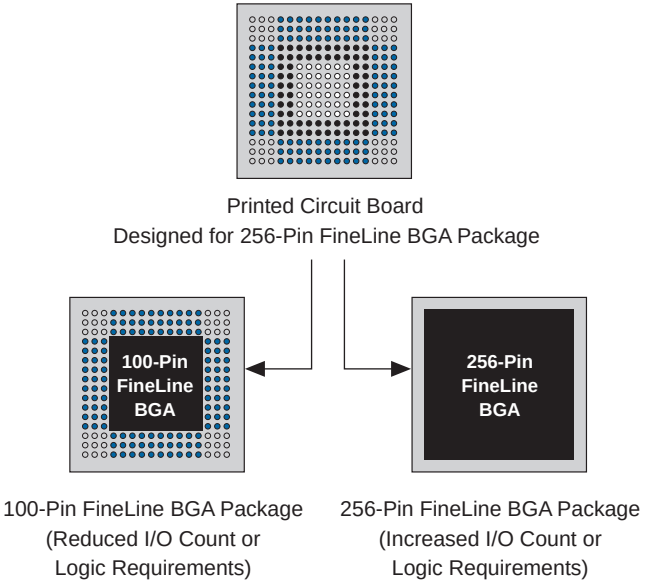
The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see Figure 7).

*Figure 7. SameFrame Pin-Out Example*



## In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k¾.

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

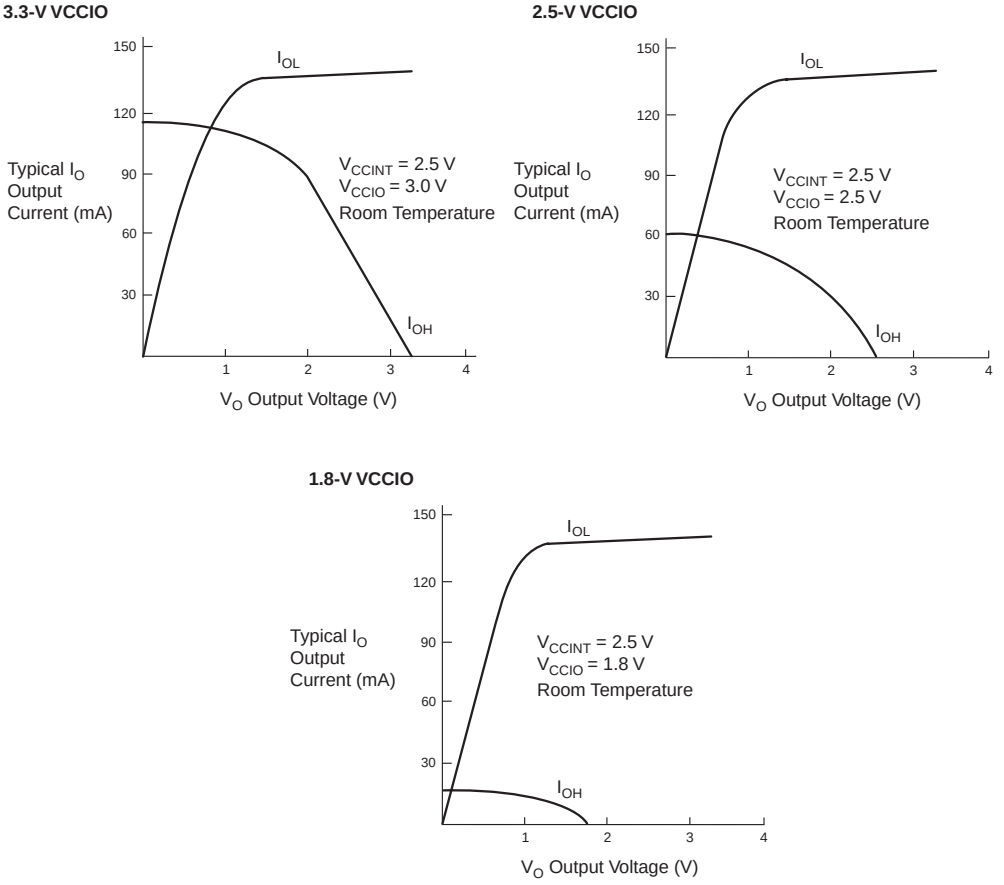
The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using STAPL for ISP & ICR via an Embedded Processor)*.

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Figure 12 shows the typical output drive characteristics of MAX 7000B devices.

***Figure 12. Output Drive Characteristics of MAX 7000B Devices***



Tables 18 through 32 show MAX 7000B device timing parameters.

**Table 18. EPM7032B External Timing Parameters** *Notes (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3.5 | | -5.0 | | -7.5 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 3.5 | | 5.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 3.5 | | 5.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.1 | | 3.0 | | 4.5 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.0 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 2.4 | 1.0 | 3.4 | 1.0 | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 0.9 | | 1.3 | | 1.9 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | 0.6 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 3.6 | 1.0 | 5.1 | 1.0 | 7.6 | ns |
| $t_{ACH}$ | Array clock high time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 3.3 | | 4.7 | | 7.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 303.0 | | 212.8 | | 142.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 3.3 | | 4.7 | | 7.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 303.0 | | 212.8 | | 142.9 | | MHz |

*Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays* *Notes (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -3.5 | | -5.0 | | -7.5 | | |
| | | Min | Max | Min | Max | Min | Max | |
| 3.3 V TTL/CMOS | Input to (PIA) | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| 2.5 V TTL/CMOS | Input to PIA | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to global clock and clear | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to fast input register | | 0.2 | | 0.3 | | 0.4 | ns |
| | All outputs | | 0.2 | | 0.3 | | 0.4 | ns |
| 1.8 V TTL/CMOS | Input to PIA | | 0.5 | | 0.8 | | 1.1 | ns |
| | Input to global clock and clear | | 0.5 | | 0.8 | | 1.1 | ns |
| | Input to fast input register | | 0.4 | | 0.5 | | 0.8 | ns |
| | All outputs | | 1.2 | | 1.8 | | 2.6 | ns |
| SSTL-2 Class I | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-2 Class II | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | –0.1 | | –0.1 | | –0.2 | ns |
| SSTL-3 Class I | Input to PIA | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-3 Class II | Input to PIA | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| GTL+ | Input to PIA | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to global clock and clear | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to fast input register | | 1.5 | | 2.1 | | 3.2 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

| Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays *Notes (1)* | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **I/O Standard** | **Parameter** | **Speed Grade** | | | | | | **Unit** |
| | | **-3.5** | | **-5.0** | | **-7.5** | | |
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of all LABs.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

*Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -5 | | -7 | | |
| | | Min | Max | Min | Max | Min | Max | |
| 3.3 V TTL/CMOS | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| 2.5 V TTL/CMOS | Input to PIA | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to global clock and clear | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to fast input register | | 0.2 | | 0.3 | | 0.4 | ns |
| | All outputs | | 0.2 | | 0.3 | | 0.4 | ns |
| 1.8 V TTL/CMOS | Input to PIA | | 0.5 | | 0.7 | | 1.1 | ns |
| | Input to global clock and clear | | 0.5 | | 0.7 | | 1.1 | ns |
| | Input to fast input register | | 0.4 | | 0.6 | | 0.9 | ns |
| | All outputs | | 1.2 | | 1.7 | | 2.6 | ns |
| SSTL-2 Class I | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-2 Class II | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | –0.1 | | –0.1 | | –0.2 | ns |
| SSTL-3 Class I | Input to PIA | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-3 Class II | Input to PIA | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| GTL+ | Input to PIA | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to global clock and clear | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to fast input register | | 1.5 | | 2.1 | | 3.2 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Table 25. EPM7128B Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.6 | | 0.8 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.6 | | 0.8 | ns |
| $t_{FIN}$ | Fast input delay | | | 1.3 | | 2.9 | | 3.7 | ns |
| $t_{FIND}$ | Programmable delay adder for fast input | | | 1.0 | | 1.5 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.5 | | 2.8 | | 3.8 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.6 | | 2.9 | | 3.8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.4 | | 2.6 | | 3.4 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.1 | | 0.3 | | 0.4 | ns |
| $t_{OD1}$ | Output buffer and pad delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.9 | | 1.7 | | 2.2 | ns |
| $t_{OD3}$ | Output buffer and pad delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.9 | | 6.7 | | 7.2 | ns |
| $t_{ZX1}$ | Output buffer enable delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.8 | | 3.3 | | 4.4 | ns |
| $t_{ZX3}$ | Output buffer enable delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.8 | | 8.3 | | 9.4 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 1.8 | | 3.3 | | 4.4 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 1.9 | | 2.6 | | ns |
| $t_{H}$ | Register hold time | | 0.4 | | 0.8 | | 1.1 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 0.8 | | 0.9 | | 0.9 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.2 | | 1.6 | | 1.6 | | ns |
| $t_{RD}$ | Register delay | | | 0.5 | | 1.1 | | 1.4 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{IC}$ | Array clock delay | | | 1.4 | | 2.8 | | 3.6 | ns |
| $t_{EN}$ | Register enable time | | | 1.4 | | 2.6 | | 3.4 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.1 | | 2.3 | | 3.1 | ns |
| $t_{PRE}$ | Register preset time | | | 1.0 | | 1.9 | | 2.6 | ns |
| $t_{CLR}$ | Register clear time | | | 1.0 | | 1.9 | | 2.6 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 1.0 | | 2.0 | | 2.8 | ns |
| $t_{LPA}$ | Low-power adder | *(4)* | | 1.5 | | 2.8 | | 3.8 | ns |

*Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -4 | | -7 | | -10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

*Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -5 | | -7 | | -10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

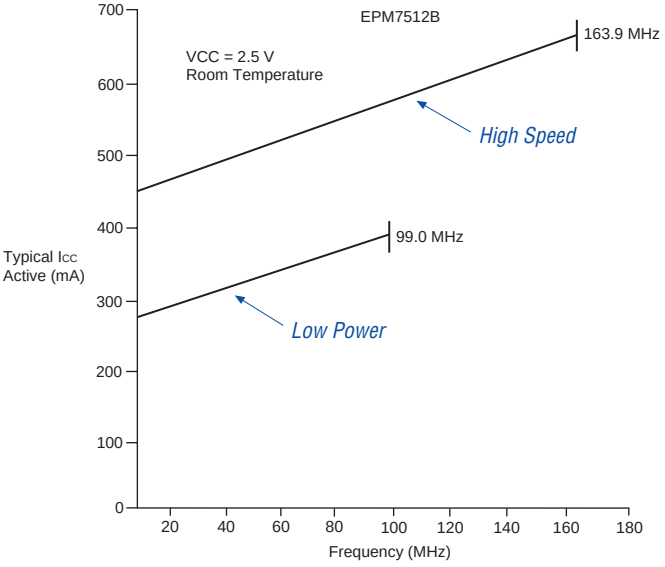
## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

*Figure 19. $I_{CC}$ vs. Frequency for EPM7512B Devices*



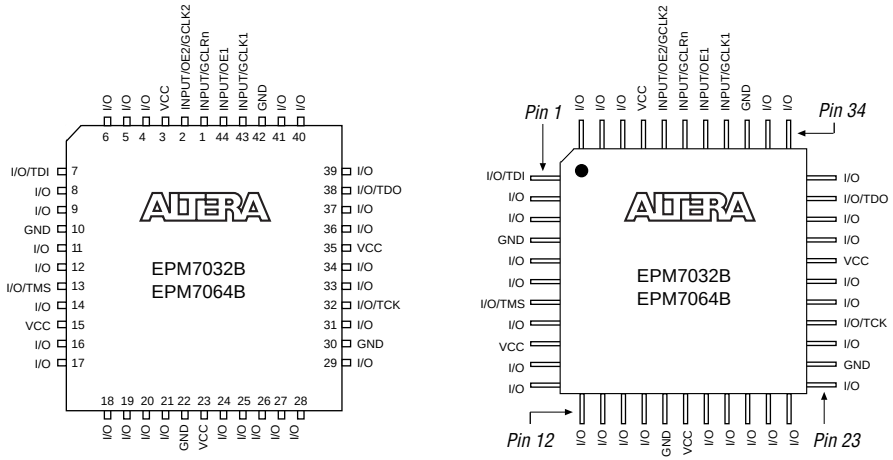
# Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

***Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram***

*Package outlines not drawn to scale.*




44-Pin PLCC

44-Pin TQFP

*Figure 25. 144-Pin TQFP Package Pin-Out Diagram*

*Package outline not drawn to scale.*

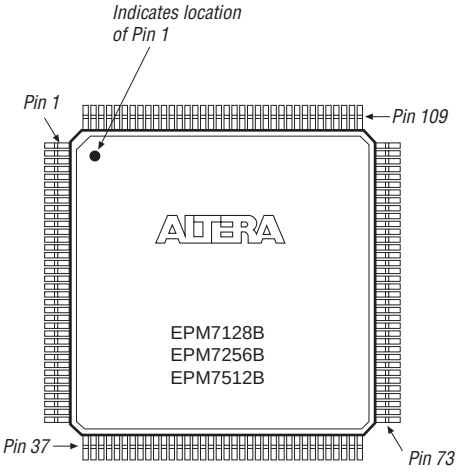



*Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram*

*Package outline not drawn to scale.*

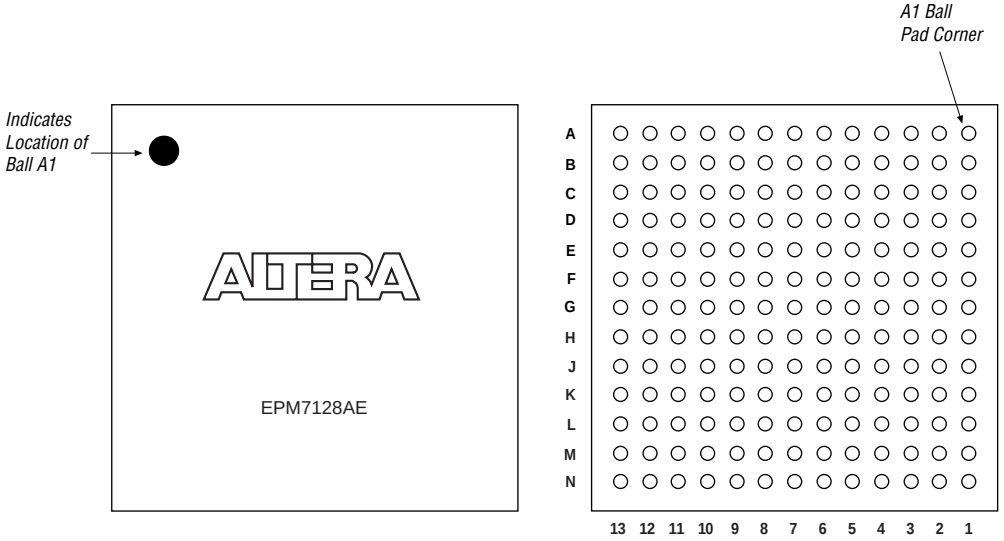
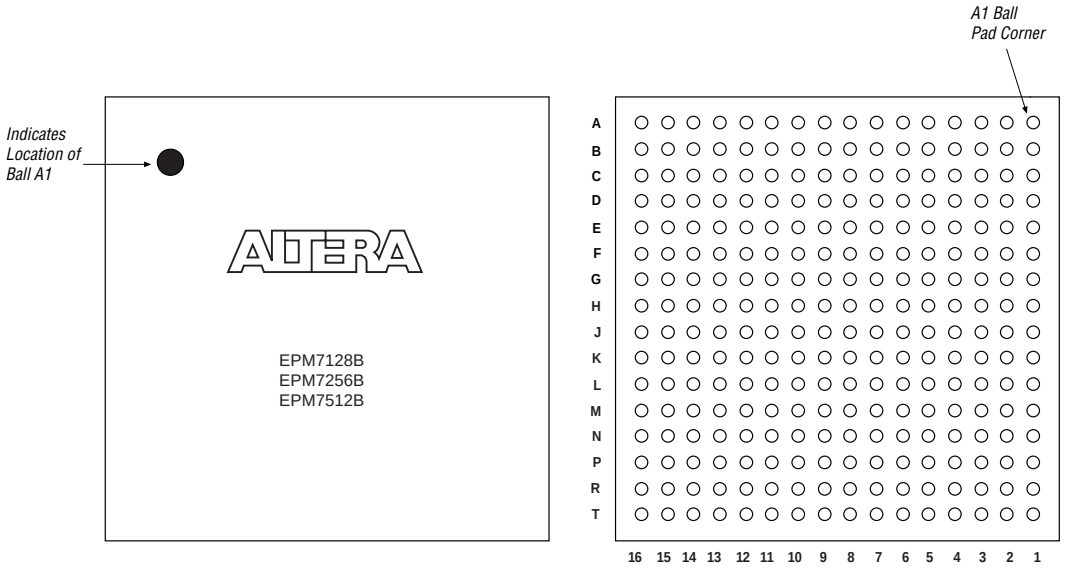


*Figure 29. 256-Pin FineLine BGA Package Pin-Out Diagram*

*Package outline not drawn to scale.*




# Revision History

The information contained in the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.5 supersedes information published in previous versions.

## Version 3.5

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.5:

- Updated Figure 28.

## Version 3.4

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.4:

- Updated text in the "Power Sequencing & Hot-Socketing" section.

## Version 3.3

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.3:

- Updated Table 3.
- Added Tables 4 through 6.

## Version 3.2

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.2:

- Updated *Note (10)* and added ambient temperature ($T_A$) information to Table 15.

## Version 3.1

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.1:

- Updated $V_{IH}$ and $V_{IL}$ specifications in Table 16.
- Updated leakage current conditions in Table 16.

## Version 3.0

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.0:

- Updated timing numbers in Table 1.
- Updated Table 16.
- Updated timing in Tables 18, 19, 21, 22, 24, 25, 27, 28, 30, and 31.

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