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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=epm7128bfc256-4">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=epm7128bfc256-4</a>

## ...and More Features

- System-level features
  - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
  - Programmable power-saving mode for 50% or greater power reduction in each macrocell
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
  - Bus-hold option on I/O pins
  - PCI compatible
  - Bus-friendly architecture including programmable slew-rate control
  - Open-drain output option
  - Programmable security bit for protection of proprietary designs
  - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
  - Supports hot-socketing operation
  - Programmable ground pins
- Advanced architecture features
  - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
  - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
  - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
  - Two global clock signals with optional inversion
  - Programmable power-up states for macrocell registers
  - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
  - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
  - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
  - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera’s Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf)-capable in-circuit tester

## General Description

MAX 7000B devices are high-density, high-performance devices based on Altera’s second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See [Table 2](#).

<b>Table 2. MAX 7000B Speed Grades</b> <i>Note (1)</i>					
Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

**Notes:**

- (1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See [Table 3](#).

**Table 3. MAX 7000B Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP (2)	49-Pin 0.8-mm Ultra FineLine BGA (3)	100- Pin TQFP	100-Pin FineLine BGA (4)	144- Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA (3)	208- Pin PQFP	256- Pin BGA	256-Pin FineLine BGA (4)
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B				41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B							120	141	176	212	212

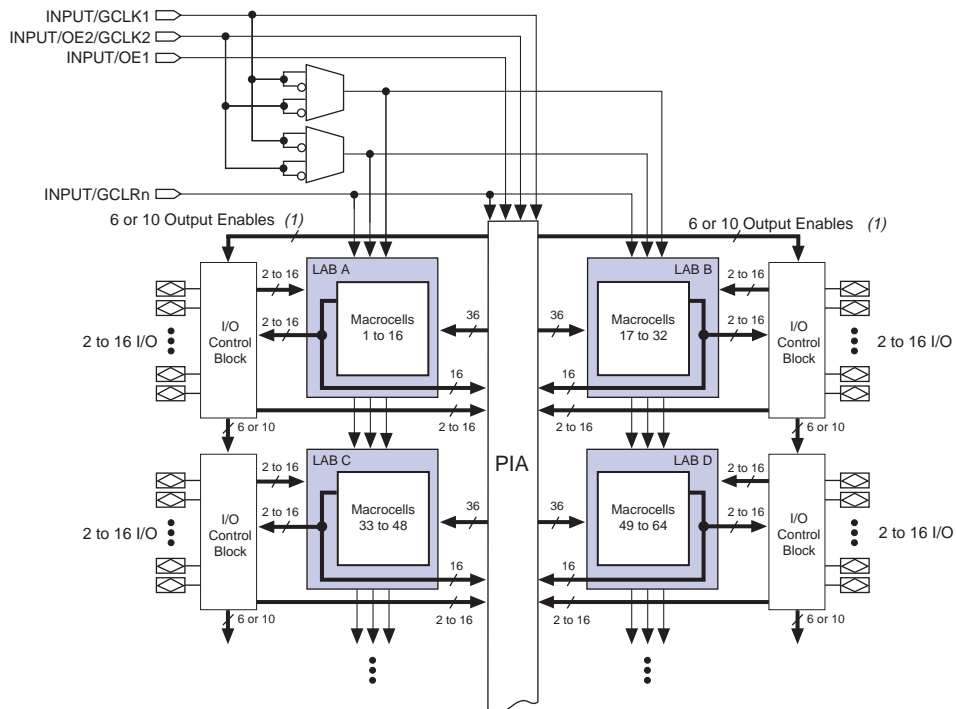
**Notes:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) Contact Altera for up-to-date information on available device package options.
- (3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.
- (4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

Figure 1. MAX 7000B Device Block Diagram



**Note:**

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

## Logic Array Blocks

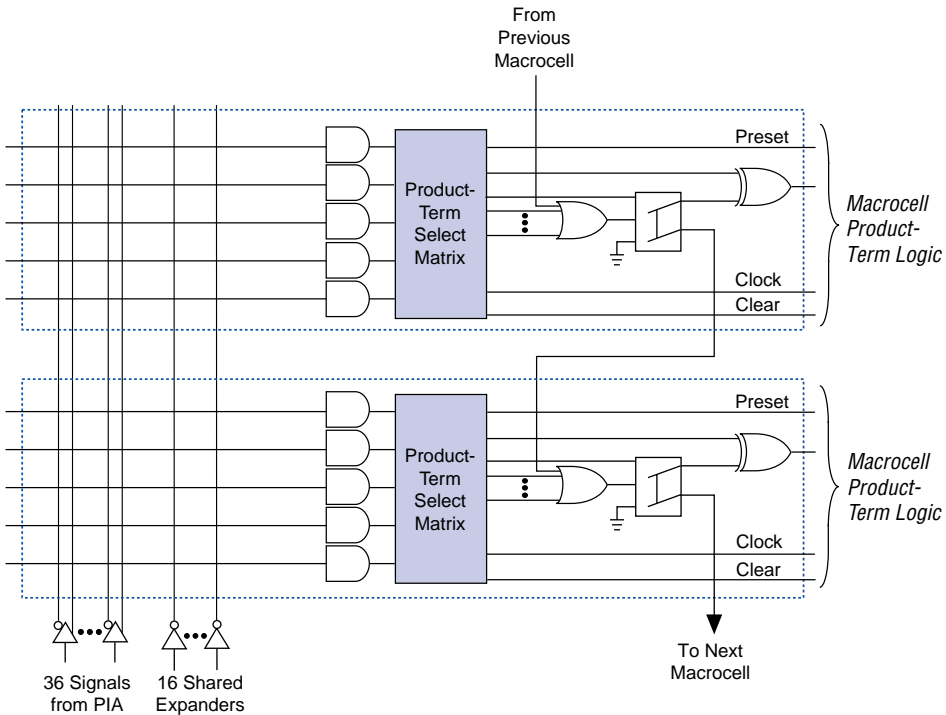
The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

**Figure 4. MAX 7000B Parallel Expanders**

*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



### Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

## Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters.

## Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

The  $V_{CCIO}$  pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

**Table 10. MAX 7000B MultiVolt I/O Support**

V <sub>CCIO</sub> (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

### Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

### Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

### Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

### Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.



I/O Standard	Parameter	Speed Grade						Unit
		-3.5		-5.0		-7.5		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

Table 22. EPM7064B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.5		0.7	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.5		0.7	ns
$t_{FIN}$	Fast input delay			0.9		1.3		2.0	ns
$t_{FIND}$	Programmable delay adder for fast input			1.0		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.1		3.2	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.6		0.9	ns
$t_{LAD}$	Logic array delay			1.4		2.0		3.1	ns
$t_{LAC}$	Logic control array delay			1.2		1.7		2.6	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.3	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.8	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.8	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.6		2.2		3.4	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.6		7.2		8.4	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		1.6		2.2		3.4	ns
$t_{SU}$	Register setup time		0.7		1.1		1.6		ns
$t_H$	Register hold time		0.4		0.5		0.9		ns
$t_{FSU}$	Register setup time of fast input		0.8		0.8		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.2		1.4		ns
$t_{RD}$	Register delay			0.5		0.6		0.9	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.5	ns
$t_{IC}$	Array clock delay			1.2		1.8		2.8	ns
$t_{EN}$	Register enable time			1.2		1.7		2.6	ns
$t_{GLOB}$	Global control delay			0.7		1.1		1.6	ns
$t_{PRE}$	Register preset time			1.0		1.3		1.9	ns
$t_{CLR}$	Register clear time			1.0		1.3		1.9	ns
$t_{PIA}$	PIA delay	(2)		0.7		1.0		1.4	ns
$t_{LPA}$	Low-power adder	(4)		1.5		2.1		3.2	ns

Table 24. EPM7128B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	C1 = 35 pF (2)		4.0		7.5		10.0	ns
$t_{PD2}$	I/O input to non-registered output	C1 = 35 pF (2)		4.0		7.5		10.0	ns
$t_{SU}$	Global clock setup time	(2)	2.5		4.5		6.1		ns
$t_H$	Global clock hold time	(2)	0.0		0.0		0.0		ns
$t_{FSU}$	Global clock setup time of fast input		1.0		1.5		1.5		ns
$t_{FH}$	Global clock hold time of fast input		1.0		1.0		1.0		ns
$t_{FZHSU}$	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
$t_{FZHH}$	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
$t_{CO1}$	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.7	1.0	7.5	ns
$t_{CH}$	Global clock high time		1.5		3.0		4.0		ns
$t_{CL}$	Global clock low time		1.5		3.0		4.0		ns
$t_{ASU}$	Array clock setup time	(2)	1.2		2.0		2.8		ns
$t_{AH}$	Array clock hold time	(2)	0.2		0.7		0.9		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF (2)	1.0	4.1	1.0	8.2	1.0	10.8	ns
$t_{ACH}$	Array clock high time		1.5		3.0		4.0		ns
$t_{ACL}$	Array clock low time		1.5		3.0		4.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset		1.5		3.0		4.0		ns
$t_{CNT}$	Minimum global clock period	(2)		4.1		7.9		10.6	ns
$f_{CNT}$	Maximum internal global clock frequency	(2), (3)	243.9		126.6		94.3		MHz
$t_{ACNT}$	Minimum array clock period	(2)		4.1		7.9		10.6	ns
$f_{ACNT}$	Maximum internal array clock frequency	(2), (3)	243.9		126.6		94.3		MHz

Table 25. EPM7128B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.6		0.8	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.6		0.8	ns
$t_{FIN}$	Fast input delay			1.3		2.9		3.7	ns
$t_{FIND}$	Programmable delay adder for fast input			1.0		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.8		3.8	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.8		1.0	ns
$t_{LAD}$	Logic array delay			1.6		2.9		3.8	ns
$t_{LAC}$	Logic control array delay			1.4		2.6		3.4	ns
$t_{IOE}$	Internal output enable delay			0.1		0.3		0.4	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.7		2.2	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.7		7.2	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.8		3.3		4.4	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.8		8.3		9.4	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		1.8		3.3		4.4	ns
$t_{SU}$	Register setup time		1.0		1.9		2.6		ns
$t_{H}$	Register hold time		0.4		0.8		1.1		ns
$t_{FSU}$	Register setup time of fast input		0.8		0.9		0.9		ns
$t_{FH}$	Register hold time of fast input		1.2		1.6		1.6		ns
$t_{RD}$	Register delay			0.5		1.1		1.4	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.4	ns
$t_{IC}$	Array clock delay			1.4		2.8		3.6	ns
$t_{EN}$	Register enable time			1.4		2.6		3.4	ns
$t_{GLOB}$	Global control delay			1.1		2.3		3.1	ns
$t_{PRE}$	Register preset time			1.0		1.9		2.6	ns
$t_{CLR}$	Register clear time			1.0		1.9		2.6	ns
$t_{PIA}$	PIA delay	(2)		1.0		2.0		2.8	ns
$t_{LPA}$	Low-power adder	(4)		1.5		2.8		3.8	ns

Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.6		0.8	ns
	Input to global clock and clear		0.3		0.6		0.8	ns
	Input to fast input register		0.2		0.4		0.5	ns
	All outputs		0.2		0.4		0.5	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.9		1.3	ns
	Input to global clock and clear		0.5		0.9		1.3	ns
	Input to fast input register		0.4		0.8		1.0	ns
	All outputs		1.2		2.3		3.0	ns
SSTL-2 Class I	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		-0.1		-0.2		-0.3	ns
SSTL-3 Class I	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.7		3.2		4.3	ns
	Input to global clock and clear		1.7		3.2		4.3	ns
	Input to fast input register		1.6		3.0		4.0	ns
	All outputs		0.0		0.0		0.0	ns

**Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		-0.1		-0.2		-0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.5		0.7	ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.3	ns
	All outputs		0.2		0.3		0.3	ns
1.8 V TTL/CMOS	Input to PIA		0.7		1.0		1.3	ns
	Input to global clock and clear		0.6		0.8		1.0	ns
	Input to fast input register		0.5		0.6		0.8	ns
	All outputs		1.3		1.8		2.3	ns
SSTL-2 Class I	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		-0.1		-0.1		-0.2	ns
SSTL-3 Class I	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.5		3.3	ns
	Input to global clock and clear		1.9		2.6		3.5	ns
	Input to fast input register		1.8		2.5		3.3	ns
	All outputs		0.0		0.0		0.0	ns

**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$ , in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).



The  $I_{CCINT}$  value depends on the switching frequency and the application logic. The  $I_{CCINT}$  value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$$

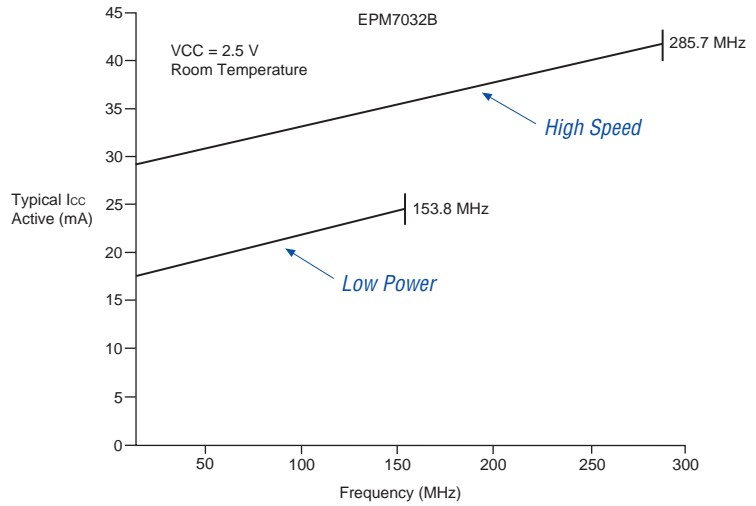
The parameters in this equation are:

- $MC_{TON}$  = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (.rpt)  
 $MC_{DEV}$  = Number of macrocells in the device  
 $MC_{USED}$  = Total number of macrocells in the design, as reported in the Report File  
 $f_{MAX}$  = Highest clock frequency to the device  
 $tog_{LC}$  = Average percentage of logic cells toggling at each clock (typically 12.5%)  
A, B, C = Constants, shown in [Table 33](#)

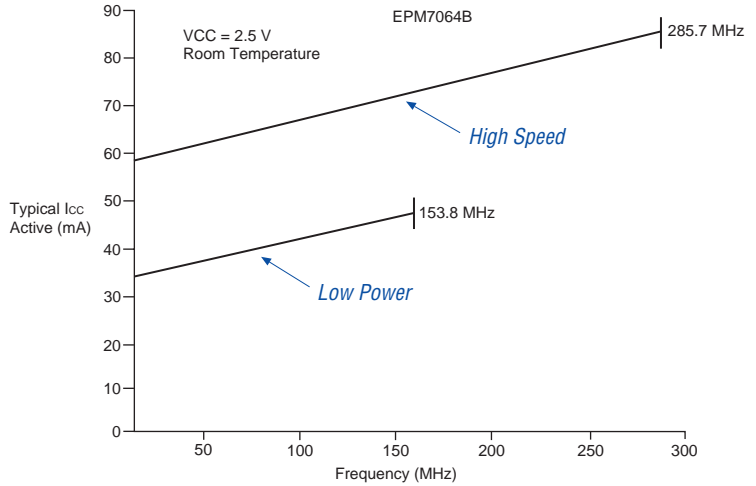
Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an  $I_{CC}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

**Figure 15.  $I_{CC}$  vs. Frequency for EPM7032B Devices**



**Figure 16.  $I_{CC}$  vs. Frequency for EPM7064B Devices**



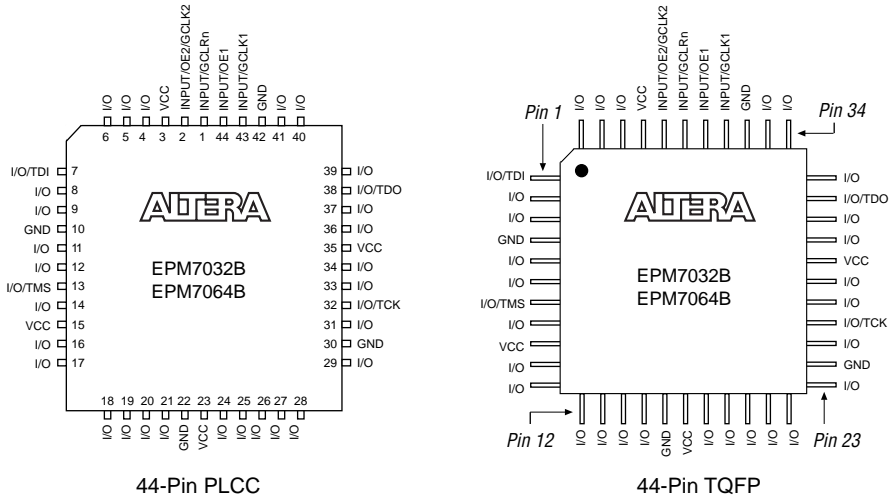
## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

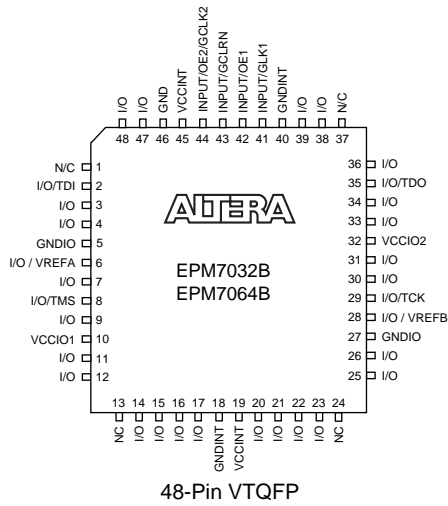
**Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram**

*Package outlines not drawn to scale.*



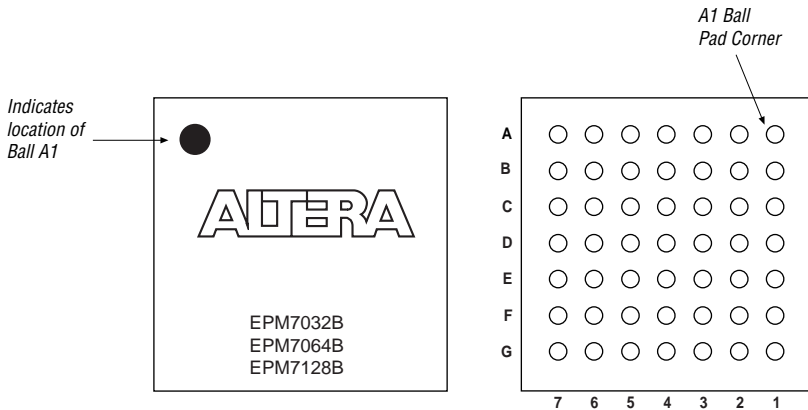
**Figure 21. 48-Pin VTQFP Package Pin-Out Diagram**

Package outlines not drawn to scale.



**Figure 22. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram**

Package outline not drawn to scale.



### Version 3.3

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.3:

- Updated [Table 3](#).
- Added [Tables 4](#) through [6](#).

### Version 3.2

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.2:

- Updated [Note \(10\)](#) and added ambient temperature ( $T_A$ ) information to [Table 15](#).

### Version 3.1

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.1:

- Updated  $V_{IH}$  and  $V_{IL}$  specifications in [Table 16](#).
- Updated leakage current conditions in [Table 16](#).

### Version 3.0

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.0:

- Updated timing numbers in [Table 1](#).
- Updated [Table 16](#).
- Updated timing in [Tables 18, 19, 21, 22, 24, 25, 27, 28, 30, and 31](#).



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