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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	41
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	49-LFBGA
Supplier Device Package	49-UBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128bfc49-4

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000B devices.

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

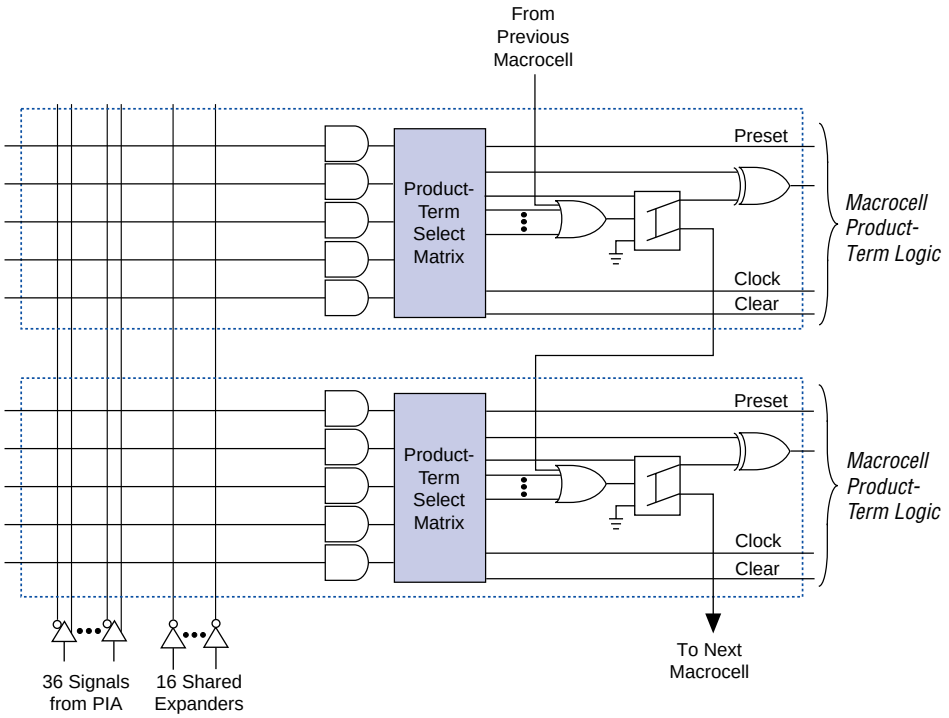
Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Figure 4. MAX 7000B Parallel Expanders

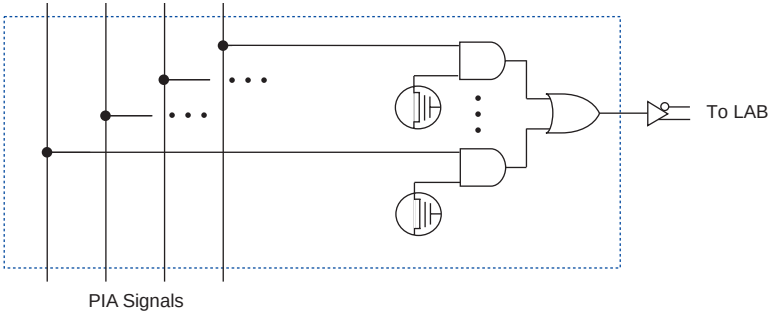
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000B PIA Routing



While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCIO` pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

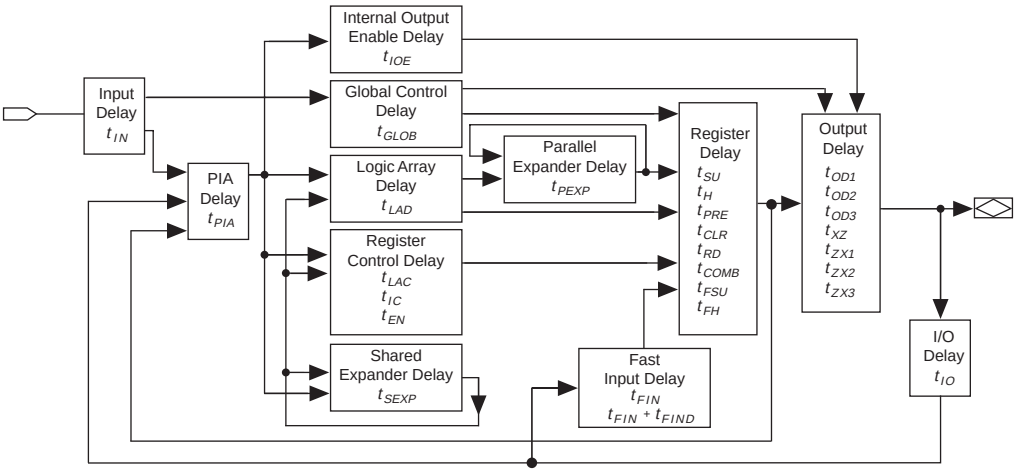
Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Tables 18 through 32 show MAX 7000B device timing parameters.

Table 18. EPM7032B External Timing Parameters *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(2)*	2.1		3.0		4.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.9		1.3		1.9		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	3.6	1.0	5.1	1.0	7.6	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(2)*		3.3		4.7		7.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		3.3		4.7		7.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz

Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays *Notes (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3.5		-5.0		-7.5		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to (PIA)		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.8		1.1	ns
	Input to global clock and clear		0.5		0.8		1.1	ns
	Input to fast input register		0.4		0.5		0.8	ns
	All outputs		1.2		1.8		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.8		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.8		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		–0.1		–0.1		–0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.8		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.8		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.6		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

Table 21. EPM7064B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(2)*	2.1		3.0		4.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.9		1.3		1.9		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	3.6	1.0	5.1	1.0	7.6	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(2)*		3.3		4.7		7.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		3.3		4.7		7.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz

Table 22. EPM7064B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_{H}	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	*(2)*		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.1		3.2	ns

Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of all LABs.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 24. EPM7128B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	2.5		4.5		6.1		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.7	1.0	7.5	ns
t_{CH}	Global clock high time		1.5		3.0		4.0		ns
t_{CL}	Global clock low time		1.5		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.2		2.0		2.8		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.7		0.9		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.1	1.0	8.2	1.0	10.8	ns
t_{ACH}	Array clock high time		1.5		3.0		4.0		ns
t_{ACL}	Array clock low time		1.5		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.1		7.9		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	243.9		126.6		94.3		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.1		7.9		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	243.9		126.6		94.3		MHz

Table 31. EPM7512B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.3		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.3		0.5	ns
t_{FIN}	Fast input delay			2.2		3.2		4.0	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		2.7	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.7	ns
t_{LAD}	Logic array delay			1.7		2.3		3.0	ns
t_{LAC}	Logic control array delay			1.5		2.0		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.2	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.6	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		2.8		3.8		5.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		7.8		8.8		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.8		3.8		5.0	ns
t_{SU}	Register setup time		1.5		2.0		2.6		ns
t_{H}	Register hold time		0.4		0.5		0.7		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.5		0.7		1.0	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.8		2.4		3.1	ns
t_{EN}	Register enable time			1.5		2.0		2.6	ns
t_{GLOB}	Global control delay			2.0		2.8		3.6	ns
t_{PRE}	Register preset time			1.0		1.4		1.9	ns
t_{CLR}	Register clear time			1.0		1.4		1.9	ns
t_{PIA}	PIA delay	*(2)*		2.4		3.4		4.5	ns
t_{LPA}	Low-power adder	*(4)*		2.0		2.7		3.6	ns

Figure 15. I_{CC} vs. Frequency for EPM7032B Devices

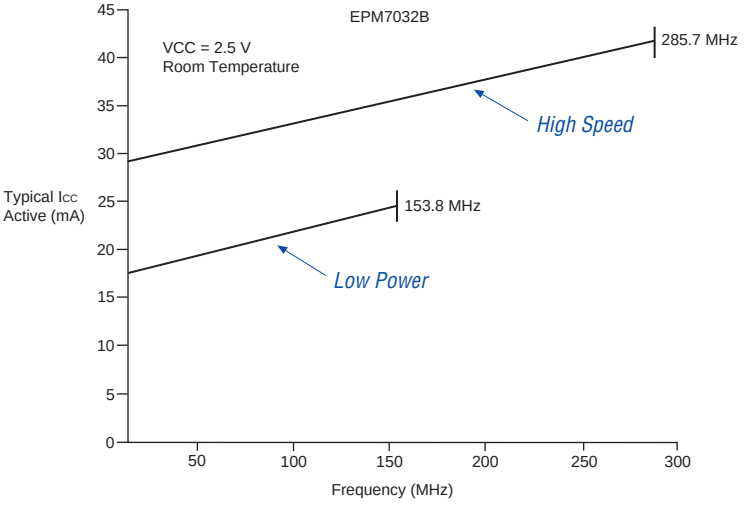


Figure 16. I_{CC} vs. Frequency for EPM7064B Devices

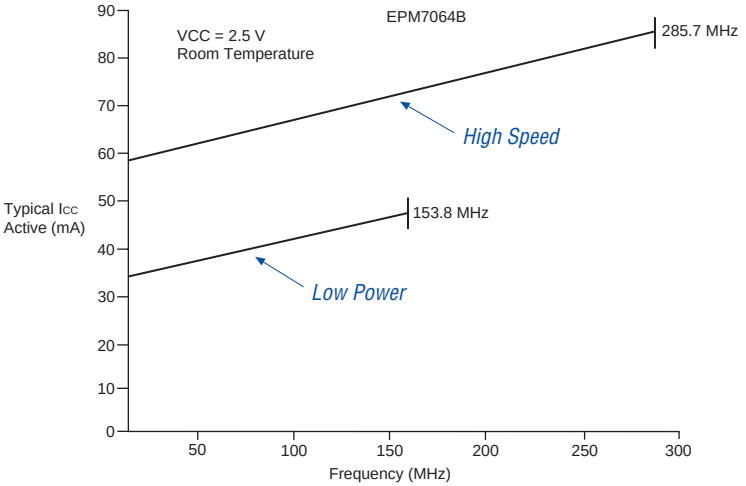


Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

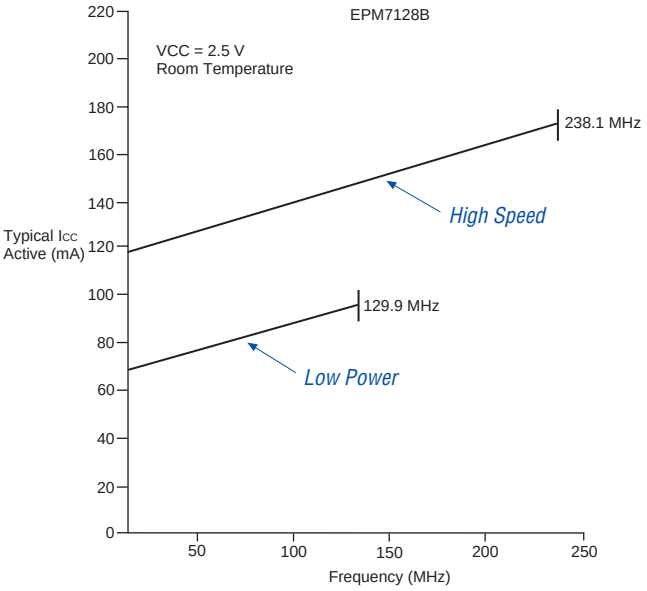
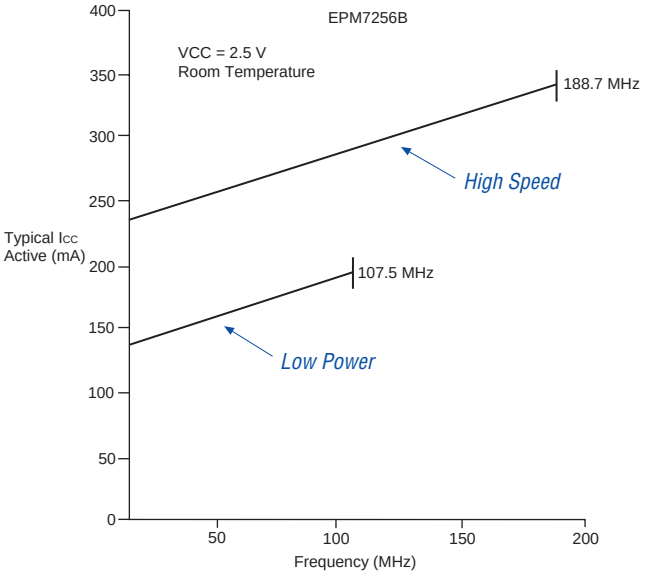


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices



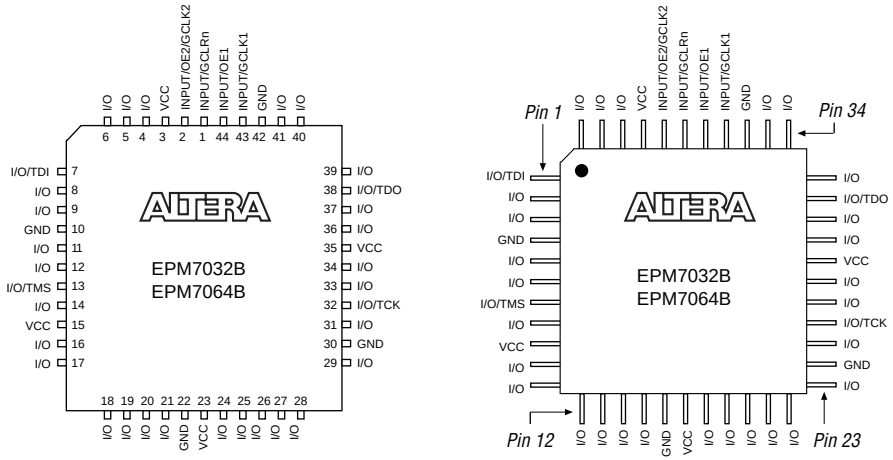
Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TQFP

Figure 25. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

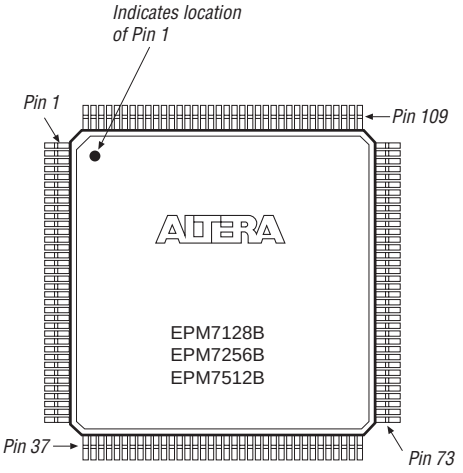


Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram

Package outline not drawn to scale.

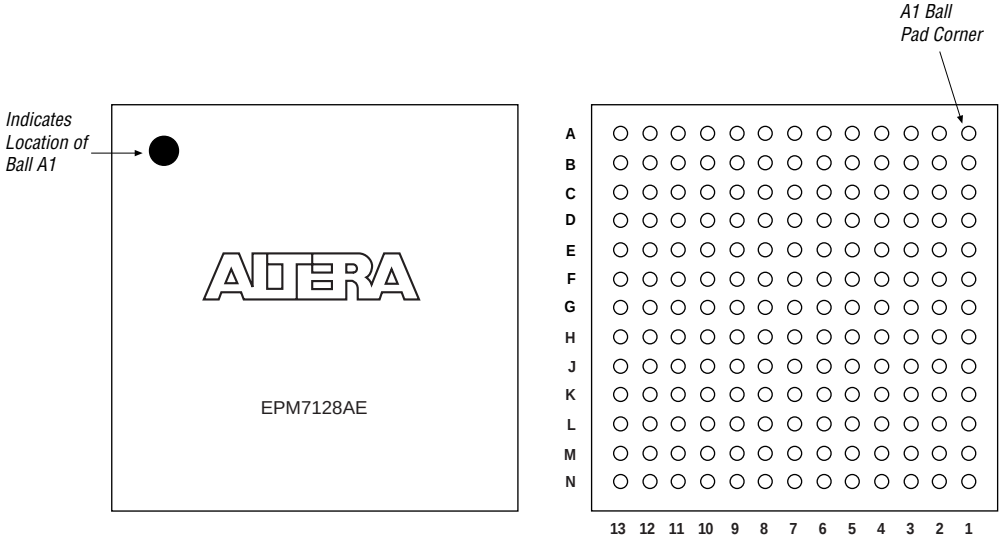


Figure 27. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.