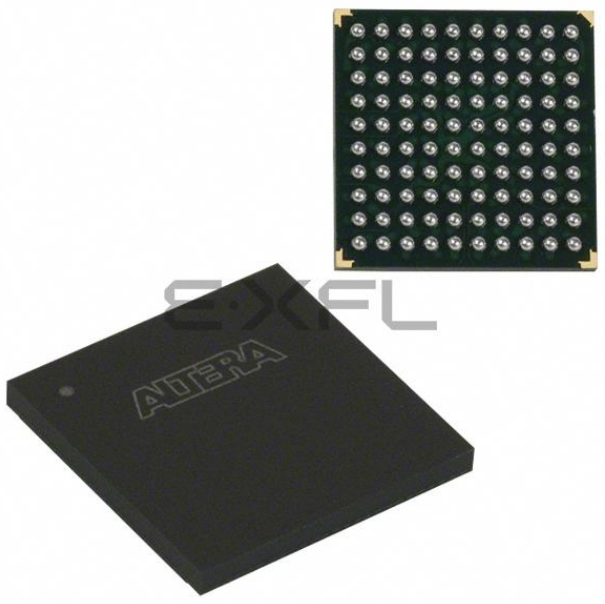

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128bfi100-7

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See Table 2.

Table 2. MAX 7000B Speed Grades *Note (1)*

Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

Notes:
(1) Contact Altera Marketing for up-to-date information on available device speed grades.

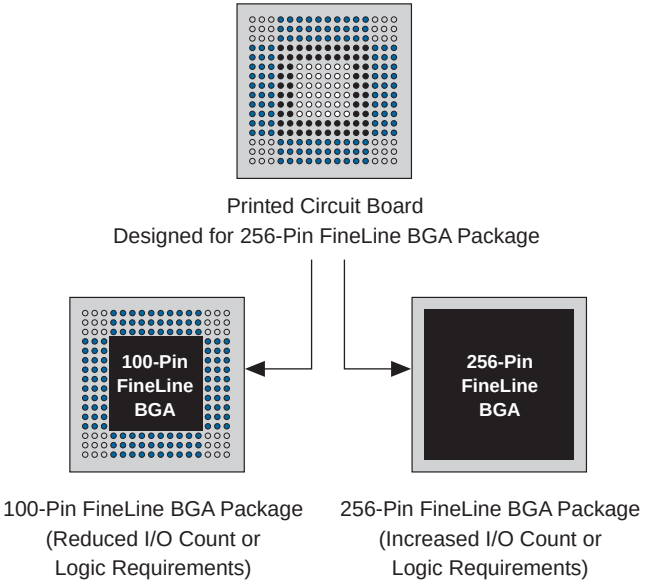
The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See Table 3.

SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see Figure 7).

Figure 7. SameFrame Pin-Out Example



Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000B device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

The programming times described in Tables 4 through 6 are associated with the worst-case method using the enhanced ISP algorithm.

Table 4. MAX 7000B t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EMP7032B	2.12	70,000	0.002	18,000
EMP7064B	2.12	120,000	0.002	35,000
EMP7128B	2.12	222,000	0.002	69,000
EMP7256B	2.12	466,000	0.002	151,000
EMP7512B	2.12	914,000	0.002	300,000

Tables 5 and 6 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 5. MAX 7000B In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	2.13	2.13	2.15	2.19	2.26	2.47	2.82	3.52	s
EMP7064B	2.13	2.14	2.18	2.24	2.36	2.72	3.32	4.52	s
EMP7128B	2.14	2.16	2.23	2.34	2.56	3.23	4.34	6.56	s
EMP7256B	2.17	2.21	2.35	2.58	3.05	4.45	6.78	11.44	s
EMP7512B	2.21	2.30	2.58	3.03	3.95	6.69	11.26	20.40	s

Table 1. MAX 7000B Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EMP7064B	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EMP7128B	0.01	0.02	0.04	0.07	0.14	0.35	0.69	1.38	s
EMP7256B	0.02	0.03	0.08	0.15	0.30	0.76	1.51	3.02	s
EMP7512B	0.03	0.06	0.15	0.30	0.60	1.50	3.00	6.00	s

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. Tables 7 and 8 show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

Table 7. MAX 7000B Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

Table 8. 32-Bit MAX 7000B Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

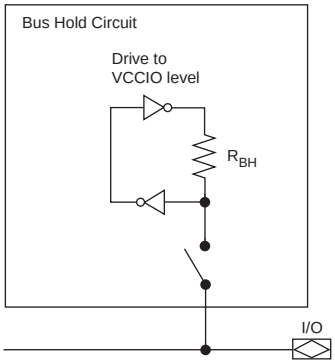
See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG boundary-scan testing.

Figure 8 shows the timing information for the JTAG signals.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the ***PCI Local Bus Specification Revision 2.2*** except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications

Device	Specification	
	33-MHz PCI	66-MHz PCI
EPM7032B	All speed grades	-3
EPM7064B	All speed grades	-3
EPM7128B	All speed grades	-4
EPM7256B	All speed grades	-5 *(1)*
EPM7512B	All speed grades	-5 *(1)*

Note:

(1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

Table 17. MAX 7000B Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

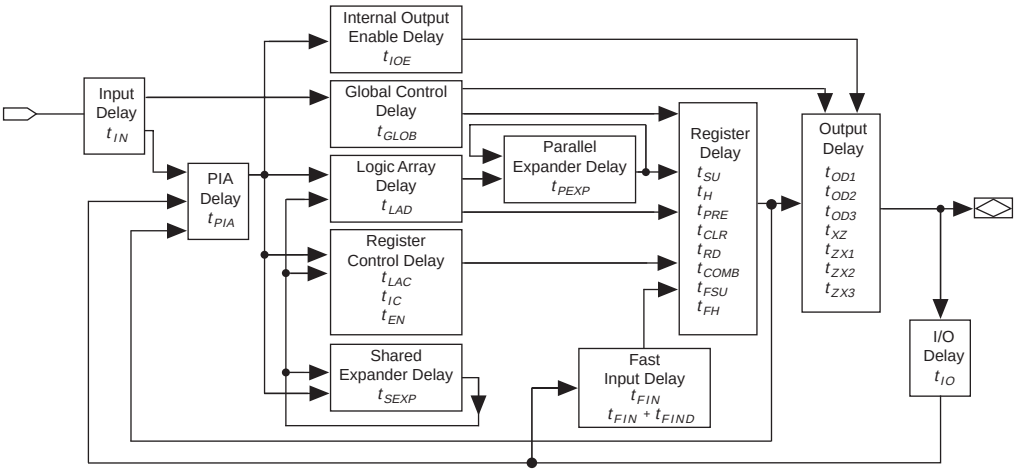
Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(4) These values are specified under the Recommended Operating Conditions in Table 15 on page 29.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
(7) This value is specified for normal device operation. During power-up, the maximum leakage current is ±300 µA.
(8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V_{CCIO}.
(9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.
(10) The POR time for all 7000B devices does not exceed 100 µs. The sufficient V_{CCINT} voltage level for POR is 2.375 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Figure 14. MAX 7000B Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

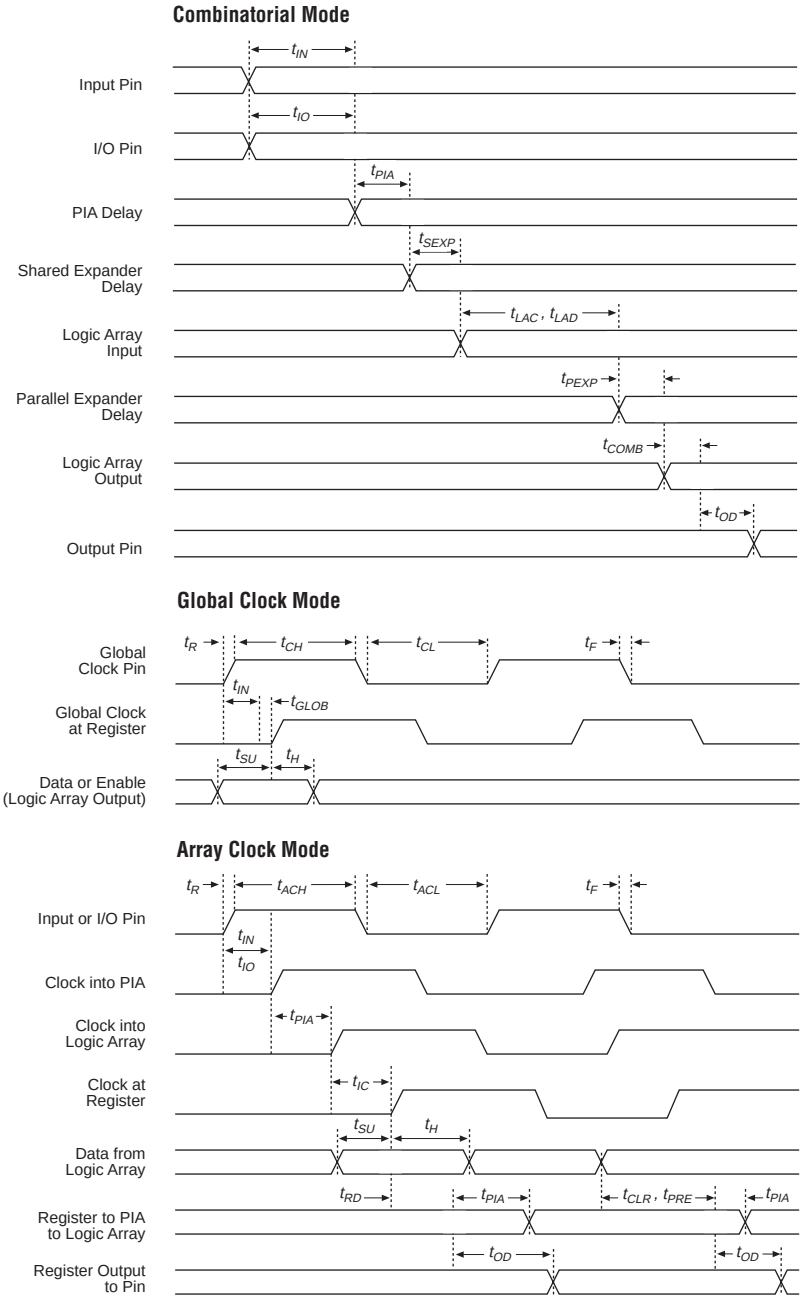


Table 19. EPM7032B Internal Timing Parameters *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_{H}	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	*(2)*		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.1		3.2	ns

Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays *Notes (1)*								
I/O Standard	**Parameter**	**Speed Grade**						**Unit**
		-3.5		**-5.0**		**-7.5**		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of all LABs.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 24. EPM7128B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	2.5		4.5		6.1		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.7	1.0	7.5	ns
t_{CH}	Global clock high time		1.5		3.0		4.0		ns
t_{CL}	Global clock low time		1.5		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.2		2.0		2.8		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.7		0.9		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.1	1.0	8.2	1.0	10.8	ns
t_{ACH}	Array clock high time		1.5		3.0		4.0		ns
t_{ACL}	Array clock low time		1.5		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.1		7.9		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	243.9		126.6		94.3		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.1		7.9		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	243.9		126.6		94.3		MHz

Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 28. EPM7256B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.6		0.8	ns
t_{FIN}	Fast input delay			1.5		2.5		3.1	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.3		3.0	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.8	ns
t_{LAD}	Logic array delay			1.7		2.5		3.3	ns
t_{LAC}	Logic control array delay			1.5		2.2		2.9	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.4		1.9	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.4		6.9	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		2.2		3.3		4.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		7.2		8.3		9.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.2		3.3		4.5	ns
t_{SU}	Register setup time		1.2		1.8		2.5		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.7		1.0		1.3	ns
t_{COMB}	Combinatorial delay			0.3		0.4		0.5	ns
t_{IC}	Array clock delay			1.5		2.3		3.0	ns
t_{EN}	Register enable time			1.5		2.2		2.9	ns
t_{GLOB}	Global control delay			1.3		2.1		2.7	ns
t_{PRE}	Register preset time			1.0		1.6		2.1	ns
t_{CLR}	Register clear time			1.0		1.6		2.1	ns
t_{PIA}	PIA delay	*(2)*		1.7		2.6		3.3	ns
t_{LPA}	Low-power adder	*(4)*		2.0		3.0		4.0	ns

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		–0.1		–0.2		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 33

Table 33. MAX 7000B I_{CC} Equation Constants

Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 15. I_{CC} vs. Frequency for EPM7032B Devices

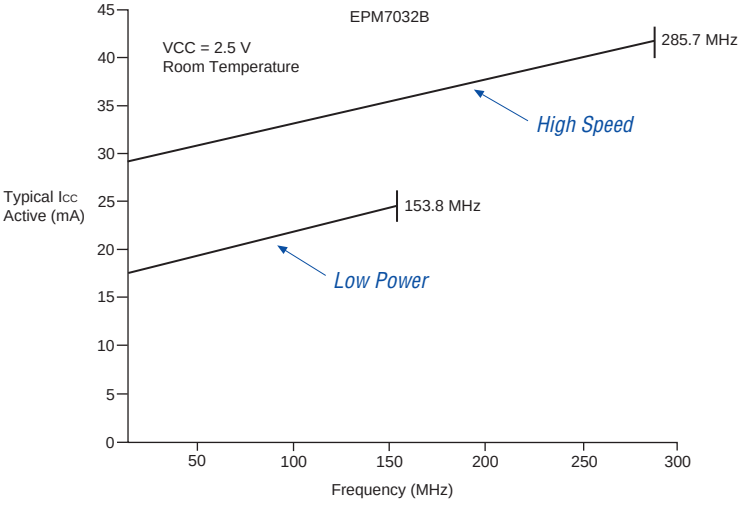


Figure 16. I_{CC} vs. Frequency for EPM7064B Devices

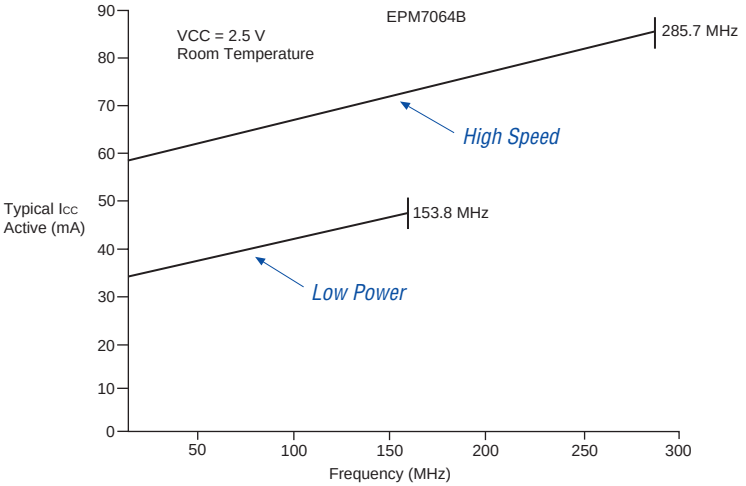


Figure 19. I_{CC} vs. Frequency for EPM7512B Devices

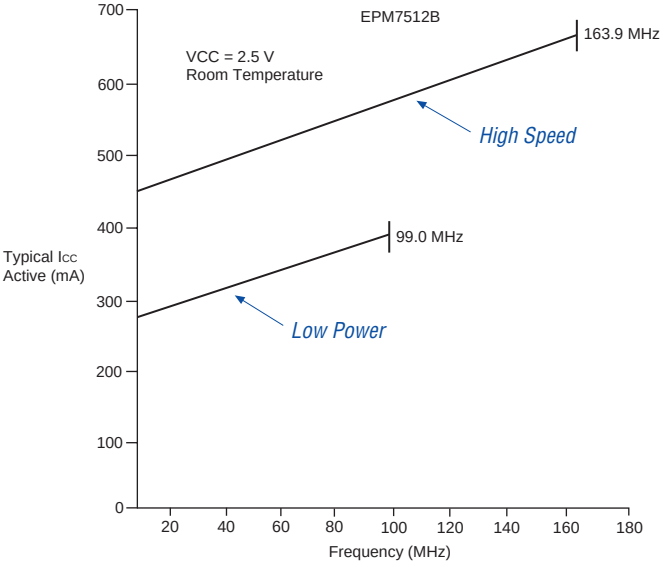


Figure 23. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

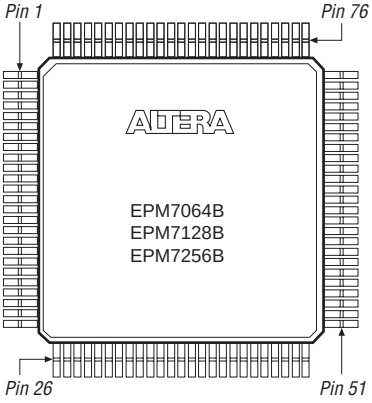


Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

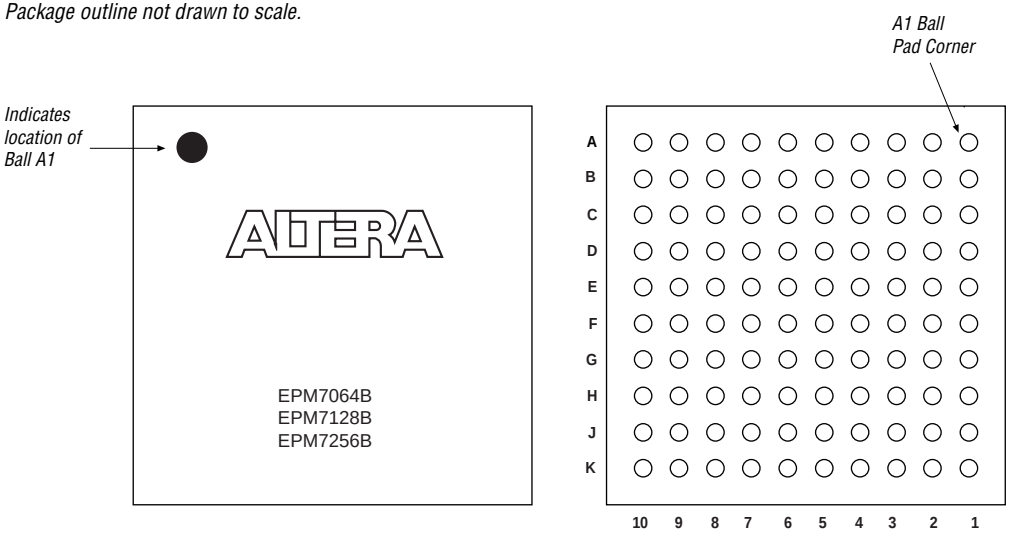


Figure 25. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

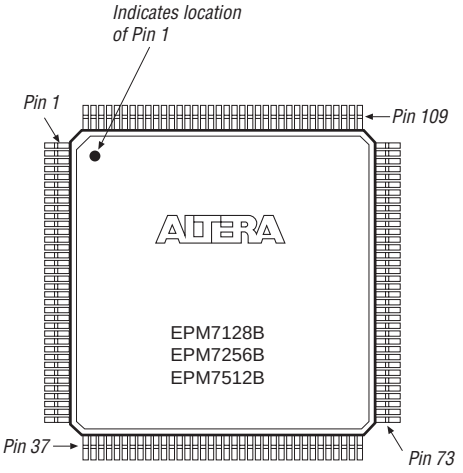


Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram

Package outline not drawn to scale.