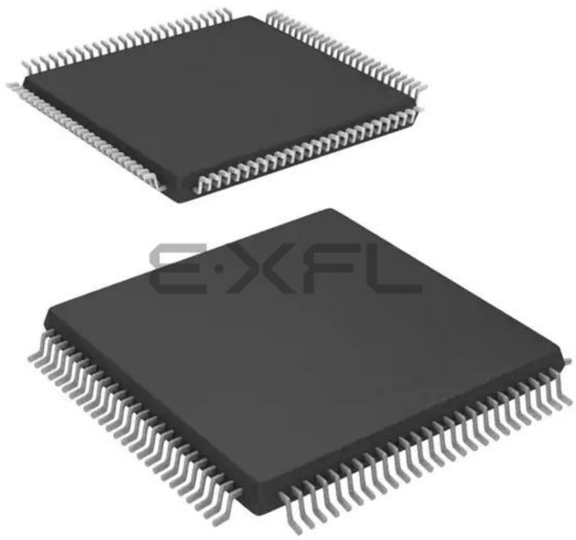
# Intel - EPM7128BTC100-7 Datasheet



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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 2.375V ~ 2.625V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 128 |
| Number of Gates | 2500 |
| Number of I/O | 84 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7128btc100-7 |

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

## General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See Table 2.

**Table 2. MAX 7000B Speed Grades** *Note (1)*

| Device | Speed Grade | | | | |
|---|---|---|---|---|---|
| | -3 | -4 | -5 | -7 | -10 |
| EPM7032B | ✓ | | ✓ | ✓ | |
| EPM7064B | ✓ | | ✓ | ✓ | |
| EPM7128B | | ✓ | | ✓ | ✓ |
| EPM7256B | | | ✓ | ✓ | ✓ |
| EPM7512B | | | ✓ | ✓ | ✓ |

*Notes:*
(1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See Table 3.

*Table 3. MAX 7000B Maximum User I/O Pins Note (1)*

| Device | 44-Pin PLCC | 44-Pin TQFP | 48-Pin TQFP (2) | 49-Pin 0.8-mm Ultra FineLine BGA (3) | 100-Pin TQFP | 100-Pin FineLine BGA (4) | 144-Pin TQFP | 169-Pin 0.8-mm Ultra FineLine BGA (3) | 208-Pin PQFP | 256-Pin BGA | 256-Pin FineLine BGA (4) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EPM7032B | 36 | 36 | 36 | 36 | | | | | | | |
| EPM7064B | 36 | 36 | 40 | 41 | 68 | 68 | | | | | |
| EPM7128B | | | | 41 | 84 | 84 | 100 | 100 | | | 100 |
| EPM7256B | | | | | 84 | | 120 | 141 | 164 | | 164 |
| EPM7512B | | | | | | | 120 | 141 | 176 | 212 | 212 |

*Notes:*

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) Contact Altera for up-to-date information on available device package options.

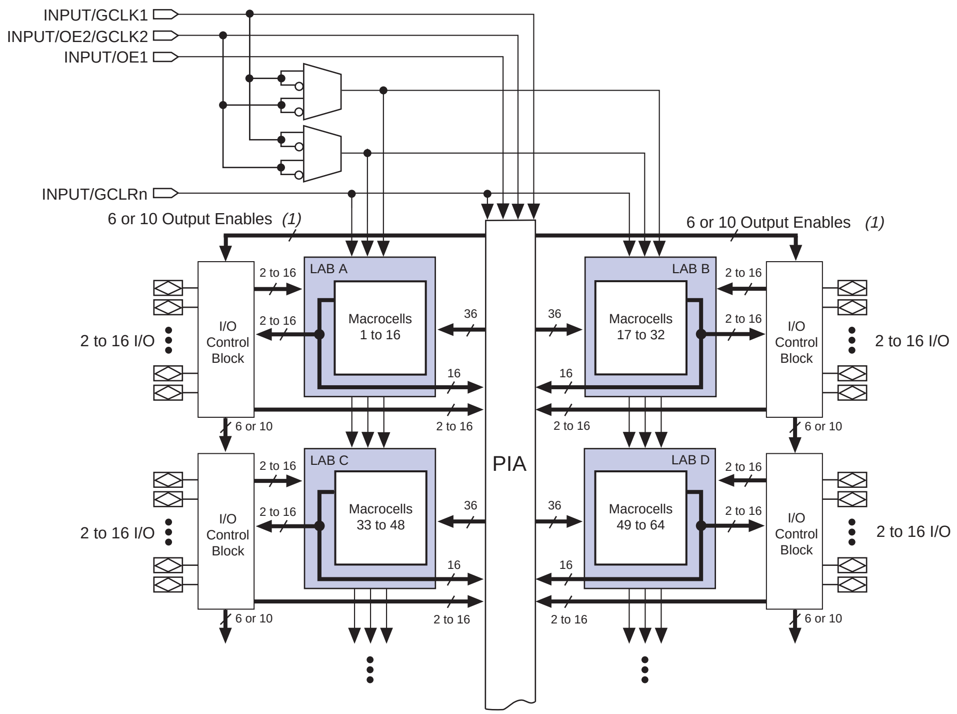
(3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

(4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

*Figure 1. MAX 7000B Device Block Diagram*




*Note:*

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

## Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

## In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k¾.

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using STAPL for ISP & ICR via an Embedded Processor)*.

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000B device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (`TCK`) frequency and the number of `TCK` cycles to shift instructions, address, and data into the device.

*Table 10. MAX 7000B MultiVolt I/O Support*

| $V_{CCIO}$ (V) | Input Signal (V) | | | | Output Signal (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | | | | ✓ | ✓ |

## Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

## Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

## Slew-Rate Control

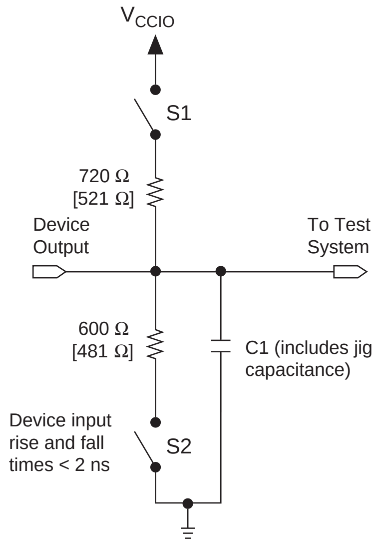
The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

## Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

*Figure 11. MAX 7000B AC Test Conditions*

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.*




## Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

*Table 14. MAX 7000B Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | | –0.5 | 3.6 | V |
| $V_{CCIO}$ | Supply voltage | | –0.5 | 3.6 | V |
| $V_I$ | DC input voltage | (2) | –2.0 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –33 | 50 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_A$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Under bias | –65 | 135 | ° C |

| *Table 17. MAX 7000B Device Capacitance* *Note (9)* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(4) These values are specified under the Recommended Operating Conditions in Table 15 on page 29.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The $I_{OL}$ parameter refers to low-level TTL or CMOS output current.
(7) This value is specified for normal device operation. During power-up, the maximum leakage current is ±300 µA.
(8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to $V_{CCIO}$.
(9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.
(10) The POR time for all 7000B devices does not exceed 100 µs. The sufficient $V_{CCINT}$ voltage level for POR is 2.375 V. The device is fully initialized within the POR time after $V_{CCINT}$ reaches the sufficient POR voltage level.
(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

| *Table 19. EPM7032B Internal Timing Parameters* *Notes (1)* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | **Unit** |
| | | | **-3.5** | | **-5.0** | | **-7.5** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{FIN}$ | Fast input delay | | | 0.9 | | 1.3 | | 2.0 | ns |
| $t_{FIND}$ | Programmable delay adder for fast input | | | 1.0 | | 1.5 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.5 | | 2.1 | | 3.2 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.6 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.4 | | 2.0 | | 3.1 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.2 | | 1.7 | | 2.6 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | Output buffer and pad delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.9 | | 1.2 | | 1.8 | ns |
| $t_{OD3}$ | Output buffer and pad delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.9 | | 6.2 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.6 | | 2.2 | | 3.4 | ns |
| $t_{ZX3}$ | Output buffer enable delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.6 | | 7.2 | | 8.4 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 1.6 | | 2.2 | | 3.4 | ns |
| $t_{SU}$ | Register setup time | | 0.7 | | 1.1 | | 1.6 | | ns |
| $t_{H}$ | Register hold time | | 0.4 | | 0.5 | | 0.9 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 0.8 | | 0.8 | | 1.1 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.2 | | 1.2 | | 1.4 | | ns |
| $t_{RD}$ | Register delay | | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.8 | | 2.8 | ns |
| $t_{EN}$ | Register enable time | | | 1.2 | | 1.7 | | 2.6 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.7 | | 1.1 | | 1.6 | ns |
| $t_{PRE}$ | Register preset time | | | 1.0 | | 1.3 | | 1.9 | ns |
| $t_{CLR}$ | Register clear time | | | 1.0 | | 1.3 | | 1.9 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 0.7 | | 1.0 | | 1.4 | ns |
| $t_{LPA}$ | Low-power adder | *(4)* | | 1.5 | | 2.1 | | 3.2 | ns |

| ***Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays*** *Notes (1)* | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **I/O Standard** | **Parameter** | **Speed Grade** | | | | | | **Unit** |
| | | **-3.5** | | **-5.0** | | **-7.5** | | |
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| 3.3 V TTL/CMOS | Input to (PIA) | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| 2.5 V TTL/CMOS | Input to PIA | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to global clock and clear | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to fast input register | | 0.2 | | 0.3 | | 0.4 | ns |
| | All outputs | | 0.2 | | 0.3 | | 0.4 | ns |
| 1.8 V TTL/CMOS | Input to PIA | | 0.5 | | 0.8 | | 1.1 | ns |
| | Input to global clock and clear | | 0.5 | | 0.8 | | 1.1 | ns |
| | Input to fast input register | | 0.4 | | 0.5 | | 0.8 | ns |
| | All outputs | | 1.2 | | 1.8 | | 2.6 | ns |
| SSTL-2 Class I | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-2 Class II | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | –0.1 | | –0.1 | | –0.2 | ns |
| SSTL-3 Class I | Input to PIA | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-3 Class II | Input to PIA | | 1.2 | | 1.8 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| GTL+ | Input to PIA | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to global clock and clear | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to fast input register | | 1.5 | | 2.1 | | 3.2 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

| *Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays* *Notes (1)* | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **I/O Standard** | **Parameter** | **Speed Grade** | | | | | | **Unit** |
| | | **-3.5** | | **-5.0** | | **-7.5** | | |
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

***Notes to tables:***

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of all LABs.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

*Table 22. EPM7064B Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 | | -5 | | -7 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{FIN}$ | Fast input delay | | | 0.9 | | 1.3 | | 2.0 | ns |
| $t_{FIND}$ | Programmable delay adder for fast input | | | 1.0 | | 1.5 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.5 | | 2.1 | | 3.2 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.6 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.4 | | 2.0 | | 3.1 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.2 | | 1.7 | | 2.6 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | Output buffer and pad delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.9 | | 1.2 | | 1.8 | ns |
| $t_{OD3}$ | Output buffer and pad delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.9 | | 6.2 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.6 | | 2.2 | | 3.4 | ns |
| $t_{ZX3}$ | Output buffer enable delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.6 | | 7.2 | | 8.4 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 1.6 | | 2.2 | | 3.4 | ns |
| $t_{SU}$ | Register setup time | | 0.7 | | 1.1 | | 1.6 | | ns |
| $t_{H}$ | Register hold time | | 0.4 | | 0.5 | | 0.9 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 0.8 | | 0.8 | | 1.1 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.2 | | 1.2 | | 1.4 | | ns |
| $t_{RD}$ | Register delay | | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.8 | | 2.8 | ns |
| $t_{EN}$ | Register enable time | | | 1.2 | | 1.7 | | 2.6 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.7 | | 1.1 | | 1.6 | ns |
| $t_{PRE}$ | Register preset time | | | 1.0 | | 1.3 | | 1.9 | ns |
| $t_{CLR}$ | Register clear time | | | 1.0 | | 1.3 | | 1.9 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 0.7 | | 1.0 | | 1.4 | ns |
| $t_{LPA}$ | Low-power adder | *(4)* | | 1.5 | | 2.1 | | 3.2 | ns |

| *Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) Note (1)* | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **I/O Standard** | **Parameter** | **Speed Grade** | | | | | | **Unit** |
| | | **-3** | | **-5** | | **-7** | | |
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| 3.3 V TTL/CMOS | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| 2.5 V TTL/CMOS | Input to PIA | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to global clock and clear | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to fast input register | | 0.2 | | 0.3 | | 0.4 | ns |
| | All outputs | | 0.2 | | 0.3 | | 0.4 | ns |
| 1.8 V TTL/CMOS | Input to PIA | | 0.5 | | 0.7 | | 1.1 | ns |
| | Input to global clock and clear | | 0.5 | | 0.7 | | 1.1 | ns |
| | Input to fast input register | | 0.4 | | 0.6 | | 0.9 | ns |
| | All outputs | | 1.2 | | 1.7 | | 2.6 | ns |
| SSTL-2 Class I | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-2 Class II | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | –0.1 | | –0.1 | | –0.2 | ns |
| SSTL-3 Class I | Input to PIA | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-3 Class II | Input to PIA | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| GTL+ | Input to PIA | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to global clock and clear | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to fast input register | | 1.5 | | 2.1 | | 3.2 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -5 | | -7 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of all LABs.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

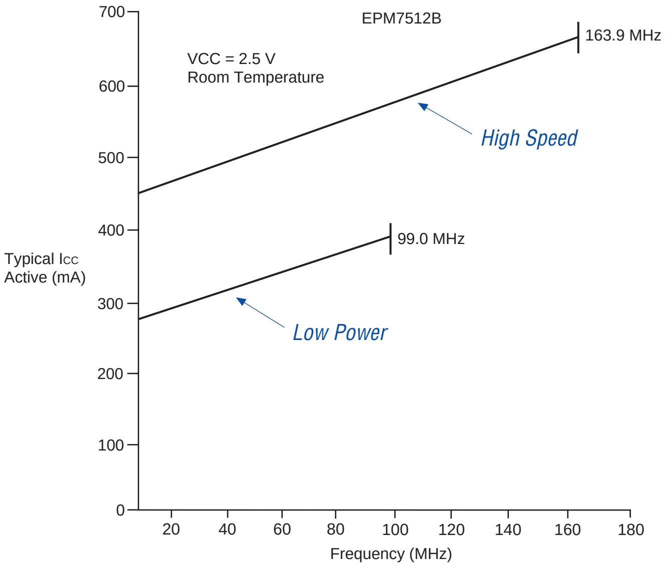
**Table 24. EPM7128B External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 4.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 4.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.5 | | 4.5 | | 6.1 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.0 | | 3.0 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 2.8 | 1.0 | 5.7 | 1.0 | 7.5 | ns |
| $t_{CH}$ | Global clock high time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.2 | | 2.0 | | 2.8 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.7 | | 0.9 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.1 | 1.0 | 8.2 | 1.0 | 10.8 | ns |
| $t_{ACH}$ | Array clock high time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 4.1 | | 7.9 | | 10.6 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 243.9 | | 126.6 | | 94.3 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 4.1 | | 7.9 | | 10.6 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 243.9 | | 126.6 | | 94.3 | | MHz |

**Table 25. EPM7128B Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.6 | | 0.8 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.6 | | 0.8 | ns |
| $t_{FIN}$ | Fast input delay | | | 1.3 | | 2.9 | | 3.7 | ns |
| $t_{FIND}$ | Programmable delay adder for fast input | | | 1.0 | | 1.5 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.5 | | 2.8 | | 3.8 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.6 | | 2.9 | | 3.8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.4 | | 2.6 | | 3.4 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.1 | | 0.3 | | 0.4 | ns |
| $t_{OD1}$ | Output buffer and pad delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.9 | | 1.7 | | 2.2 | ns |
| $t_{OD3}$ | Output buffer and pad delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.9 | | 6.7 | | 7.2 | ns |
| $t_{ZX1}$ | Output buffer enable delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.8 | | 3.3 | | 4.4 | ns |
| $t_{ZX3}$ | Output buffer enable delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.8 | | 8.3 | | 9.4 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 1.8 | | 3.3 | | 4.4 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 1.9 | | 2.6 | | ns |
| $t_{H}$ | Register hold time | | 0.4 | | 0.8 | | 1.1 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 0.8 | | 0.9 | | 0.9 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.2 | | 1.6 | | 1.6 | | ns |
| $t_{RD}$ | Register delay | | | 0.5 | | 1.1 | | 1.4 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{IC}$ | Array clock delay | | | 1.4 | | 2.8 | | 3.6 | ns |
| $t_{EN}$ | Register enable time | | | 1.4 | | 2.6 | | 3.4 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.1 | | 2.3 | | 3.1 | ns |
| $t_{PRE}$ | Register preset time | | | 1.0 | | 1.9 | | 2.6 | ns |
| $t_{CLR}$ | Register clear time | | | 1.0 | | 1.9 | | 2.6 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 1.0 | | 2.0 | | 2.8 | ns |
| $t_{LPA}$ | Low-power adder | *(4)* | | 1.5 | | 2.8 | | 3.8 | ns |

*Figure 19. $I_{CC}$ vs. Frequency for EPM7512B Devices*



# Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

***Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram***

*Package outlines not drawn to scale.*