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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7128btc100-7n">https://www.e-xfl.com/product-detail/intel/epm7128btc100-7n</a>

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf)-capable in-circuit tester

## General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See [Table 2](#).

<b>Table 2. MAX 7000B Speed Grades</b> <i>Note (1)</i>					
Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

### Notes:

- (1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See [Table 3](#).

**Table 3. MAX 7000B Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP (2)	49-Pin 0.8-mm Ultra FineLine BGA (3)	100- Pin TQFP	100-Pin FineLine BGA (4)	144- Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA (3)	208- Pin PQFP	256- Pin BGA	256-Pin FineLine BGA (4)
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B				41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B							120	141	176	212	212

**Notes:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) Contact Altera for up-to-date information on available device package options.
- (3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.
- (4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

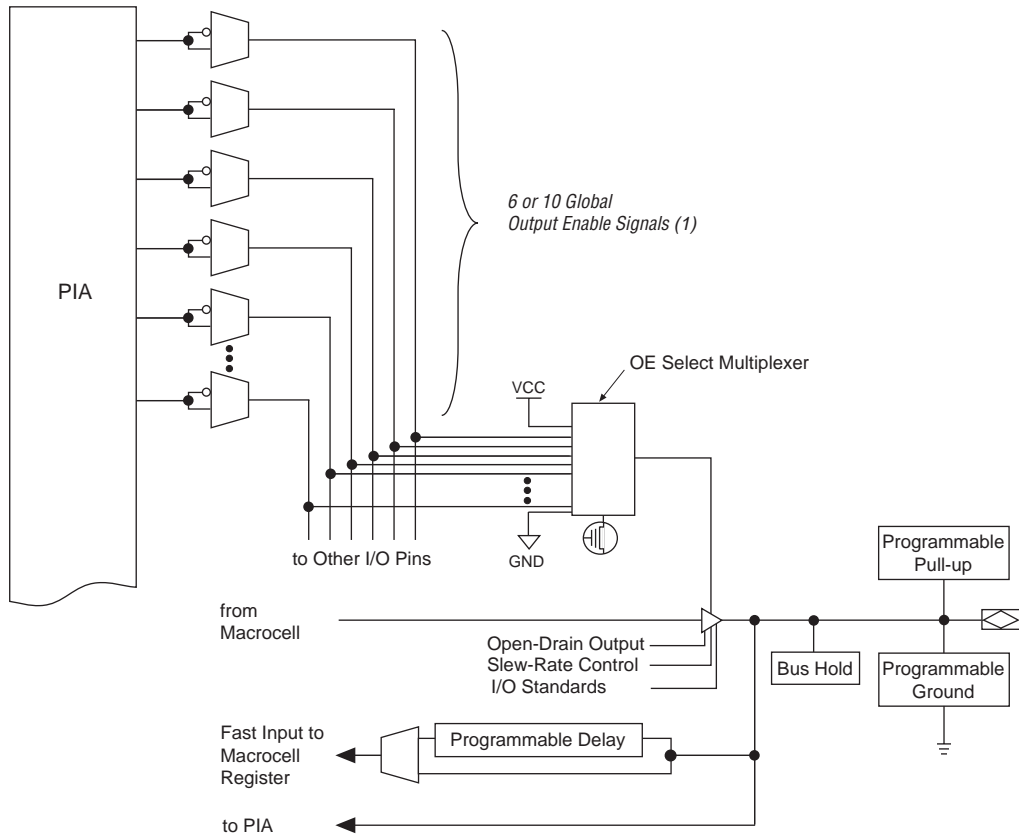
The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000B devices.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

**Figure 6. I/O Control Block of MAX 7000B Devices****Note:**

- (1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

The programming times described in [Tables 4 through 6](#) are associated with the worst-case method using the enhanced ISP algorithm.

**Table 4. MAX 7000B  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PPULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EMP7032B	2.12	70,000	0.002	18,000
EMP7064B	2.12	120,000	0.002	35,000
EMP7128B	2.12	222,000	0.002	69,000
EMP7256B	2.12	466,000	0.002	151,000
EMP7512B	2.12	914,000	0.002	300,000

[Tables 5 and 6](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 5. MAX 7000B In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	2.13	2.13	2.15	2.19	2.26	2.47	2.82	3.52	s
EMP7064B	2.13	2.14	2.18	2.24	2.36	2.72	3.32	4.52	s
EMP7128B	2.14	2.16	2.23	2.34	2.56	3.23	4.34	6.56	s
EMP7256B	2.17	2.21	2.35	2.58	3.05	4.45	6.78	11.44	s
EMP7512B	2.21	2.30	2.58	3.03	3.95	6.69	11.26	20.40	s

**Table 1. MAX 7000B Stand-Alone Verification Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EMP7064B	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EMP7128B	0.01	0.02	0.04	0.07	0.14	0.35	0.69	1.38	s
EMP7256B	0.02	0.03	0.08	0.15	0.30	0.76	1.51	3.02	s
EMP7512B	0.03	0.06	0.15	0.30	0.60	1.50	3.00	6.00	s

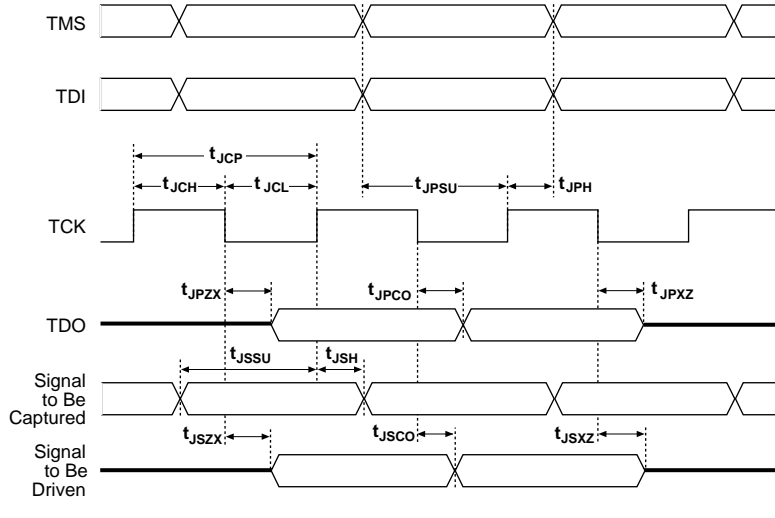
**Figure 8. MAX 7000B JTAG Waveforms**

Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

**Table 9. JTAG Timing Parameters & Values for MAX 7000B Devices***Note (1)*

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns

**Note:**(1) Timing parameters in this table apply to all  $V_{CCIO}$  levels.



## Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters.

## Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

The  $V_{CCIO}$  pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

## Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

MAX 7000B device I/O pins will not source or sink more than 300  $\mu$ A of DC current during power-up. All pins can be driven up to 4.1 V during hot-socketing.

## Design Security

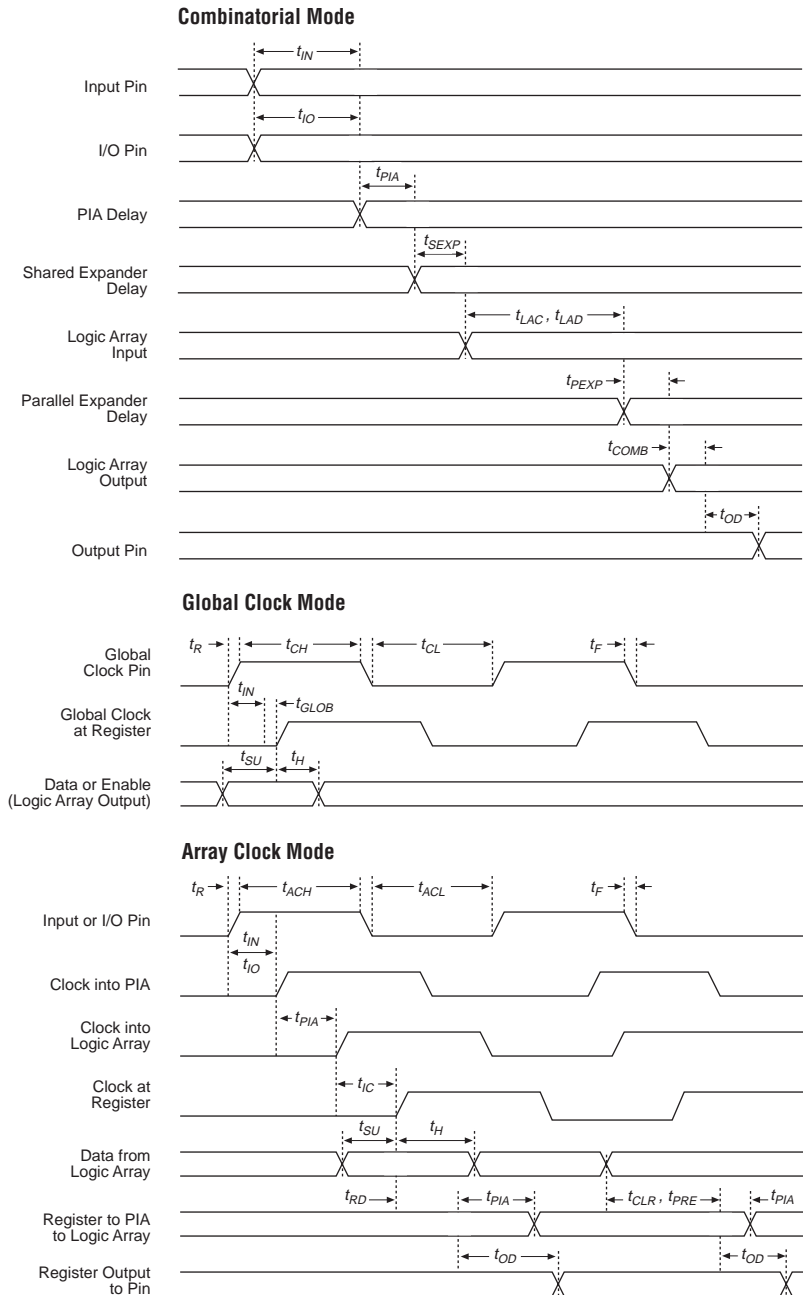
All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 11](#). Test patterns can be used and then erased during early stages of the production flow.

**Figure 14. MAX 7000B Switching Waveforms**

$t_R$  &  $t_F < 2$  ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 18 through 32 show MAX 7000B device timing parameters.

**Table 18. EPM7032B External Timing Parameters**

*Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.1		3.0		4.5		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		1.0		1.0		1.5		ns
t <sub>FH</sub>	Global clock hold time of fast input		1.0		1.0		1.0		ns
t <sub>FZHSU</sub>	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t <sub>FZHH</sub>	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t <sub>CH</sub>	Global clock high time		1.5		2.0		3.0		ns
t <sub>CL</sub>	Global clock low time		1.5		2.0		3.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	0.9		1.3		1.9		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		0.6		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t <sub>ACH</sub>	Array clock high time		1.5		2.0		3.0		ns
t <sub>ACL</sub>	Array clock low time		1.5		2.0		3.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

**Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays** *Notes (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3.5		-5.0		-7.5		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

**Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

**Table 25. EPM7128B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.6		0.8	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.6		0.8	ns
$t_{FIN}$	Fast input delay			1.3		2.9		3.7	ns
$t_{FIND}$	Programmable delay adder for fast input			1.0		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.8		3.8	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.8		1.0	ns
$t_{LAD}$	Logic array delay			1.6		2.9		3.8	ns
$t_{LAC}$	Logic control array delay			1.4		2.6		3.4	ns
$t_{IOE}$	Internal output enable delay			0.1		0.3		0.4	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.7		2.2	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.7		7.2	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.8		3.3		4.4	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.8		8.3		9.4	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		1.8		3.3		4.4	ns
$t_{SU}$	Register setup time		1.0		1.9		2.6		ns
$t_H$	Register hold time		0.4		0.8		1.1		ns
$t_{FSU}$	Register setup time of fast input		0.8		0.9		0.9		ns
$t_{FH}$	Register hold time of fast input		1.2		1.6		1.6		ns
$t_{RD}$	Register delay			0.5		1.1		1.4	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.4	ns
$t_{IC}$	Array clock delay			1.4		2.8		3.6	ns
$t_{EN}$	Register enable time			1.4		2.6		3.4	ns
$t_{GLOB}$	Global control delay			1.1		2.3		3.1	ns
$t_{PRE}$	Register preset time			1.0		1.9		2.6	ns
$t_{CLR}$	Register clear time			1.0		1.9		2.6	ns
$t_{PIA}$	PIA delay	(2)		1.0		2.0		2.8	ns
$t_{LPA}$	Low-power adder	(4)		1.5		2.8		3.8	ns

**Table 28. EPM7256B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.4		0.6		0.8	ns
$t_{IO}$	I/O input pad and buffer delay			0.4		0.6		0.8	ns
$t_{FIN}$	Fast input delay			1.5		2.5		3.1	ns
$t_{FIND}$	Programmable delay adder for fast input			1.5		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.3		3.0	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.6		0.8	ns
$t_{LAD}$	Logic array delay			1.7		2.5		3.3	ns
$t_{LAC}$	Logic control array delay			1.5		2.2		2.9	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.3	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.4		1.9	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.4		6.9	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.2		3.3		4.5	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		7.2		8.3		9.5	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		2.2		3.3		4.5	ns
$t_{SU}$	Register setup time		1.2		1.8		2.5		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.4		1.4		ns
$t_{RD}$	Register delay			0.7		1.0		1.3	ns
$t_{COMB}$	Combinatorial delay			0.3		0.4		0.5	ns
$t_{IC}$	Array clock delay			1.5		2.3		3.0	ns
$t_{EN}$	Register enable time			1.5		2.2		2.9	ns
$t_{GLOB}$	Global control delay			1.3		2.1		2.7	ns
$t_{PRE}$	Register preset time			1.0		1.6		2.1	ns
$t_{CLR}$	Register clear time			1.0		1.6		2.1	ns
$t_{PIA}$	PIA delay	(2)		1.7		2.6		3.3	ns
$t_{LPA}$	Low-power adder	(4)		2.0		3.0		4.0	ns



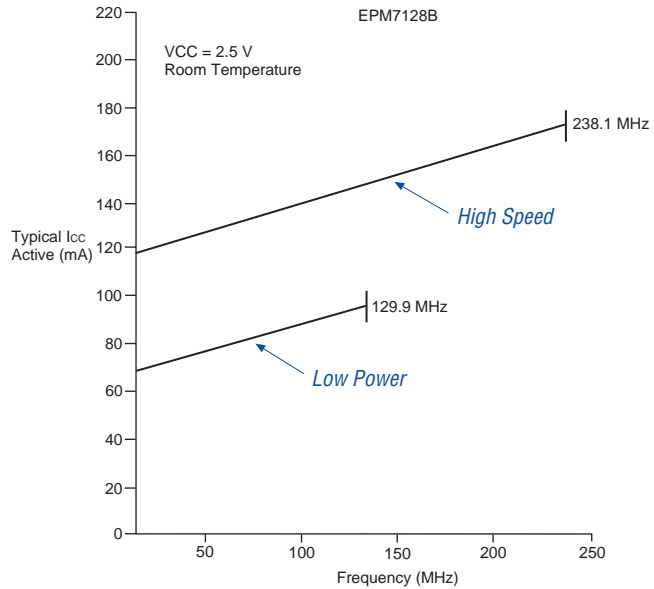
**Table 31. EPM7512B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.3		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.3		0.5	ns
$t_{FIN}$	Fast input delay			2.2		3.2		4.0	ns
$t_{FIND}$	Programmable delay adder for fast input			1.5		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.1		2.7	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5		0.7	ns
$t_{LAD}$	Logic array delay			1.7		2.3		3.0	ns
$t_{LAC}$	Logic control array delay			1.5		2.0		2.6	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.2	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.6	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.8		3.8		5.0	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		7.8		8.8		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		2.8		3.8		5.0	ns
$t_{SU}$	Register setup time		1.5		2.0		2.6		ns
$t_H$	Register hold time		0.4		0.5		0.7		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.4		1.4		ns
$t_{RD}$	Register delay			0.5		0.7		1.0	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.4	ns
$t_{IC}$	Array clock delay			1.8		2.4		3.1	ns
$t_{EN}$	Register enable time			1.5		2.0		2.6	ns
$t_{GLOB}$	Global control delay			2.0		2.8		3.6	ns
$t_{PRE}$	Register preset time			1.0		1.4		1.9	ns
$t_{CLR}$	Register clear time			1.0		1.4		1.9	ns
$t_{PIA}$	PIA delay	(2)		2.4		3.4		4.5	ns
$t_{LPA}$	Low-power adder	(4)		2.0		2.7		3.6	ns

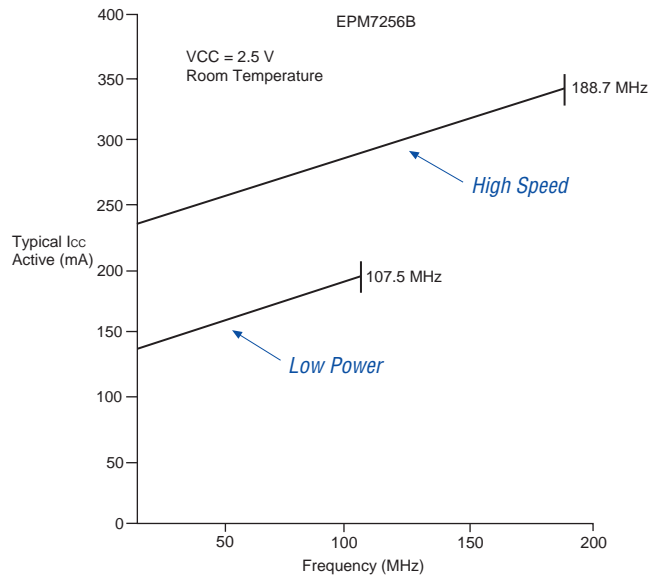
**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.5		0.7	ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.3	ns
	All outputs		0.2		0.3		0.3	ns
1.8 V TTL/CMOS	Input to PIA		0.7		1.0		1.3	ns
	Input to global clock and clear		0.6		0.8		1.0	ns
	Input to fast input register		0.5		0.6		0.8	ns
	All outputs		1.3		1.8		2.3	ns
SSTL-2 Class I	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.5		3.3	ns
	Input to global clock and clear		1.9		2.6		3.5	ns
	Input to fast input register		1.8		2.5		3.3	ns
	All outputs		0.0		0.0		0.0	ns

**Figure 17.  $I_{CC}$  vs. Frequency for EPM7128B Devices**



**Figure 18.  $I_{CC}$  vs. Frequency for EPM7256B Devices**



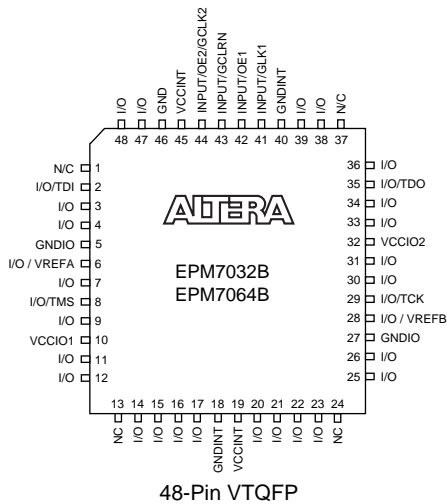
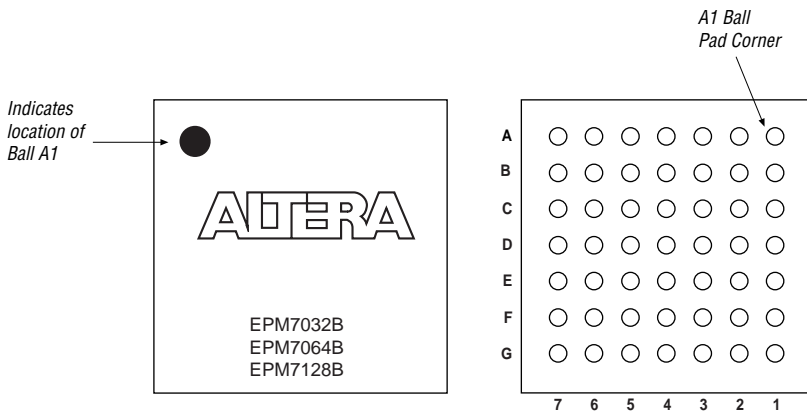
**Figure 21. 48-Pin VTQFP Package Pin-Out Diagram***Package outlines not drawn to scale.***Figure 22. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram***Package outline not drawn to scale.*

Figure 25. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

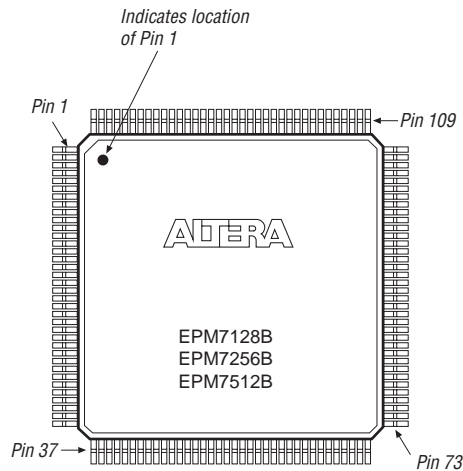


Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram

Package outline not drawn to scale.

