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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256bfc100-10

Table 3. MAX 7000B Maximum User I/O Pins Note (1)

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP (2)	49-Pin 0.8-mm Ultra FineLine BGA (3)	100-Pin TQFP	100-Pin FineLine BGA (4)	144-Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA (3)	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA (4)
EPM7032B	*36*	*36*	*36*								
EPM704B	*36*	*36*	*40*	*41*							
EPM712B				*41*	*64*	*64*	*100*	*100*		*100*	
EPM725B					*64*		*120*	*141*	*144*	*164*	
EPM7512B							*120*	*141*	*172*	*212*	*212*

Notes:

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) Contact Altera for up-to-date information on available device package options.

(3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

(4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

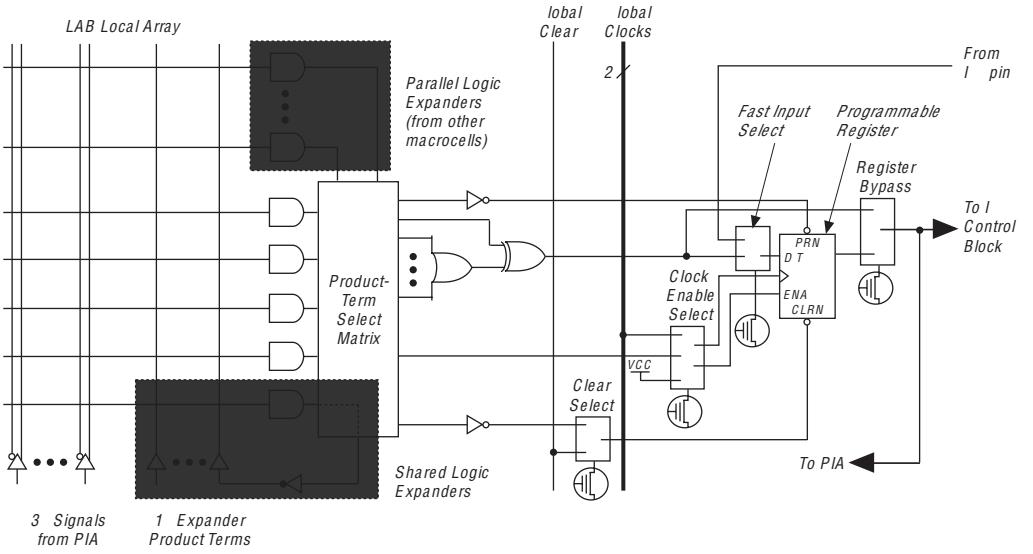
MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

Figure 2. MAX 7000B Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

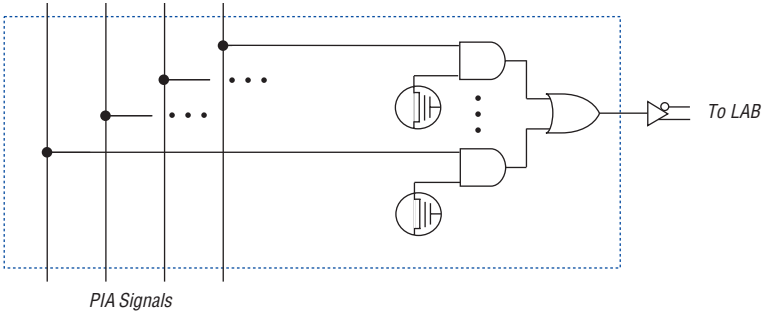
Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 5. MAX 7000B PIA Routing

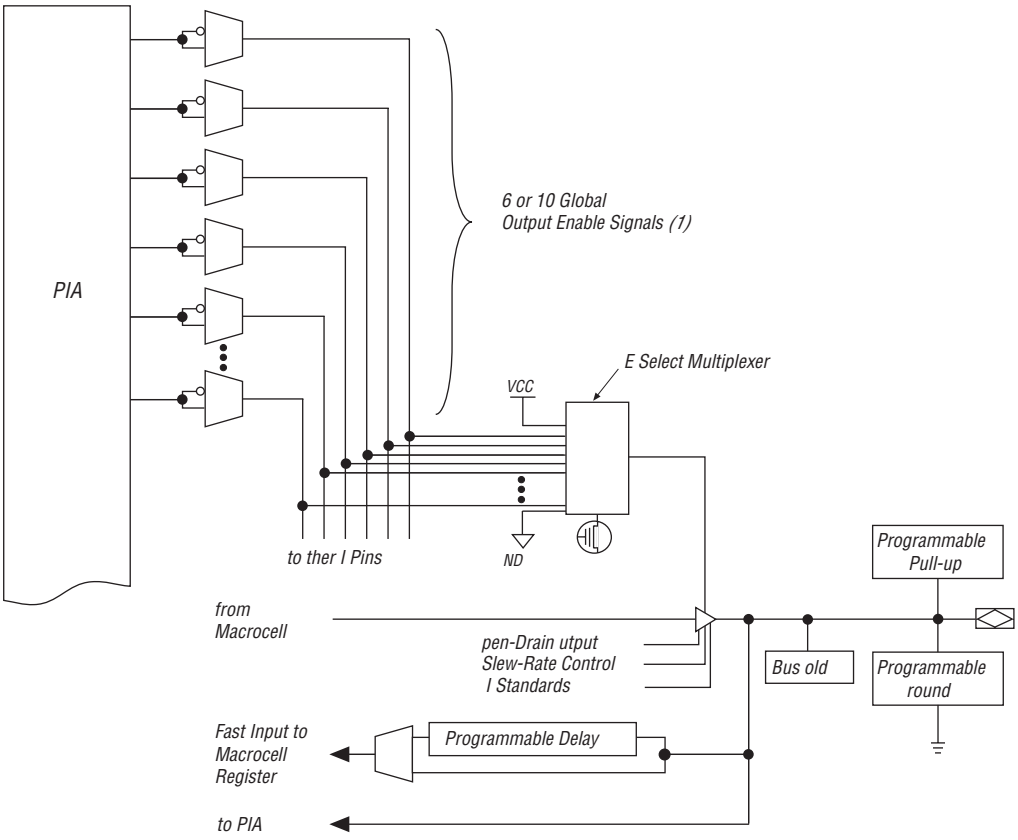


Unlike the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000B Devices



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000B device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Figure 8. MAX 7000B JTAG Waveforms

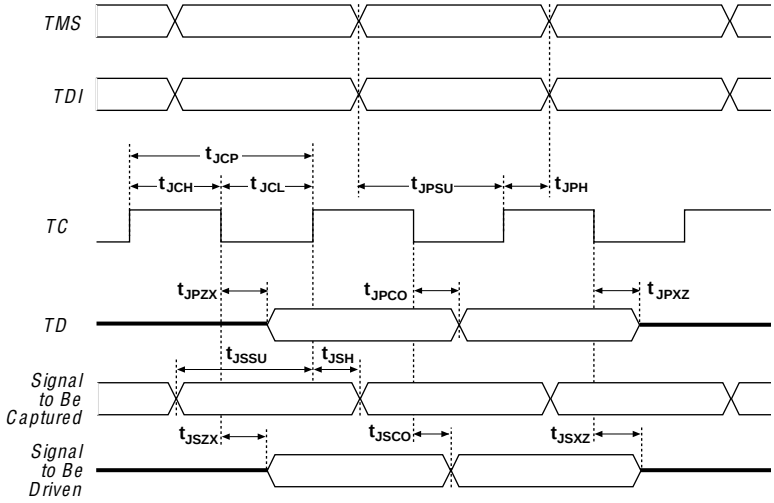


Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

Table 9. JTAG Timing Parameters & Values for MAX 7000B Devices *Note (1)*

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK *clock period*	100		ns
t_{JCH}	TCK *clock high time*	50		ns
t_{JCL}	TCK *clock low time*	50		ns
t_{JPSU}	*TA port setup time*	20		ns
t_{JPH}	*TA port hold time*	45		ns
t_{JPCO}	*TA port clock to output*		25	ns
t_{JPZX}	*TA port high impedance to valid output*		25	ns
t_{JPXZ}	*TA port valid output to high impedance*		25	ns
t_{JSSU}	*Capture register setup time*	20		ns
t_{JSH}	*Capture register hold time*	45		ns
t_{JSCO}	*Update register clock to output*		25	ns
t_{JSZX}	*Update register high impedance to valid output*		25	ns
t_{JSXZ}	*Update register valid output to high impedance*		25	ns

Note:
(1) Timing parameters in this table apply to all V_{CCIO} levels.

Table 10. MAX 7000B MultiVolt I/O Support								
V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.	v	v	v		v			
2.5	v	v	v			v		
3.3	v	v	v				v	v

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

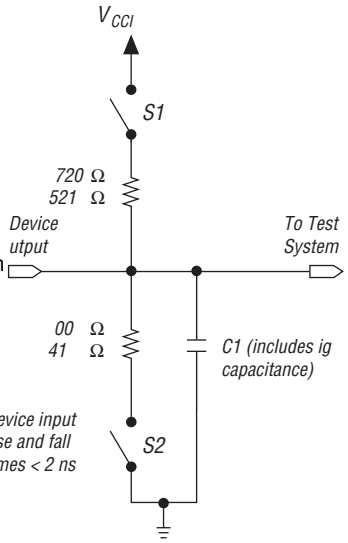
The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Figure 11. MAX 7000B AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

Table 14. MAX 7000B Device Absolute Maximum Ratings Note (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage		0.5	3.	V
V_{CCI}	Supply voltage		0.5	3.	V
V_I	DC input voltage	(2)	2.0	4.	V
I_{UT}	DC output current, per pin		33	50	mA
T_{ST}	Storage temperature	No bias	5	150	C
T_A	Ambient temperature	Under bias	5	135	C
T	unction temperature	Under bias	5	135	C

Figure 12 shows the typical output drive characteristics of MAX 7000B devices.

Figure 12. Output Drive Characteristics of MAX 7000B Devices

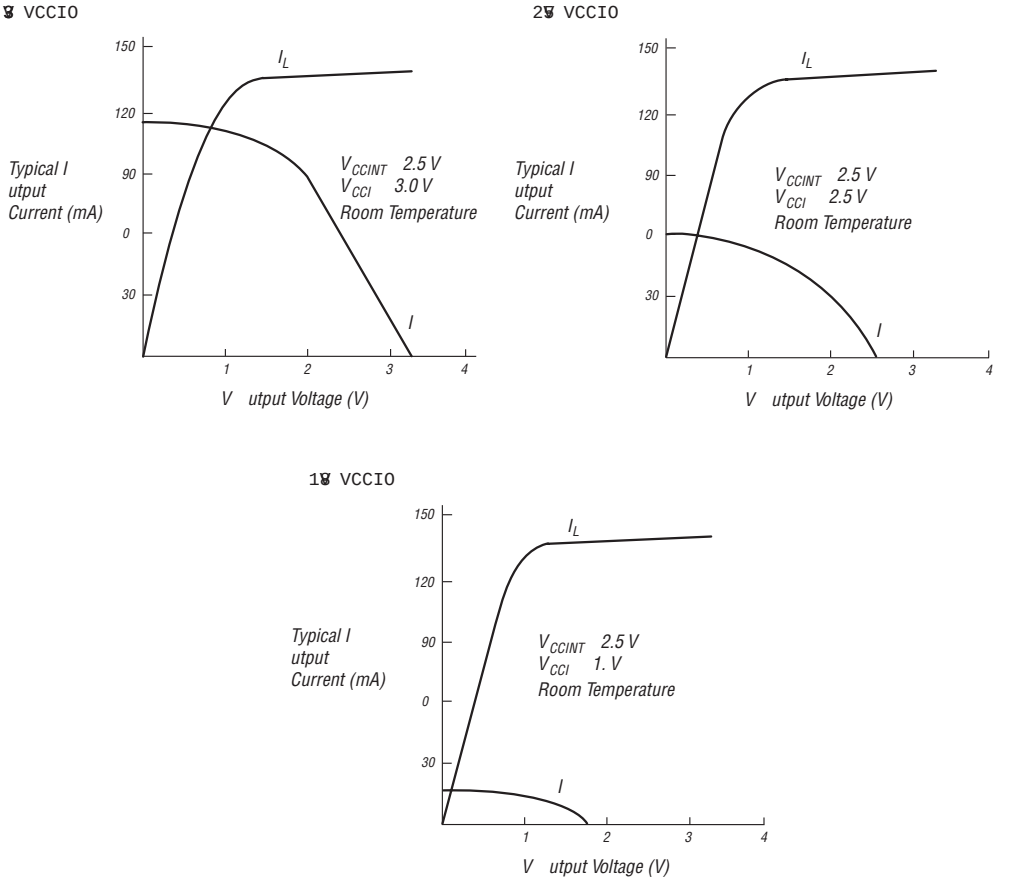


Table 19. EPM7032B Internal Timing Parameters Notes (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	utput buffer and pad delay slow slew rate off V_{CCI} 3.3 V	C1 35 pF		0.9		1.2		1.	ns
t_{OD3}	utput buffer and pad delay slow slew rate on V_{CCI} 2.5 V or 3.3 V	C1 35 pF		5.9		.2		.	ns
t_{ZX1}	utput buffer enable delay slow slew rate off V_{CCI} 3.3 V	C1 35 pF		1.		2.2		3.4	ns
t_{ZX3}	utput buffer enable delay slow slew rate on V_{CCI} 2.5 V or 3.3 V	C1 35 pF		.		7.2		.4	ns
t_{XZ}	utput buffer disable delay	C1 5 pF		1.		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.		ns
t_{H}	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.		0.		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.		2.	ns
t_{EN}	Register enable time			1.2		1.7		2.	ns
t_{GLOB}	lobal control delay			0.7		1.1		1.	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	(2)		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	(4)		1.5		2.1		3.2	ns

Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA	0.0		0.0		0.0		ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA	0.3		0.4		0.5		ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA	0.5		0.7		1.1		ns
	Input to global clock and clear		0.5		0.7		1.1	ns
	Input to fast input register		0.4		0.6		0.9	ns
	All outputs		1.2		1.7		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.9	ns
	Input to global clock and clear		1.2		1.7		2.9	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.9	ns
	Input to global clock and clear		1.2		1.7		2.9	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.1		0.1		0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.7		2.9	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.6		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.7		2.9	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.6		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL	Input to PIA	1.5		2.3		3.4		ns
	Input to global clock and clear		1.5		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	*Input to PIA*		*0.0*		*0.0*		*0.0*	*ns*
	Input to global clock and clear		*0.0*		*0.0*		*0.0*	*ns*
	Input to fast input register		*0.0*		*0.0*		*0.0*	*ns*
	All outputs		*0.0*		*0.0*		*0.0*	*ns*

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	*Input to PIA*		*0.0*		*0.0*		*0.0*	*ns*
	Input to global clock and clear		*0.0*		*0.0*		*0.0*	*ns*
	Input to fast input register		*0.0*		*0.0*		*0.0*	*ns*
	All outputs		*0.0*		*0.0*		*0.0*	*ns*

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 31. EPM7512B Internal Timing Parameters Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.3		0.5	ns
t_{IO}	I input pad and buffer delay			0.3		0.3		0.5	ns
t_{FIN}	Fast input delay			2.2		3.2		4.0	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		2.7	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.7	ns
t_{LAD}	Logic array delay			1.7		2.3		3.0	ns
t_{LAC}	Logic control array delay			1.5		2.0		2.	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.2	ns
t_{OD1}	utput buffer and pad delay slow slew rate off V_{CCI} 3.3 V	C1 35 pF		0.9		1.2		1.	ns
t_{OD3}	utput buffer and pad delay slow slew rate on V_{CCI} 2.5 V or 3.3 V	C1 35 pF		5.9		.2		.	ns
t_{ZX1}	utput buffer enable delay slow slew rate off V_{CCI} 3.3 V	C1 35 pF		2.		3.		5.0	ns
t_{ZX3}	utput buffer enable delay slow slew rate on V_{CCI} 2.5 V or 3.3 V	C1 35 pF		7.		.		10.0	ns
t_{XZ}	utput buffer disable delay	C1 5 pF		2.		3.		5.0	ns
t_{SU}	Register setup time		1.5		2.0		2.		ns
t_{H}	Register hold time		0.4		0.5		0.7		ns
t_{FSU}	Register setup time of fast input		0.		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.5		0.7		1.0	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.		2.4		3.1	ns
t_{EN}	Register enable time			1.5		2.0		2.	ns
t_{GLOB}	lobal control delay			2.0		2.		3.	ns
t_{PRE}	Register preset time			1.0		1.4		1.9	ns
t_{CLR}	Register clear time			1.0		1.4		1.9	ns
t_{PIA}	PIA delay	(2)		2.4		3.4		4.5	ns
t_{LPA}	Low-power adder	(4)		2.0		2.7		3.	ns

Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

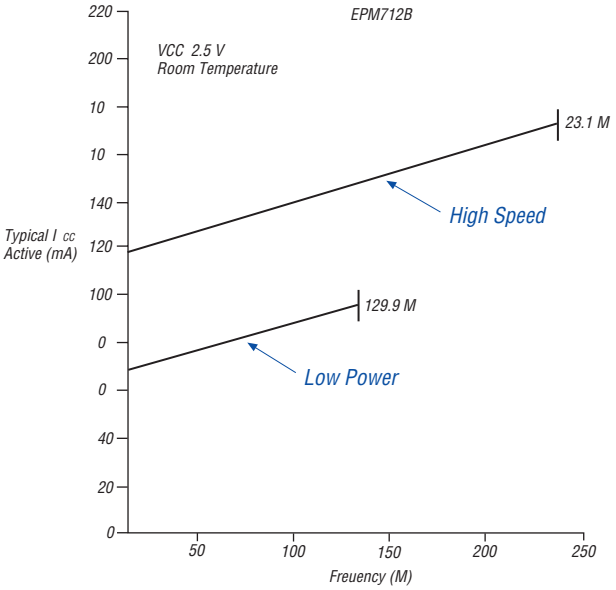
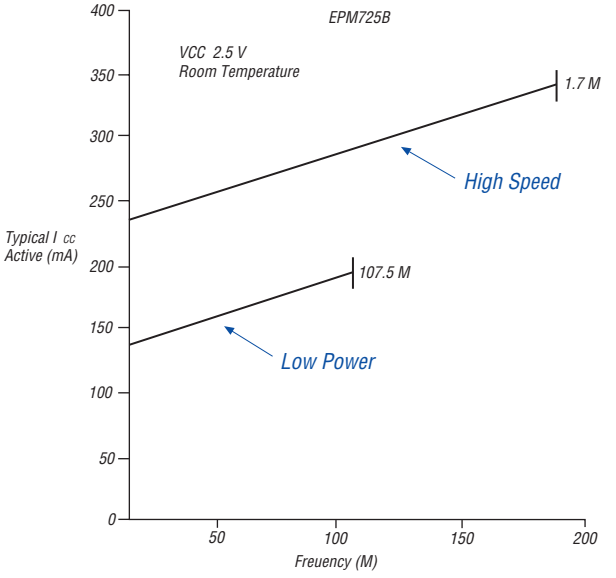


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices



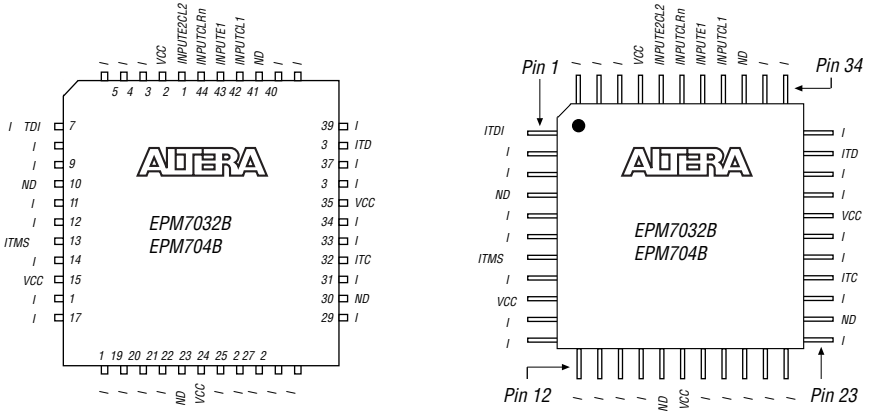
Device Pin-Outs

See the Altera web site (*http://www.altera.com*) or the Altera Digital Library for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TFP

Figure 23. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

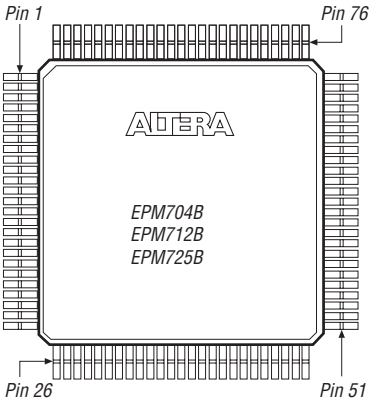


Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

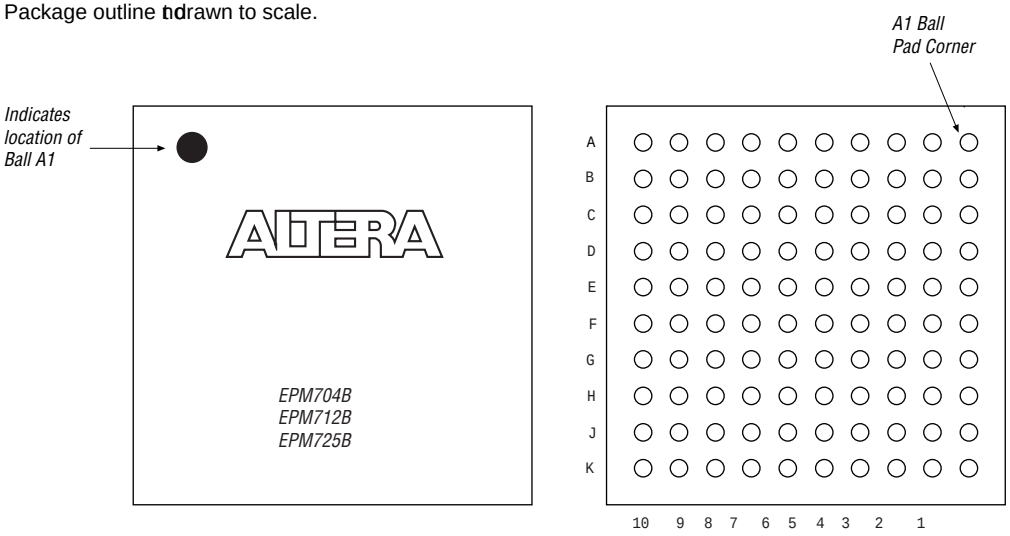
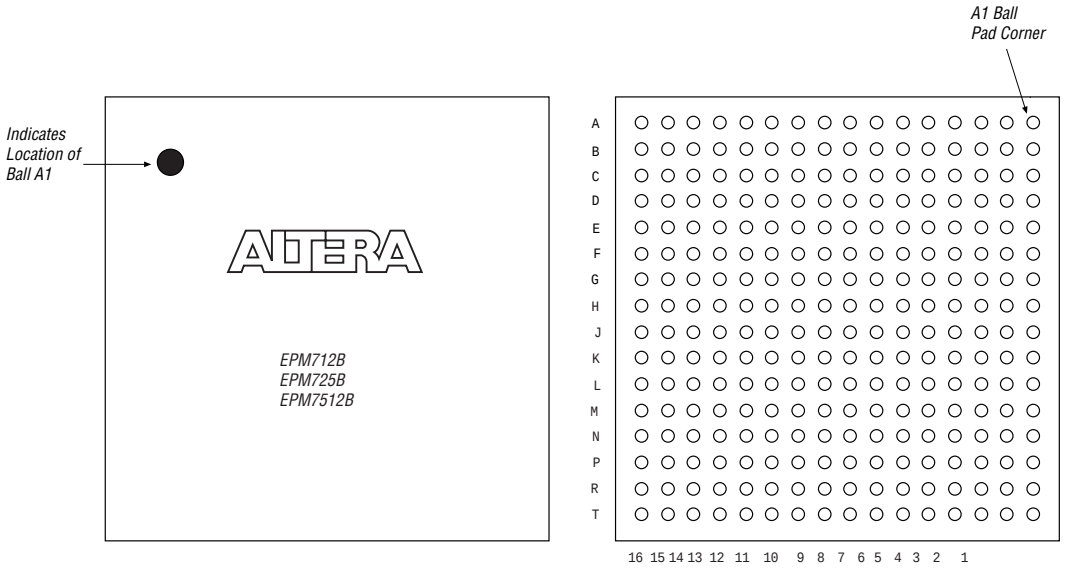


Figure 29. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.5 supersedes information published in previous versions.

Version 3.5

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.5:

- Updated Figure 28.

Version 3.4

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.4:

- Updated text in the "Power Sequencing & Hot-Socketing" section.