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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	141
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-UBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256bfc169-10

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000B devices. As shown in [Figure 1](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figure 2](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Expander Product Terms

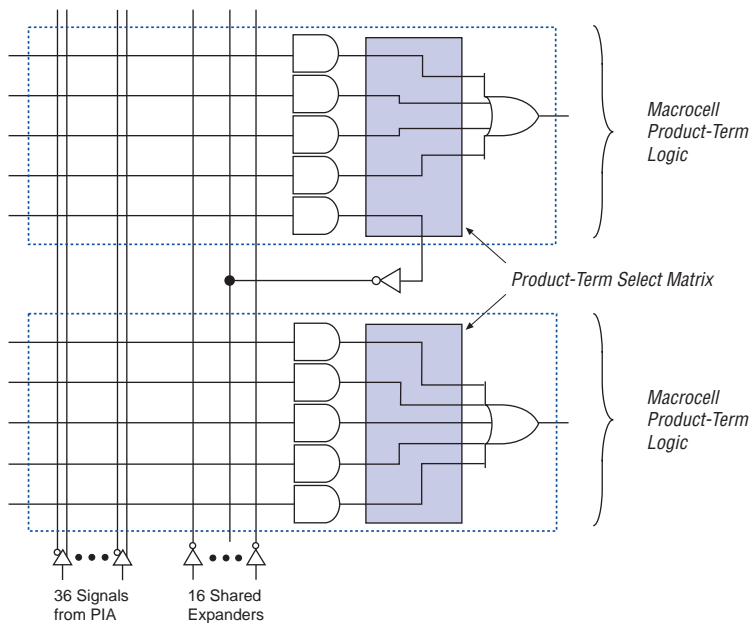
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. [Figure 3](#) shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000B Shareable Expanders

Shareable expanders can be shared by any or all macrocells in a LAB.



In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam language, see [Application Note 88 \(Using the Jam Language for ISP & ICR via an Embedded Processor\)](#) and [Application Note 122 \(Using STAPL for ISP & ICR via an Embedded Processor\)](#).

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. [Tables 7 and 8](#) show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

Table 7. MAX 7000B Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

Table 8. 32-Bit MAX 7000B Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

Notes:

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG boundary-scan testing.

[Figure 8](#) shows the timing information for the JTAG signals.

Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters.

Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCIO} pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the V_{CCIO} pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

MAX 7000B device I/O pins will not source or sink more than 300 μ A of DC current during power-up. All pins can be driven up to 4.1 V during hot-socketing.

Design Security

All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 11](#). Test patterns can be used and then erased during early stages of the production flow.

Table 15. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(10)	2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	(3)	-0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	°C
		For industrial use (11)	-40	85	°C
T_J	Junction temperature	For commercial use	0	90	°C
		For industrial use (11)	-40	105	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 19. EPM7032B Internal Timing Parameters *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_H	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	(2)		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	(4)		1.5		2.1		3.2	ns

Table 21. EPM7064B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{SU}	Global clock setup time	(2)	2.1		3.0		4.5		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t _{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t _{CH}	Global clock high time		1.5		2.0		3.0		ns
t _{CL}	Global clock low time		1.5		2.0		3.0		ns
t _{ASU}	Array clock setup time	(2)	0.9		1.3		1.9		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.6		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t _{ACH}	Array clock high time		1.5		2.0		3.0		ns
t _{ACL}	Array clock low time		1.5		2.0		3.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t _{CNT}	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t _{ACNT}	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.6		0.8	ns
	Input to global clock and clear		0.3		0.6		0.8	ns
	Input to fast input register		0.2		0.4		0.5	ns
	All outputs		0.2		0.4		0.5	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.9		1.3	ns
	Input to global clock and clear		0.5		0.9		1.3	ns
	Input to fast input register		0.4		0.8		1.0	ns
	All outputs		1.2		2.3		3.0	ns
SSTL-2 Class I	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		−0.1		−0.2		−0.3	ns
SSTL-3 Class I	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.7		3.2		4.3	ns
	Input to global clock and clear		1.7		3.2		4.3	ns
	Input to fast input register		1.6		3.0		4.0	ns
	All outputs		0.0		0.0		0.0	ns

Table 27. EPM7256B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t _{SU}	Global clock setup time	(2)	3.3		4.8		6.6		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t _{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.4		2.0		2.8		ns
t _{AH}	Array clock hold time	(2)	0.4		0.8		1.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	5.2	1.0	7.9	1.0	10.5	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		5.3		7.9		10.6	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	188.7		126.6		94.3		MHz
t _{ACNT}	Minimum array clock period	(2)		5.3		7.9		10.6	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	188.7		126.6		94.3		MHz

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.5		0.7	ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.3	ns
	All outputs		0.2		0.3		0.3	ns
1.8 V TTL/CMOS	Input to PIA		0.7		1.0		1.3	ns
	Input to global clock and clear		0.6		0.8		1.0	ns
	Input to fast input register		0.5		0.6		0.8	ns
	All outputs		1.3		1.8		2.3	ns
SSTL-2 Class I	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.5		3.3	ns
	Input to global clock and clear		1.9		2.6		3.5	ns
	Input to fast input register		1.8		2.5		3.3	ns
	All outputs		0.0		0.0		0.0	ns

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} , in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

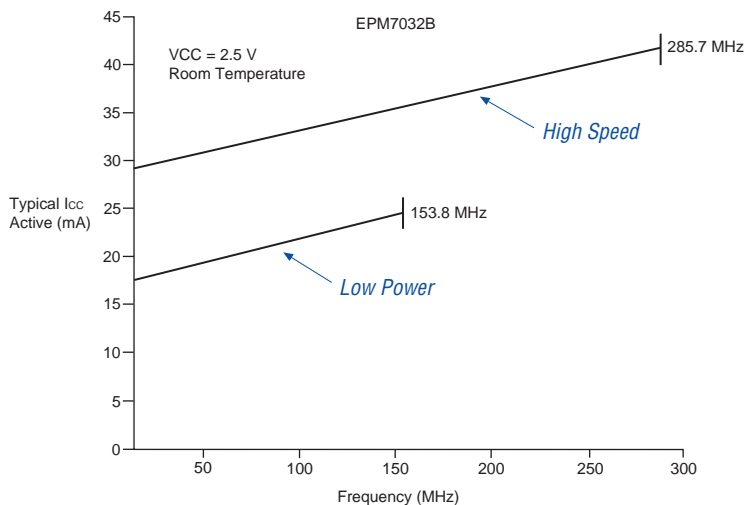
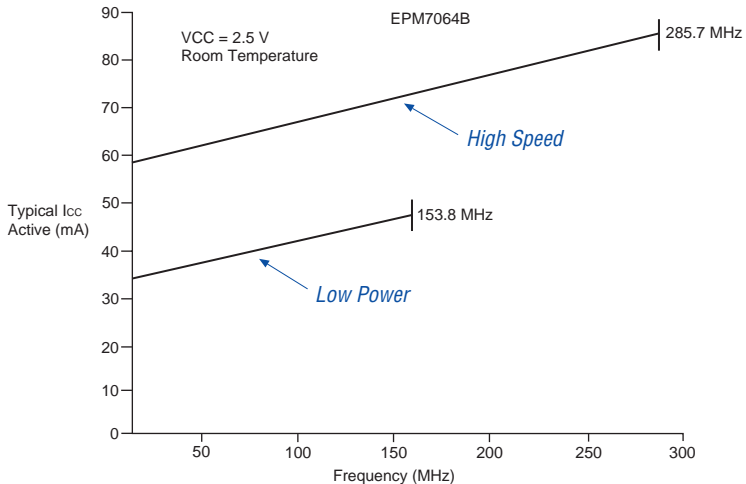
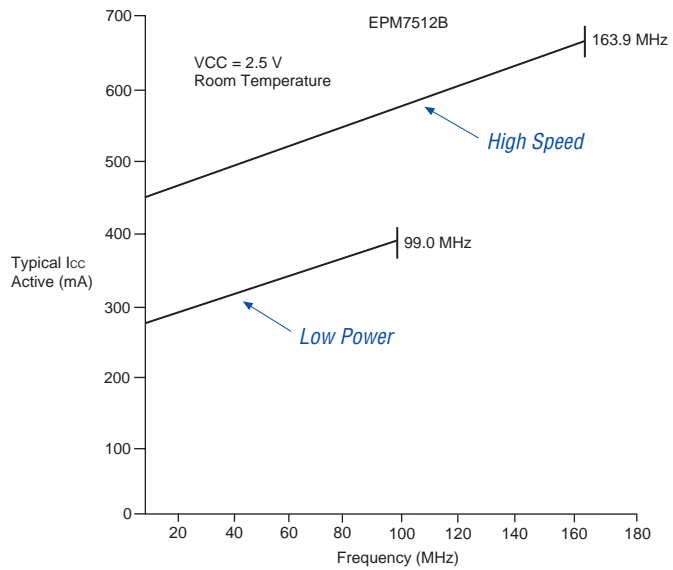
Figure 15. I_{CC} vs. Frequency for EPM7032B Devices**Figure 16. I_{CC} vs. Frequency for EPM7064B Devices**

Figure 19. I_{CC} vs. Frequency for EPM7512B Devices

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.

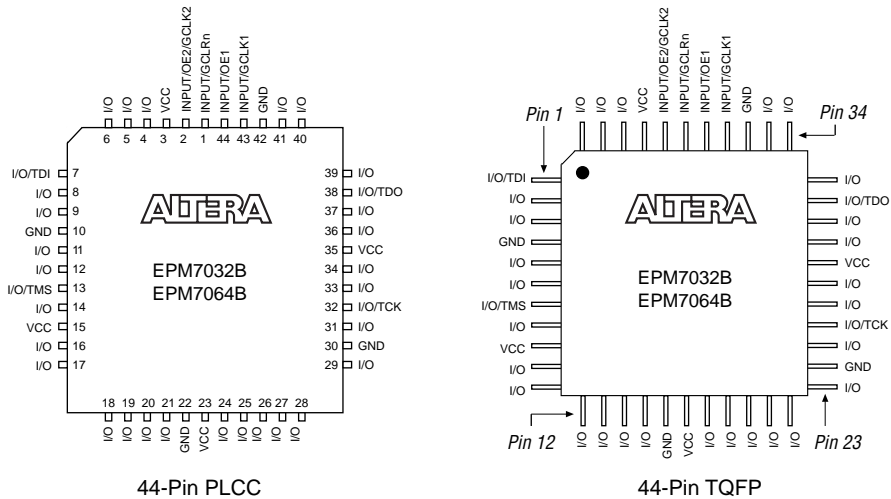
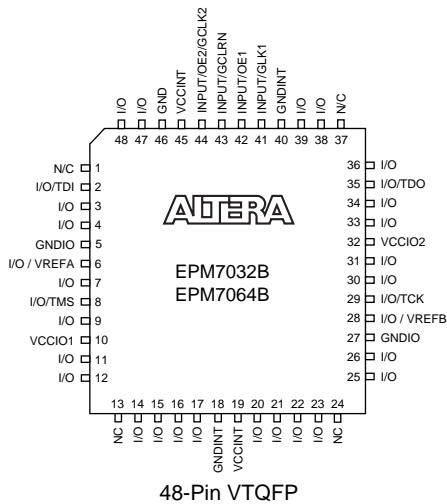


Figure 21. 48-Pin VTQFP Package Pin-Out Diagram*Package outlines not drawn to scale.***Figure 22. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram***Package outline not drawn to scale.*