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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	141
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-UBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256bfc169-5

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See Table 2.

Table 2. MAX 7000B Speed Grades *Note (1)*

Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

Notes:
(1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See Table 3.

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

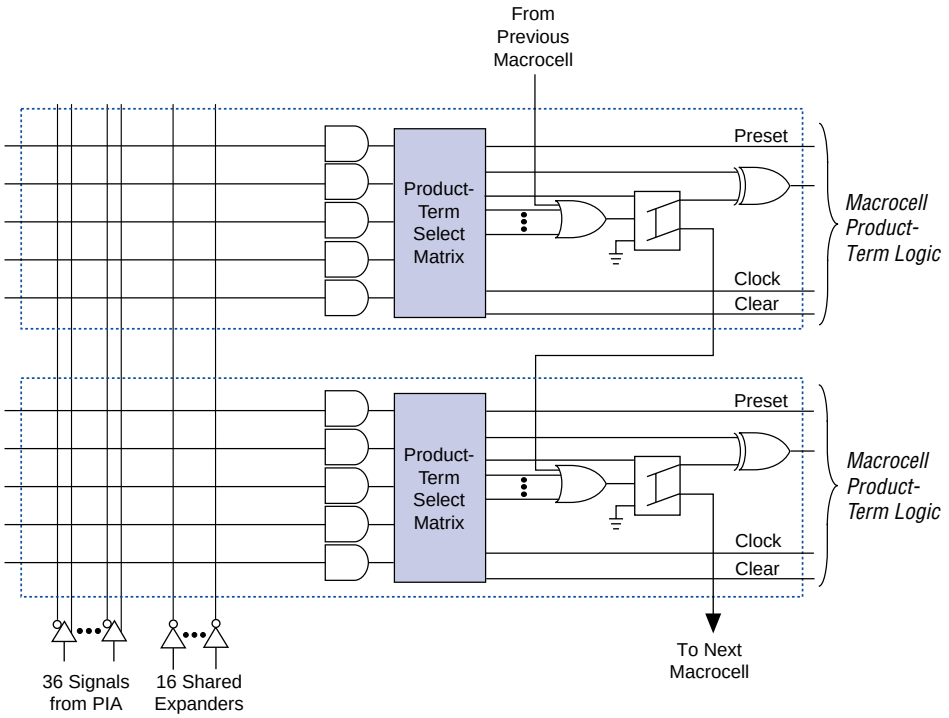
Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Figure 4. MAX 7000B Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. Tables 7 and 8 show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

Table 7. MAX 7000B Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

Table 8. 32-Bit MAX 7000B Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG boundary-scan testing.

Figure 8 shows the timing information for the JTAG signals.

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Programmable Pull-Up Resistor

Each MAX 7000B device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 50 k¾) weakly holds the output to V_{CCIO} level.

Bus Hold

Each MAX 7000B device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signals is present, the bus-hold feature can eliminate the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. The propagation delays through the input and output buffers in MAX 7000B devices are not affected by whether the bus-hold feature is enabled or disabled.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (R_{BH}) of approximately 8.5 k¾. Table 12 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each VCCIO voltage level.

Table 12. Bus Hold Parameters

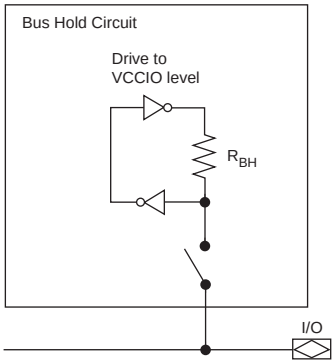
Parameter	Conditions	VCCIO Level						Units
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (max)	30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (min)	–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–295		–435		–680	µA

The bus-hold circuitry is active only during user operation. At power-up, the bus-hold circuit initializes its initial hold value as V_{CC} approaches the recommended operation conditions. When transitioning from ISP to User Mode with bus hold enabled, the bus-hold circuit captures the value present on the pin at the end of programming.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the ***PCI Local Bus Specification Revision 2.2*** except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications

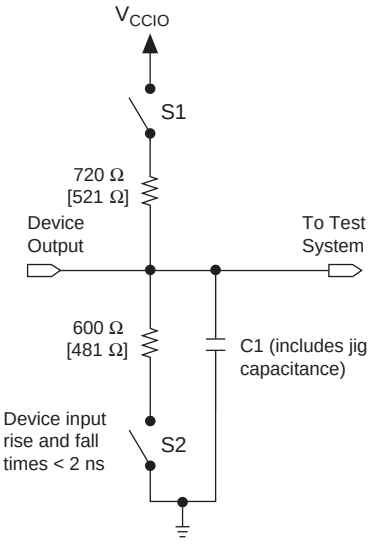
Device	Specification	
	33-MHz PCI	66-MHz PCI
EPM7032B	All speed grades	-3
EPM7064B	All speed grades	-3
EPM7128B	All speed grades	-4
EPM7256B	All speed grades	-5 *(1)*
EPM7512B	All speed grades	-5 *(1)*

Note:

(1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

Figure 11. MAX 7000B AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

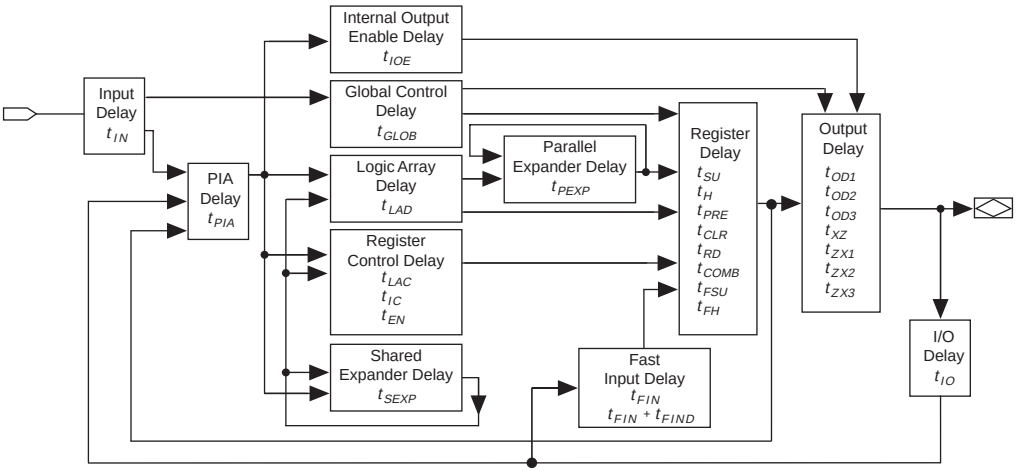
Table 14. MAX 7000B Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage		–0.5	3.6	V
V_{CCIO}	Supply voltage		–0.5	3.6	V
V_I	DC input voltage	*(2)*	–2.0	4.6	V
I_{OUT}	DC output current, per pin		–33	50	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias	–65	135	° C

Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Figure 14. MAX 7000B Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

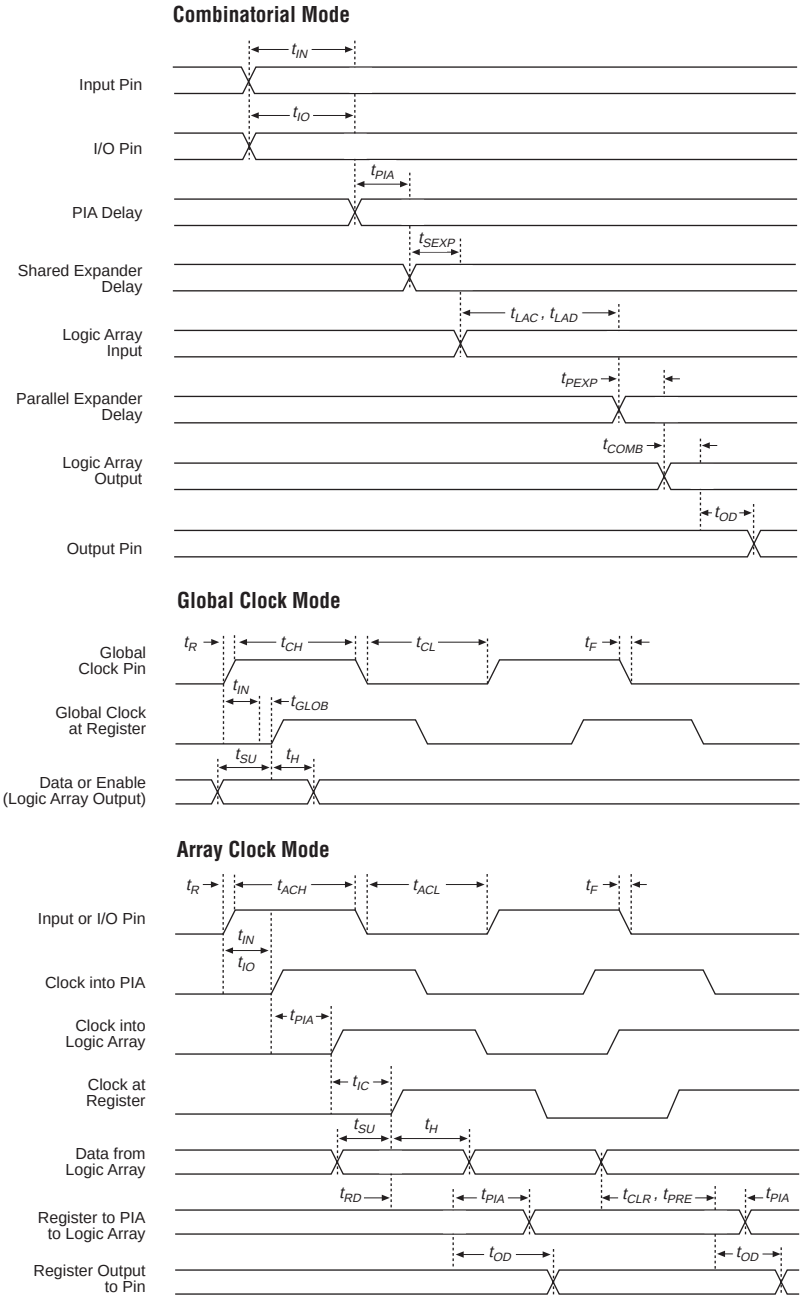


Table 19. EPM7032B Internal Timing Parameters *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_{H}	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	*(2)*		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.1		3.2	ns

Table 21. EPM7064B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(2)*	2.1		3.0		4.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.9		1.3		1.9		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	3.6	1.0	5.1	1.0	7.6	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(2)*		3.3		4.7		7.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		3.3		4.7		7.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz

Table 24. EPM7128B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	2.5		4.5		6.1		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.7	1.0	7.5	ns
t_{CH}	Global clock high time		1.5		3.0		4.0		ns
t_{CL}	Global clock low time		1.5		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.2		2.0		2.8		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.7		0.9		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.1	1.0	8.2	1.0	10.8	ns
t_{ACH}	Array clock high time		1.5		3.0		4.0		ns
t_{ACL}	Array clock low time		1.5		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.1		7.9		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	243.9		126.6		94.3		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.1		7.9		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	243.9		126.6		94.3		MHz

Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 27. EPM7256B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	3.3		4.8		6.6		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.4		2.0		2.8		ns
t_{AH}	Array clock hold time	*(2)*	0.4		0.8		1.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.2	1.0	7.9	1.0	10.5	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.3		7.9		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	188.7		126.6		94.3		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.3		7.9		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	188.7		126.6		94.3		MHz

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 33

Table 33. MAX 7000B I_{CC} Equation Constants

Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

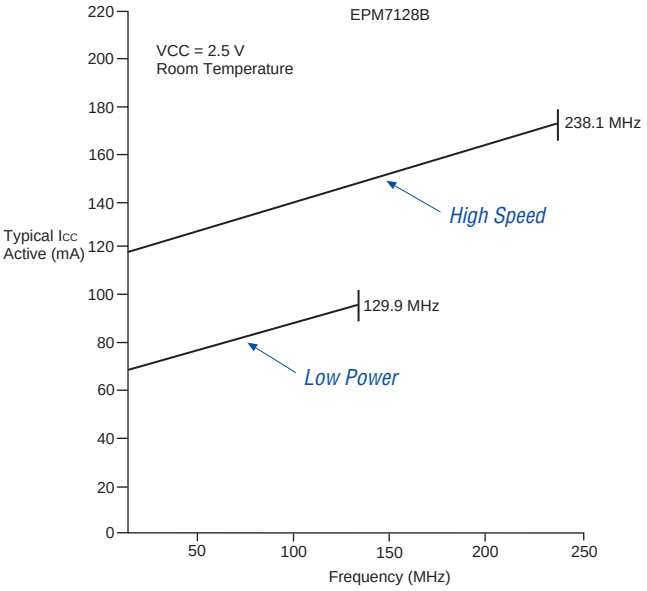
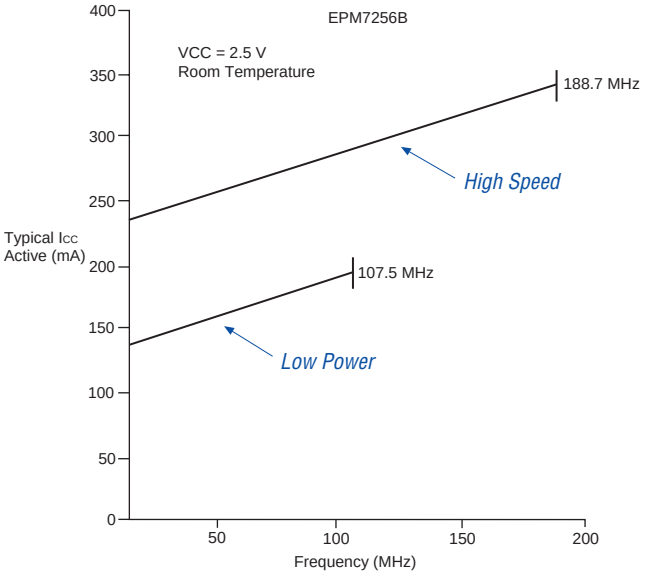


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices



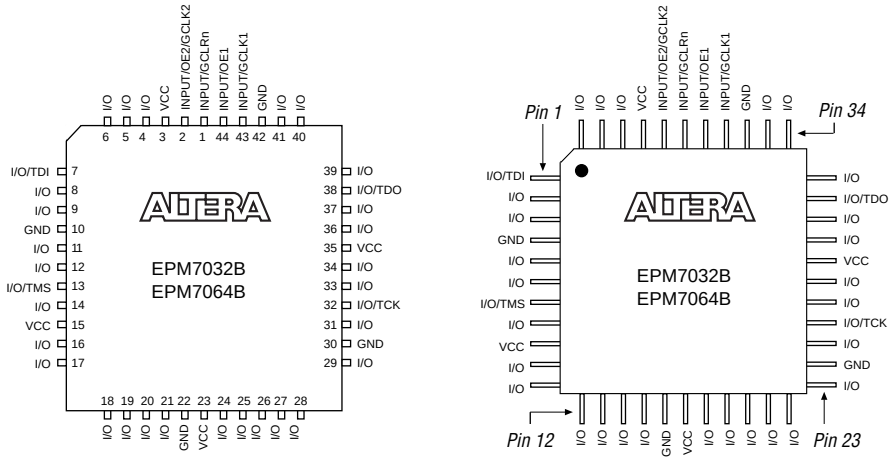
Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TQFP

Figure 27. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.