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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	141
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-UBGA (11x11)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7256bfc169-7">https://www.e-xfl.com/product-detail/intel/epm7256bfc169-7</a>

**Table 3. MAX 7000B Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP (2)	49-Pin 0.8-mm Ultra FineLine BGA (3)	100- Pin TQFP	100-Pin FineLine BGA (4)	144- Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA (3)	208- Pin PQFP	256- Pin BGA	256-Pin FineLine BGA (4)
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B				41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B							120	141	176	212	212

**Notes:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) Contact Altera for up-to-date information on available device package options.
- (3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.
- (4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.

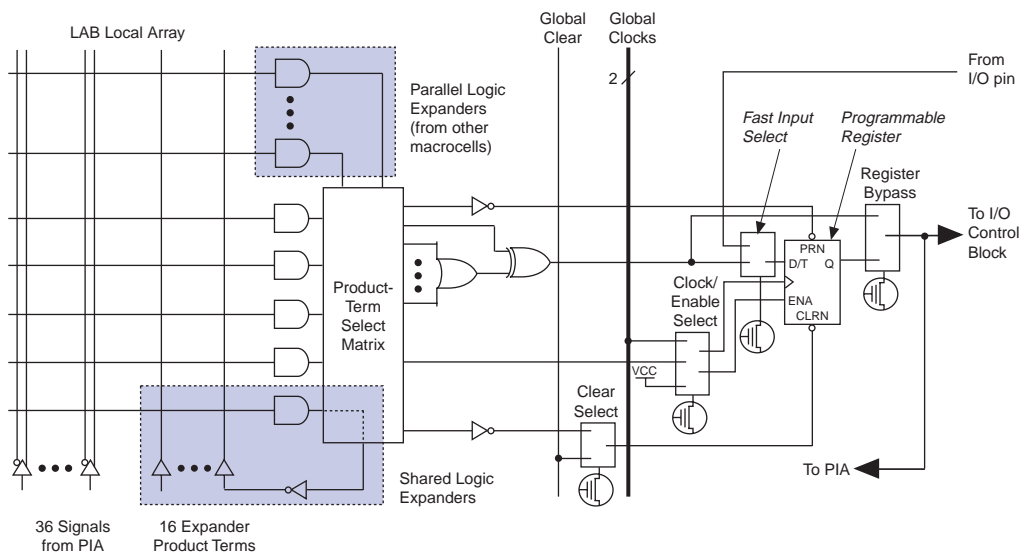
MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

## Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

**Figure 2. MAX 7000B Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

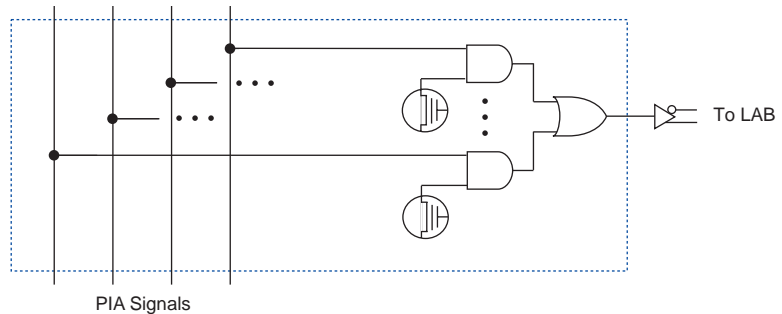
- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

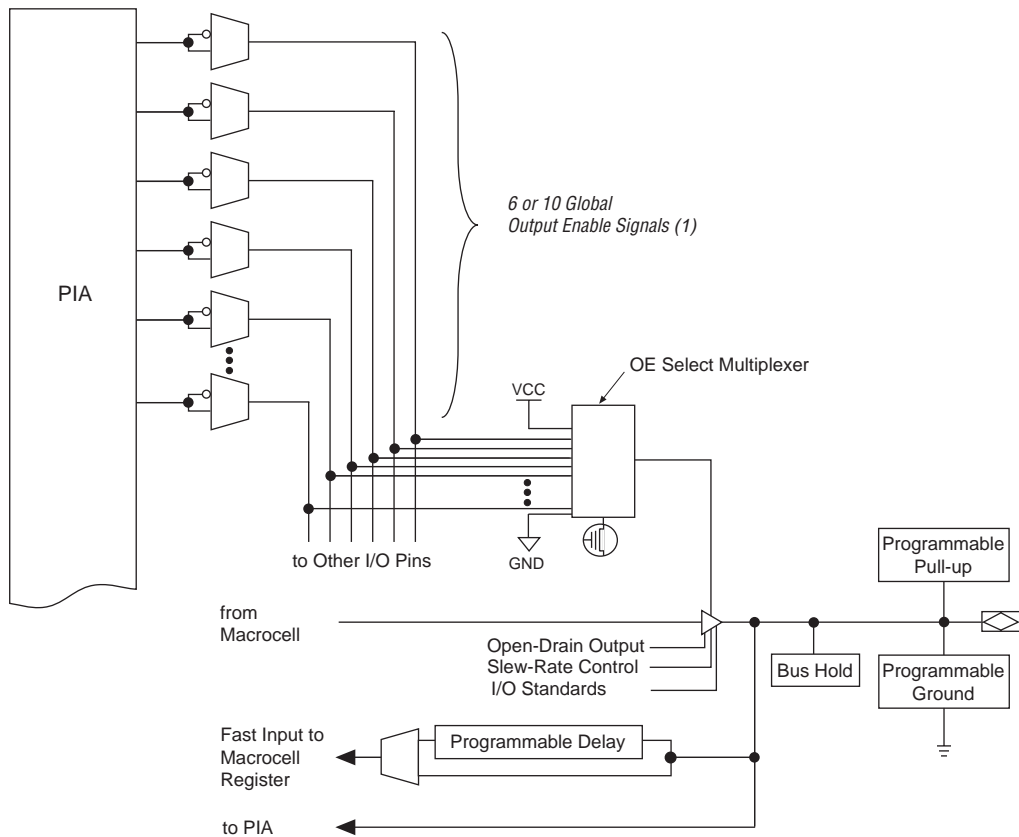
**Figure 5. MAX 7000B PIA Routing**

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

### I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000B Devices

**Note:**

- (1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. [Tables 7 and 8](#) show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

**Table 7. MAX 7000B Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

**Table 8. 32-Bit MAX 7000B Device IDCODE** *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG boundary-scan testing.

[Figure 8](#) shows the timing information for the JTAG signals.

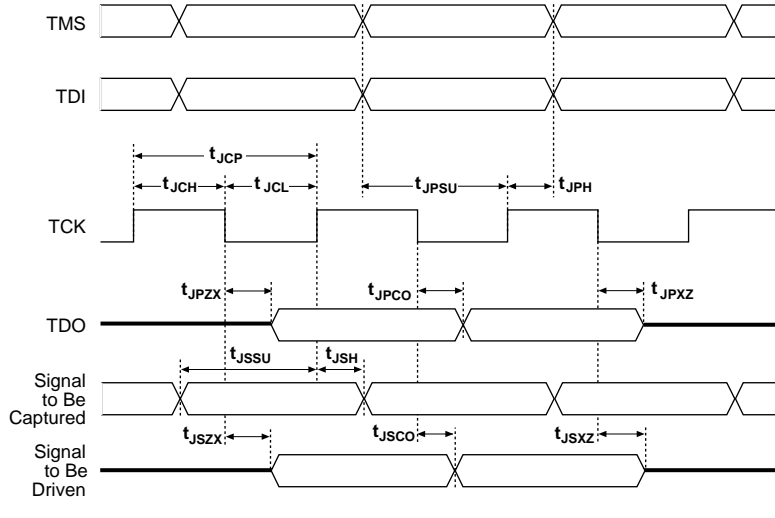
**Figure 8. MAX 7000B JTAG Waveforms**

Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

**Table 9. JTAG Timing Parameters & Values for MAX 7000B Devices***Note (1)*

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns

**Note:**(1) Timing parameters in this table apply to all  $V_{CCIO}$  levels.



**Table 10. MAX 7000B MultiVolt I/O Support**

V <sub>CCIO</sub> (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

### Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

### Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

### Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

### Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

MAX 7000B devices contain two I/O banks. Both banks support all standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Within a bank, any one of the terminated standards can be supported.

Figure 9 shows the arrangement of the MAX 7000B I/O banks.

**Figure 9. MAX 7000B I/O Banks for Various Advanced I/O Standards**

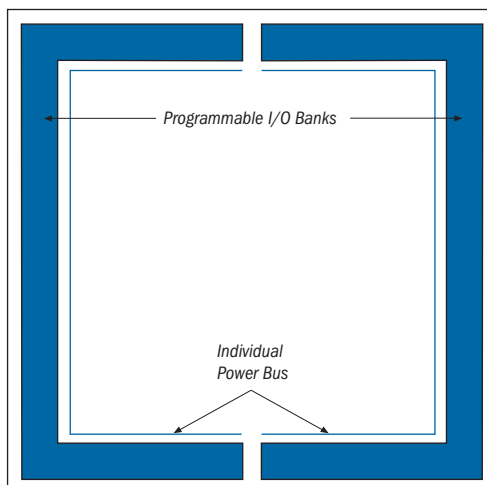


Table 11 shows which macrocells have pins in each I/O bank.

<b>Table 11. Macrocell Pins Contained in Each I/O Bank</b>		
<b>Device</b>	<b>Bank 1</b>	<b>Bank 2</b>
EPM7032B	1-16	17-32
EPM7064B	1-32	33-64
EPM7128B	1-64	65-128
EPM7256B	1-128, 177-181	129-176, 182-256
EPM7512B	1-265	266-512

Each MAX 7000B device has two VREF pins. Each can be set to a separate VREF level. Any I/O pin that uses one of the voltage-referenced standards (GTL+, SSTL-2, or SSTL-3) may use either of the two VREF pins. If these pins are not required as VREF pins, they may be individually programmed to function as user I/O pins.

Tables 18 through 32 show MAX 7000B device timing parameters.

**Table 18. EPM7032B External Timing Parameters**

*Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.1		3.0		4.5		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		1.0		1.0		1.5		ns
t <sub>FH</sub>	Global clock hold time of fast input		1.0		1.0		1.0		ns
t <sub>FZHSU</sub>	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t <sub>FZHH</sub>	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t <sub>CH</sub>	Global clock high time		1.5		2.0		3.0		ns
t <sub>CL</sub>	Global clock low time		1.5		2.0		3.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	0.9		1.3		1.9		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		0.6		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t <sub>ACH</sub>	Array clock high time		1.5		2.0		3.0		ns
t <sub>ACL</sub>	Array clock low time		1.5		2.0		3.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

**Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays** *Notes (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3.5		-5.0		-7.5		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to (PIA)		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.8		1.1	ns
	Input to global clock and clear		0.5		0.8		1.1	ns
	Input to fast input register		0.4		0.5		0.8	ns
	All outputs		1.2		1.8		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.8		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.8		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.8		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.8		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.6		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

**Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

**Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		−0.1		−0.2		−0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

**Table 31. EPM7512B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.3		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.3		0.5	ns
$t_{FIN}$	Fast input delay			2.2		3.2		4.0	ns
$t_{FIND}$	Programmable delay adder for fast input			1.5		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.1		2.7	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5		0.7	ns
$t_{LAD}$	Logic array delay			1.7		2.3		3.0	ns
$t_{LAC}$	Logic control array delay			1.5		2.0		2.6	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.2	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.6	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.8		3.8		5.0	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		7.8		8.8		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		2.8		3.8		5.0	ns
$t_{SU}$	Register setup time		1.5		2.0		2.6		ns
$t_H$	Register hold time		0.4		0.5		0.7		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.4		1.4		ns
$t_{RD}$	Register delay			0.5		0.7		1.0	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.4	ns
$t_{IC}$	Array clock delay			1.8		2.4		3.1	ns
$t_{EN}$	Register enable time			1.5		2.0		2.6	ns
$t_{GLOB}$	Global control delay			2.0		2.8		3.6	ns
$t_{PRE}$	Register preset time			1.0		1.4		1.9	ns
$t_{CLR}$	Register clear time			1.0		1.4		1.9	ns
$t_{PIA}$	PIA delay	(2)		2.4		3.4		4.5	ns
$t_{LPA}$	Low-power adder	(4)		2.0		2.7		3.6	ns

**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$ , in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in Application Note 74 (*Evaluating Power for Altera Devices*).



The  $I_{CCINT}$  value depends on the switching frequency and the application logic. The  $I_{CCINT}$  value is calculated with the following equation:

$$I_{CCINT} =$$

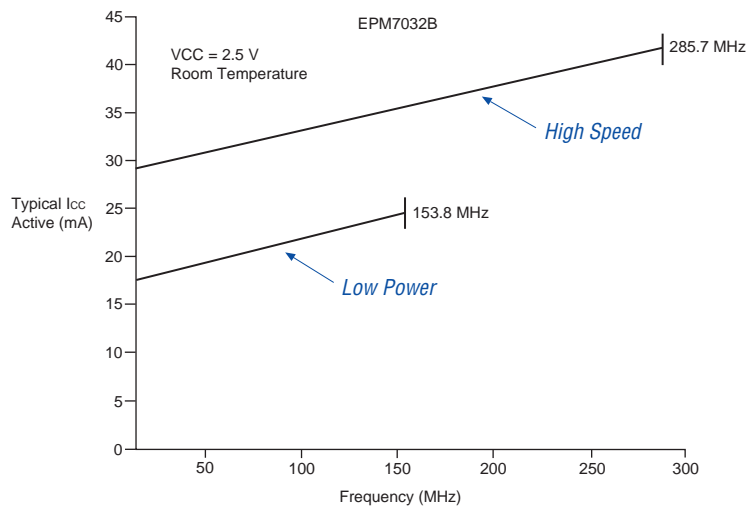
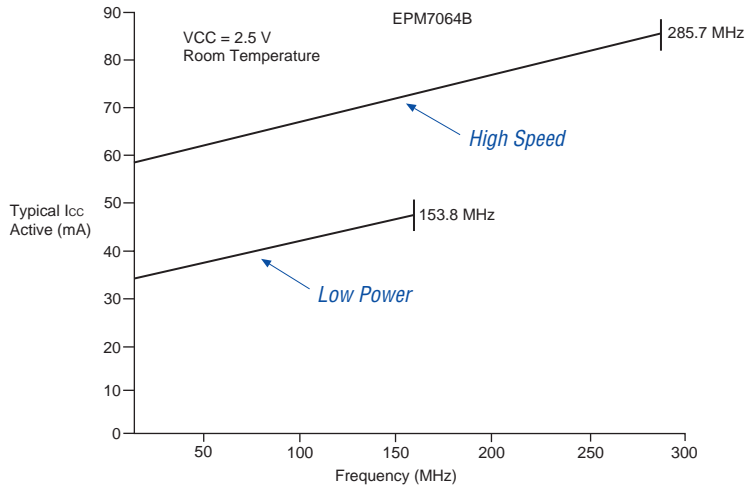
$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \log_{LC})$$

The parameters in this equation are:

- $MC_{TON}$  = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (.rpt)  
 $MC_{DEV}$  = Number of macrocells in the device  
 $MC_{USED}$  = Total number of macrocells in the design, as reported in the Report File  
 $f_{MAX}$  = Highest clock frequency to the device  
 $\log_{LC}$  = Average percentage of logic cells toggling at each clock (typically 12.5%)  
 $A, B, C$  = Constants, shown in [Table 33](#)

<b>Table 33. MAX 7000B <math>I_{CC}</math> Equation Constants</b>			
<b>Device</b>	<b>A</b>	<b>B</b>	<b>C</b>
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

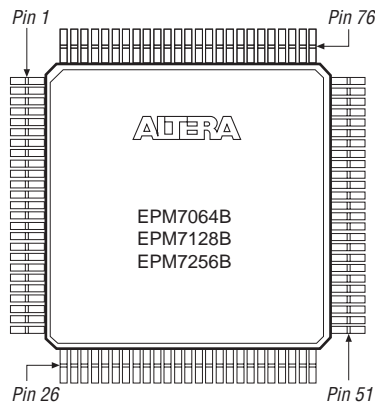
This calculation provides an  $I_{CC}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

**Figure 15.  $I_{CC}$  vs. Frequency for EPM7032B Devices****Figure 16.  $I_{CC}$  vs. Frequency for EPM7064B Devices**

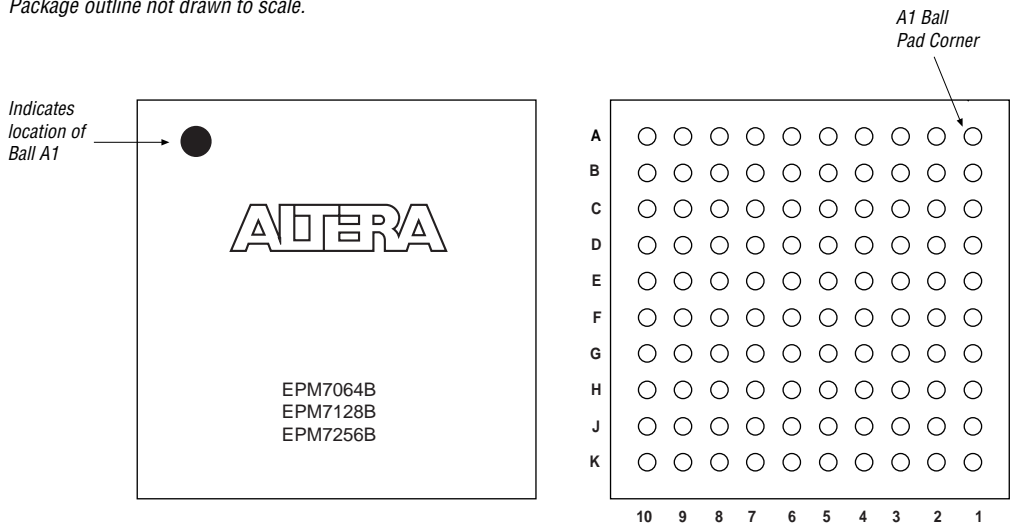


**Figure 23. 100-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

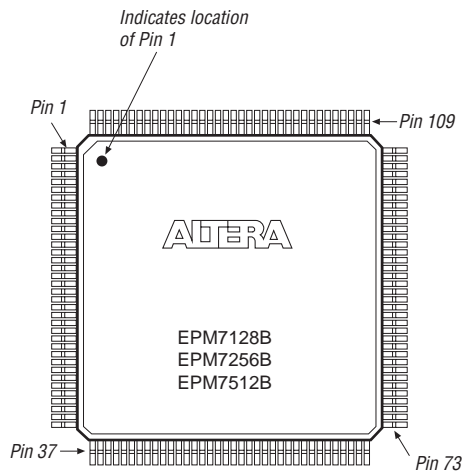
**Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram**

Package outline not drawn to scale.



**Figure 25. 144-Pin TQFP Package Pin-Out Diagram**

*Package outline not drawn to scale.*



**Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram**

*Package outline not drawn to scale.*

