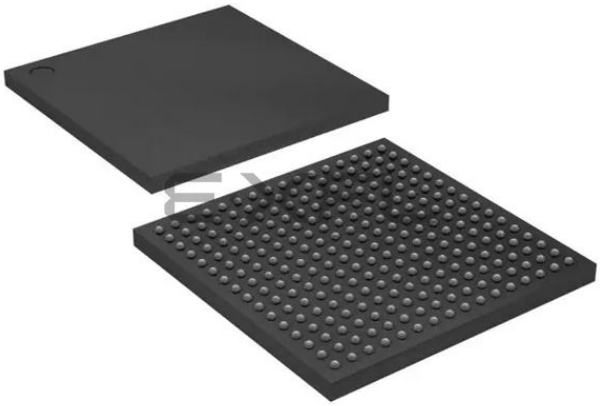

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5 ns |
| Voltage Supply - Internal | 2.375V ~ 2.625V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 256 |
| Number of Gates | 5000 |
| Number of I/O | 164 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7256bfc256-5 |

## …and More Features

- System-level features
  - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
  - Programmable power-saving mode for 50% or greater power reduction in each macrocell
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
  - Bus-hold option on I/O pins
  - PCI compatible
  - Bus-friendly architecture including programmable slew-rate control
  - Open-drain output option
  - Programmable security bit for protection of proprietary designs
  - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
  - Supports hot-socketing operation
  - Programmable ground pins
- Advanced architecture features
  - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
  - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
  - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
  - Two global clock signals with optional inversion
  - Programmable power-up states for macrocell registers
  - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
  - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
  - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
  - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

## General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See Table 2.

*Table 2. MAX 7000B Speed Grades* *Note (1)*

| Device | Speed Grade | | | | |
|---|---|---|---|---|---|
| | -3 | -4 | -5 | -7 | -10 |
| EPM7032B | ✓ | | ✓ | ✓ | |
| EPM7064B | ✓ | | ✓ | ✓ | |
| EPM7128B | | ✓ | | ✓ | ✓ |
| EPM7256B | | | ✓ | ✓ | ✓ |
| EPM7512B | | | ✓ | ✓ | ✓ |

*Notes:*
(1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See Table 3.

*Table 3. MAX 7000B Maximum User I/O Pins* *Note (1)*

| Device | 44-Pin PLCC | 44-Pin TQFP | 48-Pin TQFP *(2)* | 49-Pin 0.8-mm Ultra FineLine BGA *(3)* | 100-Pin TQFP | 100-Pin FineLine BGA *(4)* | 144-Pin TQFP | 169-Pin 0.8-mm Ultra FineLine BGA *(3)* | 208-Pin PQFP | 256-Pin BGA | 256-Pin FineLine BGA *(4)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EPM7032B | 36 | 36 | 36 | 36 | | | | | | | |
| EPM7064B | 36 | 36 | 40 | 41 | 68 | 68 | | | | | |
| EPM7128B | | | | 41 | 84 | 84 | 100 | 100 | | | 100 |
| EPM7256B | | | | | 84 | | 120 | 141 | 164 | | 164 |
| EPM7512B | | | | | | | 120 | 141 | 176 | 212 | 212 |

*Notes:*

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) Contact Altera for up-to-date information on available device package options.

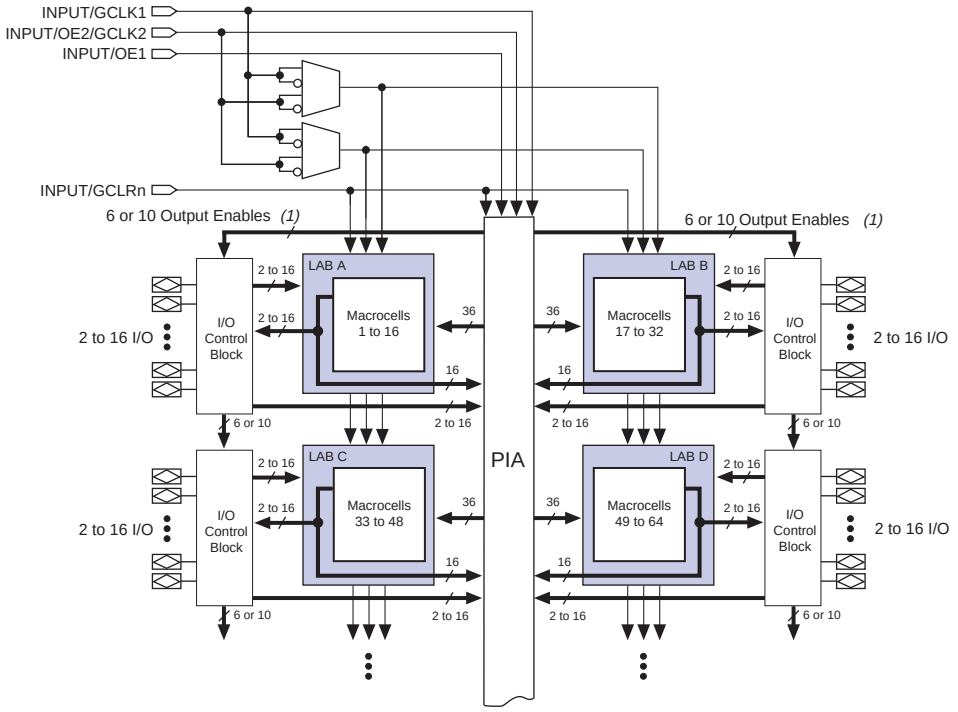
(3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

(4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

*Figure 1. MAX 7000B Device Block Diagram*




*Note:*
(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

## Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000B Device*

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: $t_{PROG}$ = Programming time
$t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
$f_{TCK}$ = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: $t_{VER}$ = Verify time
$t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

*Table 10. MAX 7000B MultiVolt I/O Support*

| $V_{CCIO}$ (V) | Input Signal (V) | | | | Output Signal (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | | | | ✓ | ✓ |

## Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

## Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

## Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

## Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

## Programmable Pull-Up Resistor

Each MAX 7000B device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 50 k¾) weakly holds the output to $V_{CCIO}$ level.

## Bus Hold

Each MAX 7000B device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signals is present, the bus-hold feature can eliminate the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than $V_{CCIO}$ to prevent overdriving signals. The propagation delays through the input and output buffers in MAX 7000B devices are not affected by whether the bus-hold feature is enabled or disabled.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance ($R_{BH}$) of approximately 8.5 k¾. Table 12 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each VCCIO voltage level.

*Table 12. Bus Hold Parameters*

| Parameter | Conditions | VCCIO Level | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $V_{IN} > V_{IL}$ (max) | 30 | | 50 | | 70 | | µA |
| High sustaining current | $V_{IN} < V_{IH}$ (min) | –30 | | –50 | | –70 | | µA |
| Low overdrive current | $0 V < V_{IN} < V_{CCIO}$ | | 200 | | 300 | | 500 | µA |
| High overdrive current | $0 V < V_{IN} < V_{CCIO}$ | | –295 | | –435 | | –680 | µA |

The bus-hold circuitry is active only during user operation. At power-up, the bus-hold circuit initializes its initial hold value as $V_{CC}$ approaches the recommended operation conditions. When transitioning from ISP to User Mode with bus hold enabled, the bus-hold circuit captures the value present on the pin at the end of programming.

*Table 15. MAX 7000B Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(10)* | 2.375 | 2.625 | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 3.3-V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers, 2.5-V operation | | 2.375 | 2.625 | V |
| | Supply voltage for output drivers, 1.8-V operation | | 1.71 | 1.89 | V |
| $V_{CCISP}$ | Supply voltage during in-system programming | | 2.375 | 2.625 | V |
| $V_I$ | Input voltage | *(3)* | –0.5 | 3.9 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use *(11)* | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use *(11)* | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 16. MAX 7000B Device DC Operating Conditions* *Note (4)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage for 3.3-V TTL/CMOS | | 2.0 | 3.9 | V |
| | High-level input voltage for 2.5-V TTL/CMOS | | 1.7 | 3.9 | V |
| | High-level input voltage for 1.8-V TTL/CMOS | | 0.65 × $V_{CCIO}$ | 3.9 | V |
| $V_{IL}$ | Low-level input voltage for 3.3-V TTL/CMOS and PCI compliance | | –0.5 | 0.8 | V |
| | Low-level input voltage for 2.5-V TTL/CMOS | | –0.5 | 0.7 | V |
| | Low-level input voltage for 1.8-V TTL/CMOS | | –0.5 | 0.35 × $V_{CCIO}$ | |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | $V_{CCIO}$ – 0.2 | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –100 µA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 1.7 | | V |
| | 1.8-V high-level output voltage | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ =1.65 V *(5)* | 1.2 | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.4 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.2 | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.7 | V |
| | 1.8-V low-level output voltage | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 1.7 V *(6)* | | 0.4 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 3.9 V *(7)* | –10 | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_I$ = –0.5 to 3.9 V *(7)* | –10 | 10 | µA |
| $R_{ISP}$ | Value of I/O pin pull-up resistor during in-system programming or during power up | $V_{CCIO}$ = 1.7 to 3.6 V *(8)* | 20 | 74 | k¾ |

*Table 17. MAX 7000B Device Capacitance* *Note (9)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(4) These values are specified under the Recommended Operating Conditions in Table 15 on page 29.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The $I_{OL}$ parameter refers to low-level TTL or CMOS output current.
(7) This value is specified for normal device operation. During power-up, the maximum leakage current is ±300 µA.
(8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to $V_{CCIO}$.
(9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.
(10) The POR time for all 7000B devices does not exceed 100 µs. The sufficient $V_{CCINT}$ voltage level for POR is 2.375 V. The device is fully initialized within the POR time after $V_{CCINT}$ reaches the sufficient POR voltage level.
(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

*Table 21. EPM7064B External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 | | -5 | | -7 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 3.5 | | 5.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 3.5 | | 5.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.1 | | 3.0 | | 4.5 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.0 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 2.4 | 1.0 | 3.4 | 1.0 | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 0.9 | | 1.3 | | 1.9 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | 0.6 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 3.6 | 1.0 | 5.1 | 1.0 | 7.6 | ns |
| $t_{ACH}$ | Array clock high time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 3.3 | | 4.7 | | 7.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 303.0 | | 212.8 | | 142.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 3.3 | | 4.7 | | 7.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 303.0 | | 212.8 | | 142.9 | | MHz |

*Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -5 | | -7 | | |
| | | Min | Max | Min | Max | Min | Max | |
| 3.3 V TTL/CMOS | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| 2.5 V TTL/CMOS | Input to PIA | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to global clock and clear | | 0.3 | | 0.4 | | 0.6 | ns |
| | Input to fast input register | | 0.2 | | 0.3 | | 0.4 | ns |
| | All outputs | | 0.2 | | 0.3 | | 0.4 | ns |
| 1.8 V TTL/CMOS | Input to PIA | | 0.5 | | 0.7 | | 1.1 | ns |
| | Input to global clock and clear | | 0.5 | | 0.7 | | 1.1 | ns |
| | Input to fast input register | | 0.4 | | 0.6 | | 0.9 | ns |
| | All outputs | | 1.2 | | 1.7 | | 2.6 | ns |
| SSTL-2 Class I | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-2 Class II | Input to PIA | | 1.3 | | 1.9 | | 2.8 | ns |
| | Input to global clock and clear | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to fast input register | | 0.9 | | 1.3 | | 1.9 | ns |
| | All outputs | | –0.1 | | –0.1 | | –0.2 | ns |
| SSTL-3 Class I | Input to PIA | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| SSTL-3 Class II | Input to PIA | | 1.2 | | 1.7 | | 2.6 | ns |
| | Input to global clock and clear | | 0.9 | | 1.3 | | 1.9 | ns |
| | Input to fast input register | | 0.8 | | 1.1 | | 1.7 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |
| GTL+ | Input to PIA | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to global clock and clear | | 1.6 | | 2.3 | | 3.4 | ns |
| | Input to fast input register | | 1.5 | | 2.1 | | 3.2 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -5 | | -7 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of all LABs.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

*Table 24. EPM7128B External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 4.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 4.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.5 | | 4.5 | | 6.1 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.0 | | 3.0 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 2.8 | 1.0 | 5.7 | 1.0 | 7.5 | ns |
| $t_{CH}$ | Global clock high time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.2 | | 2.0 | | 2.8 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.7 | | 0.9 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.1 | 1.0 | 8.2 | 1.0 | 10.8 | ns |
| $t_{ACH}$ | Array clock high time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 4.1 | | 7.9 | | 10.6 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 243.9 | | 126.6 | | 94.3 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 4.1 | | 7.9 | | 10.6 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 243.9 | | 126.6 | | 94.3 | | MHz |

*Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -5 | | -7 | | -10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

*Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)* *Note (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -5 | | -7 | | -10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCINT}$ value depends on the switching frequency and the application logic. The $I_{CCINT}$ value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

$MC_{TON}$ = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
$MC_{DEV}$ = Number of macrocells in the device
$MC_{USED}$ = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 33

*Table 33. MAX 7000B $I_{CC}$ Equation Constants*

| Device | A | B | C |
|---|---|---|---|
| EPM7032B | 0.91 | 0.54 | 0.010 |
| EPM7064B | 0.91 | 0.54 | 0.012 |
| EPM7128B | 0.91 | 0.54 | 0.016 |
| EPM7256B | 0.91 | 0.54 | 0.017 |
| EPM7512B | 0.91 | 0.54 | 0.019 |

This calculation provides an $I_{CC}$ estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual $I_{CC}$ should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

*Figure 21. 48-Pin VTQFP Package Pin-Out Diagram*

*Package outlines not drawn to scale.*

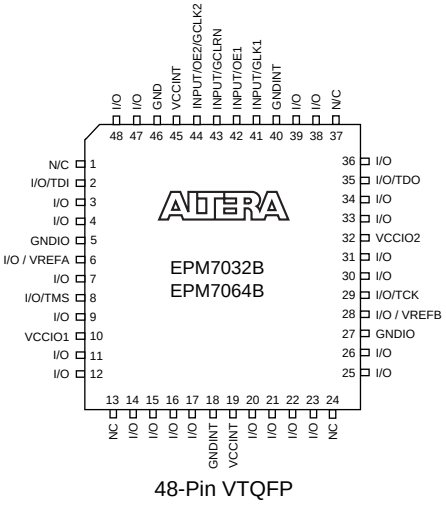
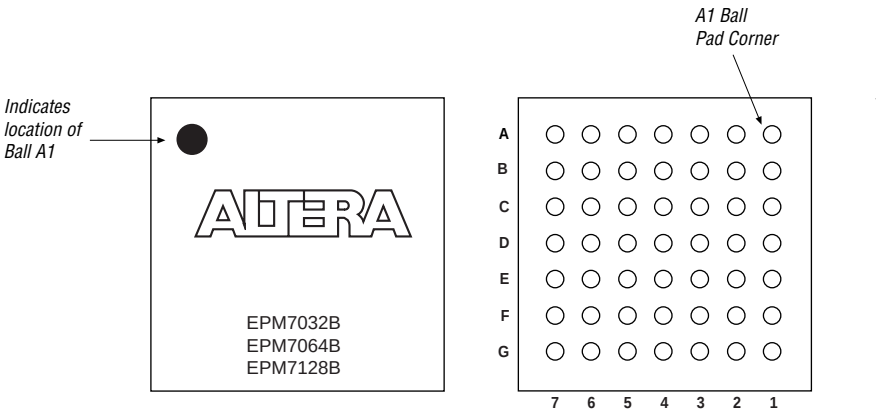



*Figure 22. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram*

*Package outline not drawn to scale.*



## Version 3.3

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.3:

- Updated Table 3.
- Added Tables 4 through 6.

## Version 3.2

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.2:

- Updated *Note (10)* and added ambient temperature ($T_A$) information to Table 15.

## Version 3.1

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.1:

- Updated $V_{IH}$ and $V_{IL}$ specifications in Table 16.
- Updated leakage current conditions in Table 16.

## Version 3.0

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.0:

- Updated timing numbers in Table 1.
- Updated Table 16.
- Updated timing in Tables 18, 19, 21, 22, 24, 25, 27, 28, 30, and 31.

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