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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	164
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7256bfc256-7n">https://www.e-xfl.com/product-detail/intel/epm7256bfc256-7n</a>

**Table 3. MAX 7000B Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP (2)	49-Pin 0.8-mm Ultra FineLine BGA (3)	100- Pin TQFP	100-Pin FineLine BGA (4)	144- Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA (3)	208- Pin PQFP	256- Pin BGA	256-Pin FineLine BGA (4)
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B				41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B							120	141	176	212	212

**Notes:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) Contact Altera for up-to-date information on available device package options.
- (3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.
- (4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 7000B architecture includes the following elements:

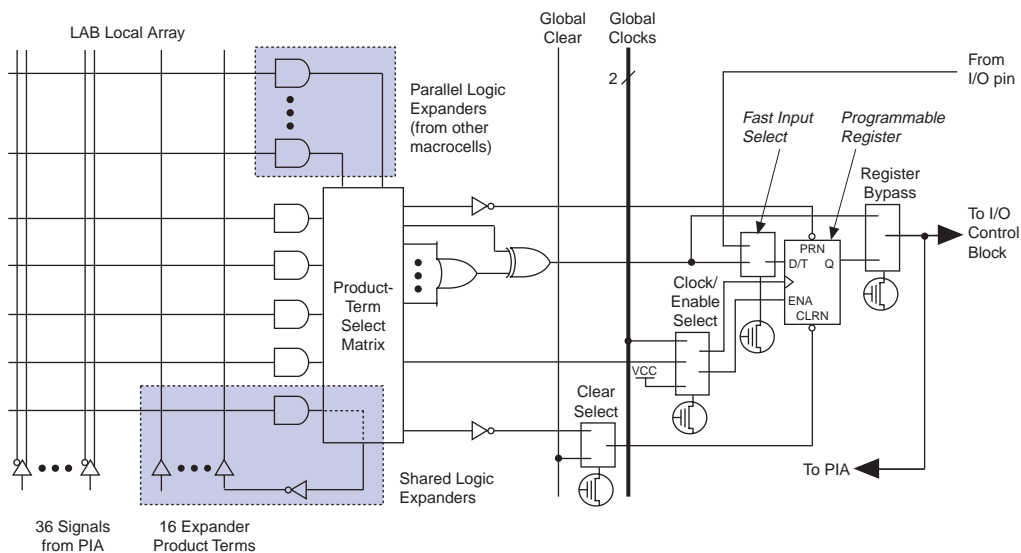
- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000B devices.

## Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

**Figure 2. MAX 7000B Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

## Expander Product Terms

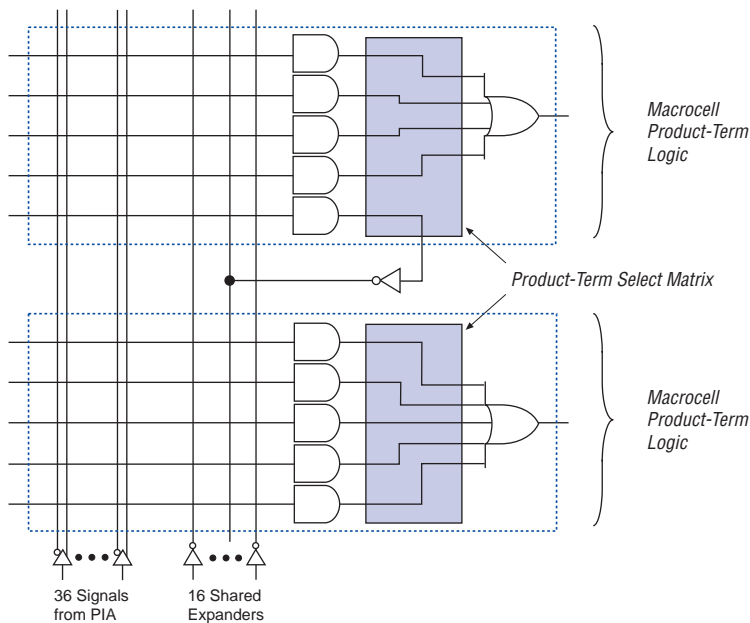
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

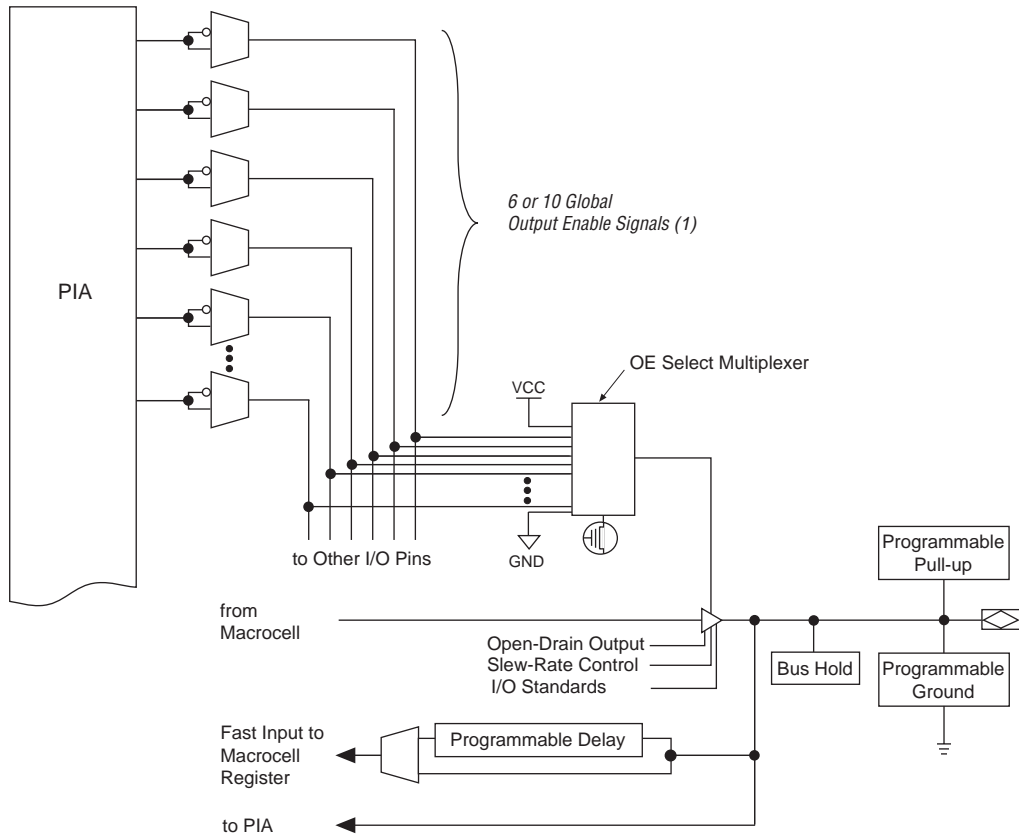
### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

**Figure 3. MAX 7000B Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in a LAB.*



**Figure 6. I/O Control Block of MAX 7000B Devices****Note:**

- (1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

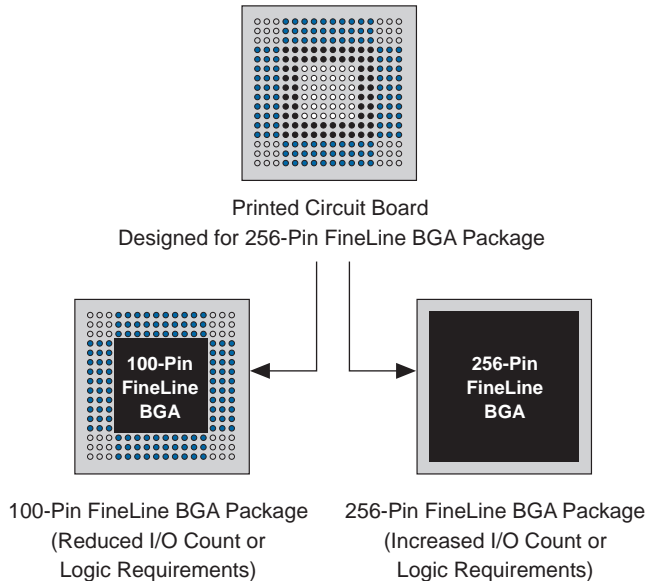
The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see [Figure 7](#)).

**Figure 7. SameFrame Pin-Out Example**



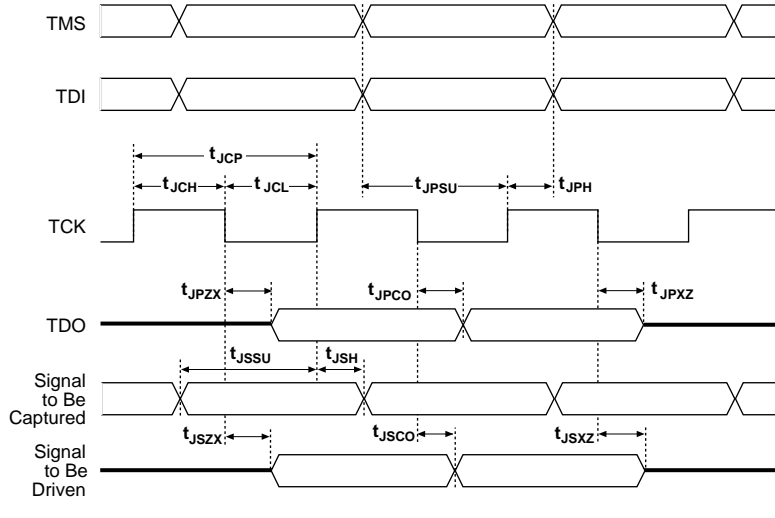
**Figure 8. MAX 7000B JTAG Waveforms**

Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

<b>Table 9. JTAG Timing Parameters &amp; Values for MAX 7000B Devices</b> <i>Note (1)</i>				
Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns

**Note:**

(1) Timing parameters in this table apply to all  $V_{CCIO}$  levels.



MAX 7000B devices contain two I/O banks. Both banks support all standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Within a bank, any one of the terminated standards can be supported.

Figure 9 shows the arrangement of the MAX 7000B I/O banks.

**Figure 9. MAX 7000B I/O Banks for Various Advanced I/O Standards**

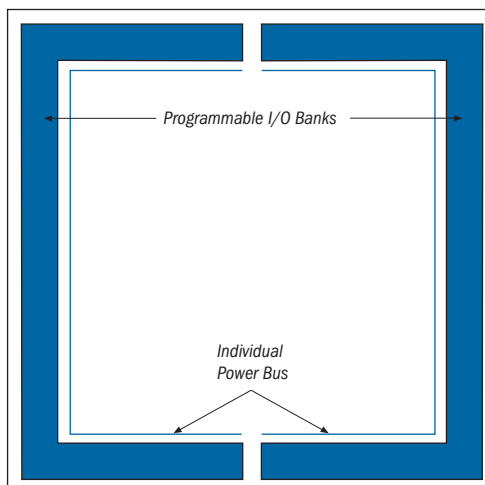


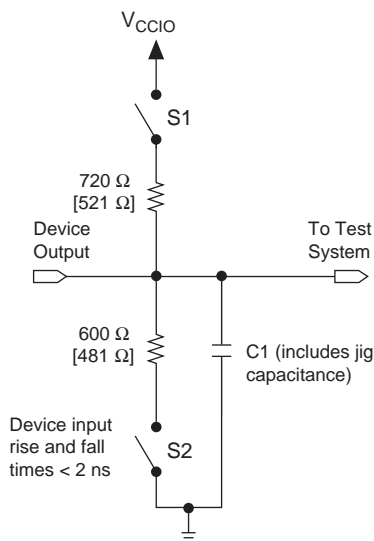
Table 11 shows which macrocells have pins in each I/O bank.

<b>Table 11. Macrocell Pins Contained in Each I/O Bank</b>		
<b>Device</b>	<b>Bank 1</b>	<b>Bank 2</b>
EPM7032B	1-16	17-32
EPM7064B	1-32	33-64
EPM7128B	1-64	65-128
EPM7256B	1-128, 177-181	129-176, 182-256
EPM7512B	1-265	266-512

Each MAX 7000B device has two VREF pins. Each can be set to a separate VREF level. Any I/O pin that uses one of the voltage-referenced standards (GTL+, SSTL-2, or SSTL-3) may use either of the two VREF pins. If these pins are not required as VREF pins, they may be individually programmed to function as user I/O pins.

**Figure 11. MAX 7000B AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



## Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

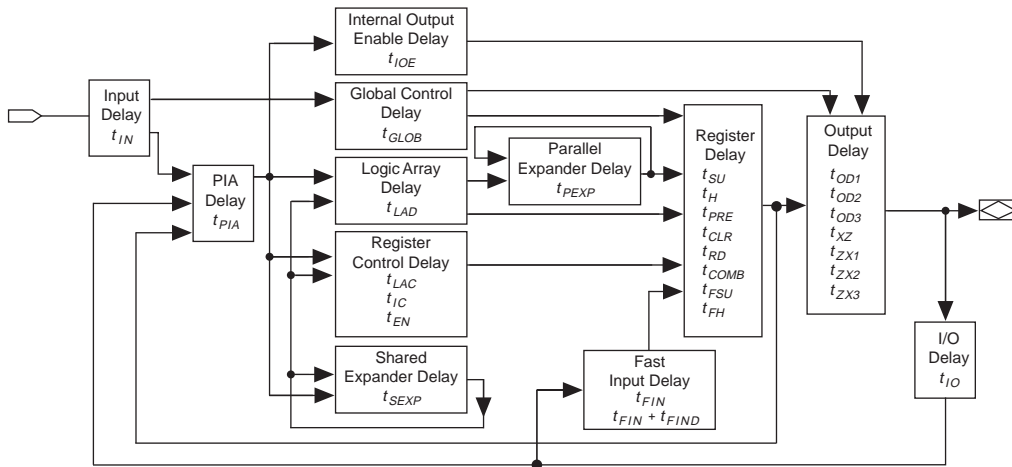
**Table 14. MAX 7000B Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage		-0.5	3.6	V
$V_{CCIO}$	Supply voltage		-0.5	3.6	V
$V_I$	DC input voltage	(2)	-2.0	4.6	V
$I_{OUT}$	DC output current, per pin		-33	50	mA
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_A$	Ambient temperature	Under bias	-65	135	°C
$T_J$	Junction temperature	Under bias	-65	135	°C

## Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

**Figure 13. MAX 7000B Timing Model**



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

Tables 18 through 32 show MAX 7000B device timing parameters.

**Table 18. EPM7032B External Timing Parameters**

*Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.1		3.0		4.5		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		1.0		1.0		1.5		ns
t <sub>FH</sub>	Global clock hold time of fast input		1.0		1.0		1.0		ns
t <sub>FZHSU</sub>	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t <sub>FZHH</sub>	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t <sub>CH</sub>	Global clock high time		1.5		2.0		3.0		ns
t <sub>CL</sub>	Global clock low time		1.5		2.0		3.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	0.9		1.3		1.9		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		0.6		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t <sub>ACH</sub>	Array clock high time		1.5		2.0		3.0		ns
t <sub>ACL</sub>	Array clock low time		1.5		2.0		3.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

**Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays** *Notes (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3.5		-5.0		-7.5		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

Table 24. EPM7128B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		4.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		4.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.5		4.5		6.1		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		1.0		1.5		1.5		ns
t <sub>FH</sub>	Global clock hold time of fast input		1.0		1.0		1.0		ns
t <sub>FZHSU</sub>	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
t <sub>FZHH</sub>	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.7	1.0	7.5	ns
t <sub>CH</sub>	Global clock high time		1.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		1.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.2		2.0		2.8		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.7		0.9		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.1	1.0	8.2	1.0	10.8	ns
t <sub>ACH</sub>	Array clock high time		1.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		1.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset		1.5		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.1		7.9		10.6	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (3)	243.9		126.6		94.3		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.1		7.9		10.6	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (3)	243.9		126.6		94.3		MHz

**Table 28. EPM7256B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.4		0.6		0.8	ns
$t_{IO}$	I/O input pad and buffer delay			0.4		0.6		0.8	ns
$t_{FIN}$	Fast input delay			1.5		2.5		3.1	ns
$t_{FIND}$	Programmable delay adder for fast input			1.5		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.3		3.0	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.6		0.8	ns
$t_{LAD}$	Logic array delay			1.7		2.5		3.3	ns
$t_{LAC}$	Logic control array delay			1.5		2.2		2.9	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.3	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.4		1.9	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.4		6.9	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.2		3.3		4.5	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		7.2		8.3		9.5	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		2.2		3.3		4.5	ns
$t_{SU}$	Register setup time		1.2		1.8		2.5		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.4		1.4		ns
$t_{RD}$	Register delay			0.7		1.0		1.3	ns
$t_{COMB}$	Combinatorial delay			0.3		0.4		0.5	ns
$t_{IC}$	Array clock delay			1.5		2.3		3.0	ns
$t_{EN}$	Register enable time			1.5		2.2		2.9	ns
$t_{GLOB}$	Global control delay			1.3		2.1		2.7	ns
$t_{PRE}$	Register preset time			1.0		1.6		2.1	ns
$t_{CLR}$	Register clear time			1.0		1.6		2.1	ns
$t_{PIA}$	PIA delay	(2)		1.7		2.6		3.3	ns
$t_{LPA}$	Low-power adder	(4)		2.0		3.0		4.0	ns

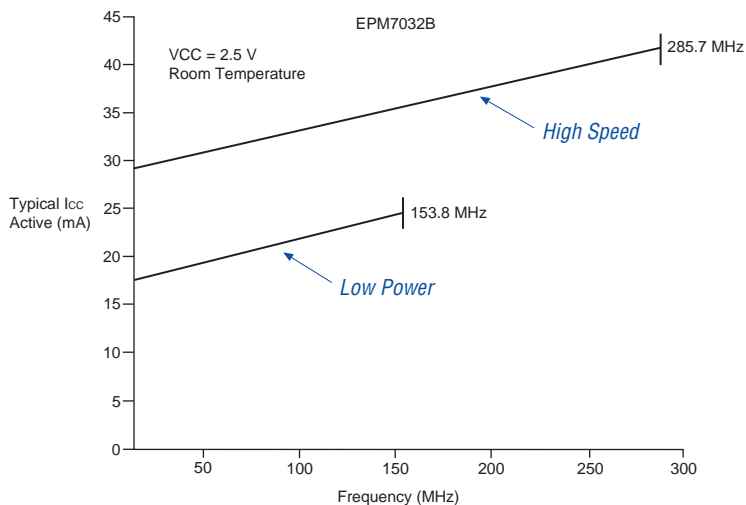
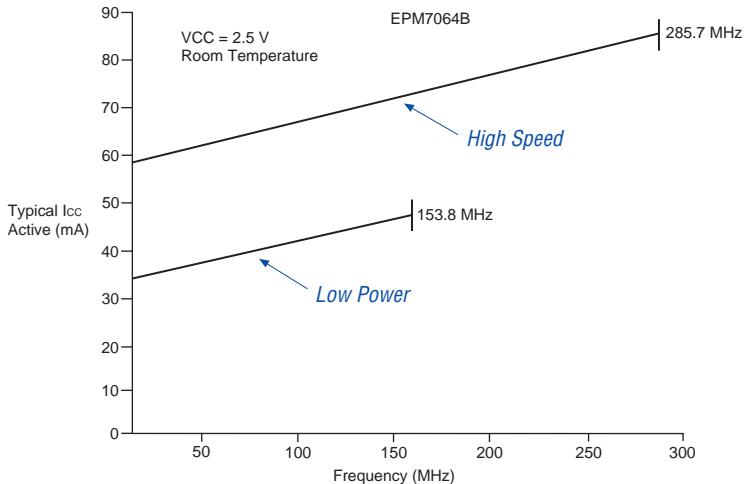
**Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.



**Figure 15.  $I_{CC}$  vs. Frequency for EPM7032B Devices****Figure 16.  $I_{CC}$  vs. Frequency for EPM7064B Devices**

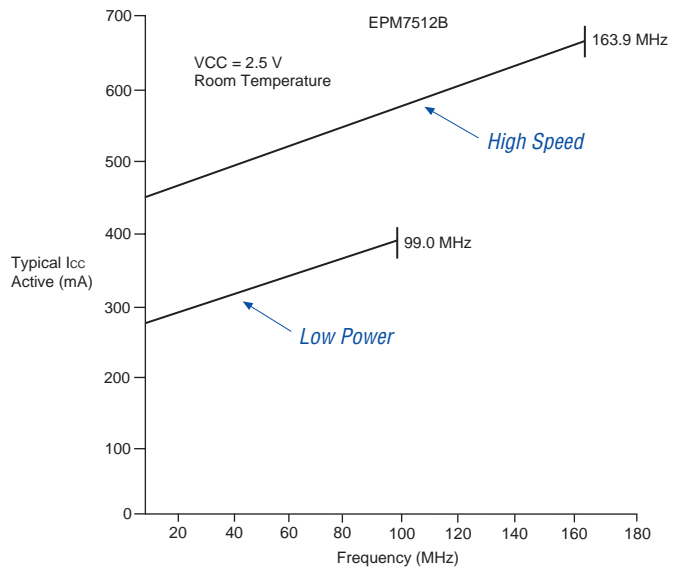
**Figure 19.  $I_{CC}$  vs. Frequency for EPM7512B Devices**

Figure 25. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

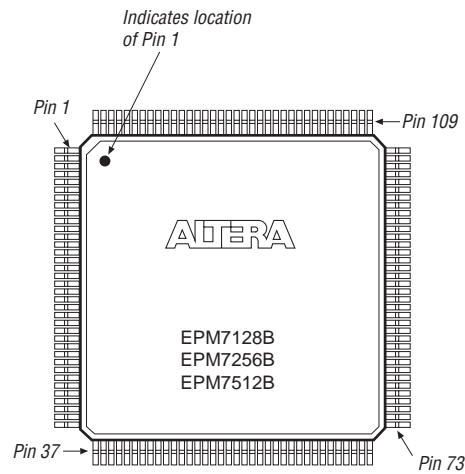
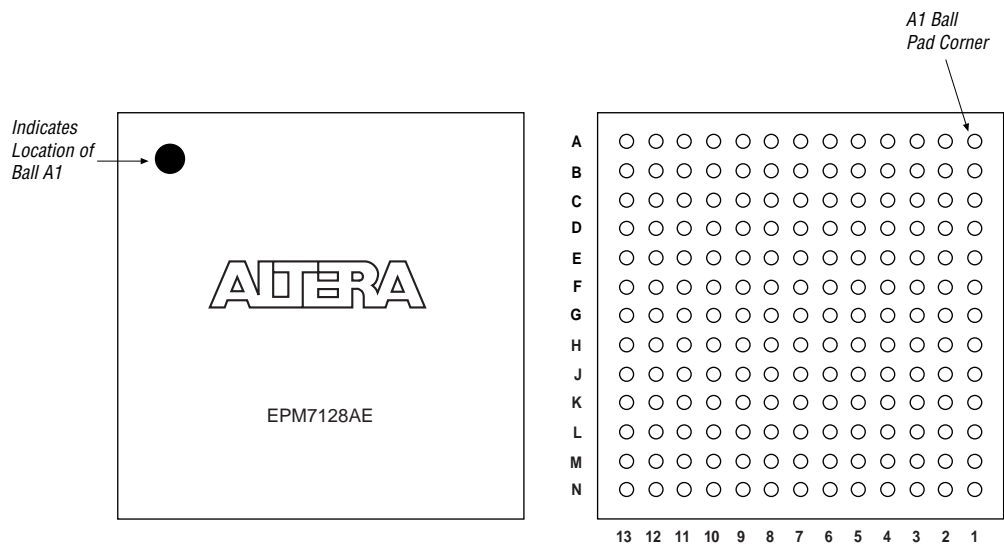


Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram

Package outline not drawn to scale.





### Version 3.3

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.3:

- Updated [Table 3](#).
- Added [Tables 4](#) through [6](#).

### Version 3.2

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.2:

- Updated [Note \(10\)](#) and added ambient temperature ( $T_A$ ) information to [Table 15](#).

### Version 3.1

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.1:

- Updated  $V_{IH}$  and  $V_{IL}$  specifications in [Table 16](#).
- Updated leakage current conditions in [Table 16](#).

### Version 3.0

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.0:

- Updated timing numbers in [Table 1](#).
- Updated [Table 16](#).
- Updated timing in [Tables 18, 19, 21, 22, 24, 25, 27, 28, 30, and 31](#).



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