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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256btc100-10n

...and More Features

- System-level features
 - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
 - Programmable power-saving mode for 50% or greater power reduction in each macrocell
 - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
 - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
 - Bus-hold option on I/O pins
 - PCI compatible
 - Bus-friendly architecture including programmable slew-rate control
 - Open-drain output option
 - Programmable security bit for protection of proprietary designs
 - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
 - Supports hot-socketing operation
 - Programmable ground pins
- Advanced architecture features
 - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
 - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
 - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
 - Two global clock signals with optional inversion
 - Programmable power-up states for macrocell registers
 - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
 - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
 - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
 - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

Table 3. MAX 7000B Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP (2)	49-Pin 0.8-mm Ultra FineLine BGA (3)	100- Pin TQFP	100-Pin FineLine BGA (4)	144- Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA (3)	208- Pin PQFP	256- Pin BGA	256-Pin FineLine BGA (4)
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B				41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B							120	141	176	212	212

Notes:

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) Contact Altera for up-to-date information on available device package options.
- (3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.
- (4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 14](#) for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



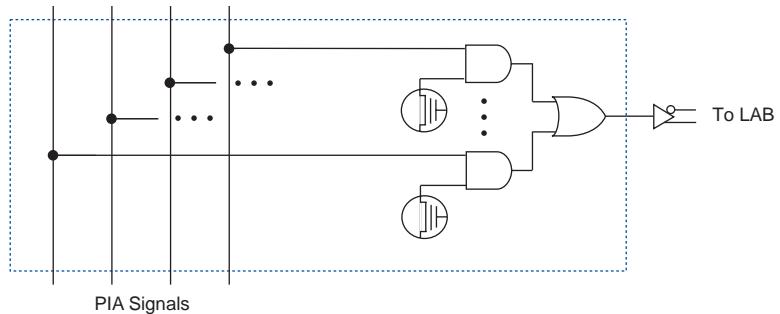
For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000B devices.

Figure 5. MAX 7000B PIA Routing

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000B device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Programming with External Hardware



MAX 7000B devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see [Programming Hardware Manufacturers](#).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000B devices include the JTAG boundary-scan test circuitry defined by IEEE Std. 1149.1. [Table 6](#) describes the JTAG instructions supported by MAX 7000B devices. The pin-out tables starting on [page 59](#) of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 6. MAX 7000B JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary-scan test data to pass synchronously through a selected device to adjacent devices during normal operation.
CLAMP	Allows the values in the boundary-scan register to determine pin states while placing the 1-bit bypass register between the TDI and TDO pins.
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO.
ISP Instructions	These instructions are used when programming MAX 7000B devices via the JTAG ports with the MasterBlaster or ByteBlasterMV download cable, or using a Jam File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf) via an embedded processor or test equipment.

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. [Tables 7 and 8](#) show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

Table 7. MAX 7000B Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

Table 8. 32-Bit MAX 7000B Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

Notes:

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG boundary-scan testing.

[Figure 8](#) shows the timing information for the JTAG signals.

Table 10. MAX 7000B MultiVolt I/O Support

V _{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

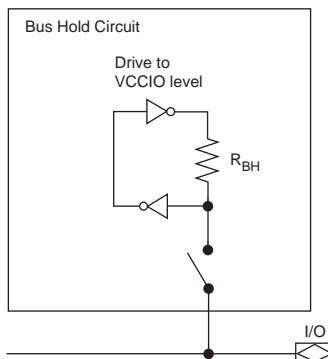
Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2* except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications

Device	Specification	
	33-MHz PCI	66-MHz PCI
EPM7032B	All speed grades	-3
EPM7064B	All speed grades	-3
EPM7128B	All speed grades	-4
EPM7256B	All speed grades	-5 (1)
EPM7512B	All speed grades	-5 (1)

Note:

- (1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

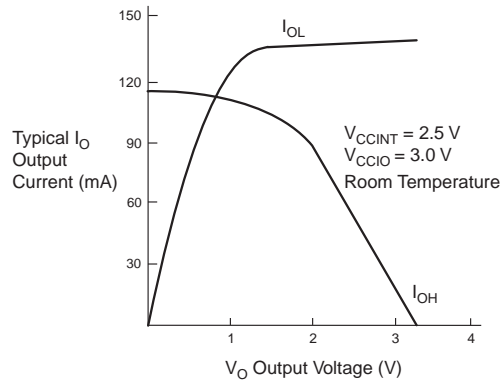
Table 15. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(10)	2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	(3)	−0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use (11)	−40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use (11)	−40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

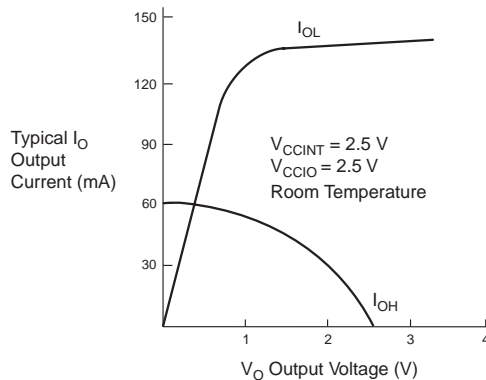
Figure 12 shows the typical output drive characteristics of MAX 7000B devices.

Figure 12. Output Drive Characteristics of MAX 7000B Devices

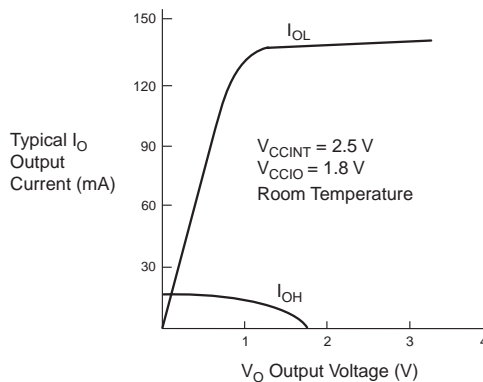
3.3-V VCCIO



2.5-V VCCIO



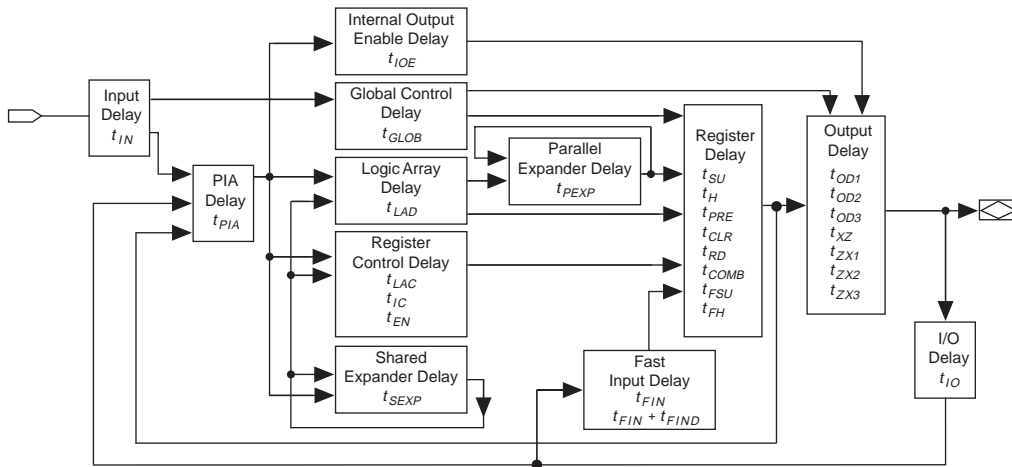
1.8-V VCCIO



Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

Table 21. EPM7064B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{SU}	Global clock setup time	(2)	2.1		3.0		4.5		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t _{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t _{CH}	Global clock high time		1.5		2.0		3.0		ns
t _{CL}	Global clock low time		1.5		2.0		3.0		ns
t _{ASU}	Array clock setup time	(2)	0.9		1.3		1.9		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.6		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t _{ACH}	Array clock high time		1.5		2.0		3.0		ns
t _{ACL}	Array clock low time		1.5		2.0		3.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t _{CNT}	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t _{ACNT}	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

Table 24. EPM7128B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		4.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		4.0		7.5		10.0	ns
t _{SU}	Global clock setup time	(2)	2.5		4.5		6.1		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t _{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.7	1.0	7.5	ns
t _{CH}	Global clock high time		1.5		3.0		4.0		ns
t _{CL}	Global clock low time		1.5		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.2		2.0		2.8		ns
t _{AH}	Array clock hold time	(2)	0.2		0.7		0.9		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.1	1.0	8.2	1.0	10.8	ns
t _{ACH}	Array clock high time		1.5		3.0		4.0		ns
t _{ACL}	Array clock low time		1.5		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		1.5		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.1		7.9		10.6	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	243.9		126.6		94.3		MHz
t _{ACNT}	Minimum array clock period	(2)		4.1		7.9		10.6	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	243.9		126.6		94.3		MHz

Table 25. EPM7128B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.6		0.8	ns
t_{FIN}	Fast input delay			1.3		2.9		3.7	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.8		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.8		1.0	ns
t_{LAD}	Logic array delay			1.6		2.9		3.8	ns
t_{LAC}	Logic control array delay			1.4		2.6		3.4	ns
t_{IOE}	Internal output enable delay			0.1		0.3		0.4	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.7		2.2	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.7		7.2	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.8		3.3		4.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.8		8.3		9.4	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		1.8		3.3		4.4	ns
t_{SU}	Register setup time		1.0		1.9		2.6		ns
t_H	Register hold time		0.4		0.8		1.1		ns
t_{FSU}	Register setup time of fast input		0.8		0.9		0.9		ns
t_{FH}	Register hold time of fast input		1.2		1.6		1.6		ns
t_{RD}	Register delay			0.5		1.1		1.4	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.4		2.8		3.6	ns
t_{EN}	Register enable time			1.4		2.6		3.4	ns
t_{GLOB}	Global control delay			1.1		2.3		3.1	ns
t_{PRE}	Register preset time			1.0		1.9		2.6	ns
t_{CLR}	Register clear time			1.0		1.9		2.6	ns
t_{PIA}	PIA delay	(2)		1.0		2.0		2.8	ns
t_{LPA}	Low-power adder	(4)		1.5		2.8		3.8	ns

Table 26. EPM7128B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		−0.1		−0.2		−0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.5		0.7	ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.3	ns
	All outputs		0.2		0.3		0.3	ns
1.8 V TTL/CMOS	Input to PIA		0.7		1.0		1.3	ns
	Input to global clock and clear		0.6		0.8		1.0	ns
	Input to fast input register		0.5		0.6		0.8	ns
	All outputs		1.3		1.8		2.3	ns
SSTL-2 Class I	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.5		3.3	ns
	Input to global clock and clear		1.9		2.6		3.5	ns
	Input to fast input register		1.8		2.5		3.3	ns
	All outputs		0.0		0.0		0.0	ns

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \log_{LC})$$

The parameters in this equation are:

- MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (.rpt)
 MC_{DEV} = Number of macrocells in the device
 MC_{USED} = Total number of macrocells in the design, as reported in the Report File
 f_{MAX} = Highest clock frequency to the device
 \log_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)
 A, B, C = Constants, shown in [Table 33](#)

Table 33. MAX 7000B I_{CC} Equation Constants			
Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.