# E·XFL

### Intel - EPM7256BTC144-7N Datasheet



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#### Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	120
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256btc144-7n

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#### Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.



Figure 2. MAX 7000B Macrocell

Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

#### Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.



Figure 5. MAX 7000B PIA Routing

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

# In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industrystandard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k<sup>3</sup>/<sub>4</sub>.

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP\_Done bit that provides safe operation when in-system programming is interrupted. This ISP\_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam language, see *Application Note 88* (Using the Jam Language for ISP & ICR via an Embedded Processor) and Application Note 122 (Using STAPL for ISP & ICR via an Embedded Processor).

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

#### Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

<sup>t</sup> PROG	= t <sub>PPULSE</sub> ++	<sup>Сусle</sup> ртск <sup>f</sup> тск
where:	t <sub>PROG</sub> t <sub>PPULSE</sub>	<ul><li>= Programming time</li><li>= Sum of the fixed times to erase, program, and verify the EEPROM cells</li></ul>
	Cycle <sub>PTCK</sub> f <sub>TCK</sub>	<ul><li>Number of TCK cycles to program a device</li><li>TCK frequency</li></ul>

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$t_{VER} =$	$t_{VPULSE} + \frac{C_1}{2}$	<sup>ICLe</sup> VTCK <sup>f</sup> TCK
where:	t <sub>VER</sub> t <sub>VPULSE</sub> Cycle <sub>VTCK</sub>	<ul><li>= Verify time</li><li>= Sum of the fixed times to verify the EEPROM cells</li><li>= Number of TCK cycles to verify a device</li></ul>

# Programmable Speed/Power Control

Output

Configuration

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters.

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

## MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V<sub>CCIO</sub> levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

#### Programmable Pull-Up Resistor

Each MAX 7000B device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 50 k<sup>3</sup>/<sub>4</sub>) weakly holds the output to  $V_{CCIO}$  level.

#### Bus Hold

Each MAX 7000B device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signals is present, the bus-hold feature can eliminate the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than  $V_{CCIO}$  to prevent overdriving signals. The propagation delays through the input and output buffers in MAX 7000B devices are not affected by whether the bus-hold feature is enabled or disabled.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance ( $R_{BH}$ ) of approximately 8.5 k<sup>3</sup>/<sub>4</sub>. Table 12 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each VCCIO voltage level.

Table 12. Bus Hold Parameters										
Parameter	Conditions		VCCIO Level					Units		
		1.8	8 V	2.5 V		2.5 V 3.3 V		3.3 V		
		Min	Max	Min	Max	Min	Max			
Low sustaining current	V <sub>IN</sub> > V <sub>IL</sub> (max)	30		50		70		μA		
High sustaining current	V <sub>IN</sub> < V <sub>IH</sub> (min)	-30		-50		-70		μΑ		
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		200		300		500	μA		
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		-295		-435		-680	μΑ		

The bus-hold circuitry is active only during user operation. At power-up, the bus-hold circuit initializes its initial hold value as  $V_{CC}$  approaches the recommended operation conditions. When transitioning from ISP to User Mode with bus hold enabled, the bus-hold circuit captures the value present on the pin at the end of programming.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

#### Figure 10. Bus-Hold Circuit



# PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2* except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing     Specifications									
Device	Specif	ication							
	33-MHz PCI	66-MHz PCI							
EPM7032B	All speed grades	-3							
EPM7064B	All speed grades	-3							
EPM7128B	All speed grades	-4							
EPM7256B	All speed grades	-5 (1)							
EPM7512B	All speed grades	-5 (1)							

#### Note:

(1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

• • •	<b>-</b> .	<b>a</b>			
Symbol	Parameter	Conditions	IVIIN	Max	Unit
V <sub>IH</sub>	High-level input voltage for 3.3-V TTL/CMOS		2.0	3.9	V
	High-level input voltage for 2.5-V TTL/CMOS		1.7	3.9	V
	High-level input voltage for 1.8-V TTL/CMOS		$0.65 \times V_{CCIO}$	3.9	V
V <sub>IL</sub>	Low-level input voltage for 3.3-V TTL/CMOS and PCI compliance		-0.5	0.8	V
	Low-level input voltage for 2.5-V TTL/CMOS		-0.5	0.7	V
	Low-level input voltage for 1.8-V TTL/CMOS		-0.5	$0.35 \times V_{CCIO}$	
V <sub>OH</sub>	3.3-V high-level TTL output voltage	$I_{OH} = -8 \text{ mA DC}, V_{CCIO} = 3.00 \text{ V} (5)$	2.4		V
V <sub>OH</sub>	3.3-V high-level CMOS output voltage	$I_{OH}$ = -0.1 mA DC, $V_{CCIO}$ = 3.00 V (5)	V <sub>CCIO</sub> - 0.2		V
	2.5-V high-level output voltage	$I_{OH}$ = -100 µA DC, $V_{CCIO}$ = 2.30 V (5)	2.1		V
		$I_{OH} = -1 \text{ mA DC}, V_{CCIO} = 2.30 \text{ V} (5)$	2.0		V
		$I_{OH} = -2 \text{ mA DC}, V_{CCIO} = 2.30 \text{ V} (5)$	1.7		V
VIH     High TTL High TTL       VIH     High TTL       VIL     Low TTL       VIL     Low TTL       VOH     3.3-'       VOH     3.3-'       VOH     3.3-'       VOH     3.3-'       VOH     3.3-'       I.8-'     1.8-'       VOL     3.3-'       I.8-'     1.8-'       I.9-     1.8-'       I.0-     1.8-'       I.18-'     1.8-'       VOL     3.3-'       VOL     1.8-'  ILI     Input  <	1.8-V high-level output voltage	$I_{OH} = -2 \text{ mA DC}, V_{CCIO} = 1.65 \text{ V} (5)$	1.2		V
V <sub>OL</sub>	3.3-V low-level TTL output voltage	I <sub>OL</sub> = 8 mA DC, V <sub>CCIO</sub> = 3.00 V (6)		0.4	V
	3.3-V low-level CMOS output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (6)		0.2	V
	2.5-V low-level output voltage	$I_{OL}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V (6)		0.2	V
		$I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V (6)		0.4	V
		I <sub>OL</sub> = 2 mA DC, V <sub>CCIO</sub> = 2.30 V (6)		0.7	V
	1.8-V low-level output voltage	I <sub>OL</sub> = 2 mA DC, V <sub>CCIO</sub> = 1.7 V (6)	$\begin{array}{ c c c c c c }\hline & & & & & & & & \\ \hline & & & & & & & \\ \hline & & & &$	V	
II.	Input leakage current	$V_1 = -0.5 \text{ to } 3.9 \text{ V} (7)$	-10	10	μΑ
I <sub>OZ</sub>	Tri-state output off-state current	$V_1 = -0.5 \text{ to } 3.9 \text{ V} (7)$	-10	10	μΑ
R <sub>ISP</sub>	Value of I/O pin pull-up resistor during in-system programming or during power up	V <sub>CCIO</sub> = 1.7 to 3.6 V (8)	20	74	k¾

Table 1	Table 17. MAX 7000B Device Capacitance Note (9)								
Symbol	Parameter	Conditions	Min	Max	Unit				
C <sub>IN</sub>	Input pin capacitance	V <sub>IN</sub> = 0 V, f = 1.0 MHz		8	pF				
C <sub>I/O</sub>	I/O pin capacitance	V <sub>OUT</sub> = 0 V, f = 1.0 MHz		8	pF				

#### Notes to tables:

- (1) See the Operating Requirements for Altera Devices Data Sheet.
- (2) Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V<sub>CCINT</sub> and V<sub>CCIO</sub> are powered.
- (4) These values are specified under the Recommended Operating Conditions in Table 15 on page 29.
- (5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I<sub>OH</sub> parameter refers to high-level TTL or CMOS output current.
- (6) The parameter is measured with 50% of the outputs each sinking the specified current. The I<sub>OL</sub> parameter refers to low-level TTL or CMOS output current.
- (7) This value is specified for normal device operation. During power-up, the maximum leakage current is  $\pm 300 \,\mu$ A.
- (8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V<sub>CCIO</sub>.
- (9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (OE1 and GCLRN) have a maximum capacitance of 15 pF.
- (10) The POR time for all 7000B devices does not exceed 100 μs. The sufficient V<sub>CCINT</sub> voltage level for POR is 2.375 V. The device is fully initialized within the POR time after V<sub>CCINT</sub> reaches the sufficient POR voltage level.
- (11) These devices support in-system programming for -40° to 100° C. For in-system programming support between -40° and 0° C, contact Altera Applications.

## Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.



See *Application Note 94* (*Understanding MAX 7000 Timing*) for more information.

Table 22.	EPM7064B Internal Timing	Parameters	Note (	1)					
Symbol	Parameter	Conditions	Speed Grade						Unit
			-	3	-	5	-	7	
			Min	Max	Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay			0.3		0.5		0.7	ns
t <sub>IO</sub>	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t <sub>FIN</sub>	Fast input delay			0.9		1.3		2.0	ns
t <sub>FIND</sub>	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t <sub>SEXP</sub>	Shared expander delay			1.5		2.1		3.2	ns
t <sub>PEXP</sub>	Parallel expander delay			0.4		0.6		0.9	ns
t <sub>LAD</sub>	Logic array delay			1.4		2.0		3.1	ns
t <sub>LAC</sub>	Logic control array delay			1.2		1.7		2.6	ns
t <sub>IOE</sub>	Internal output enable delay			0.1		0.2		0.3	ns
t <sub>OD1</sub>	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3 \text{ V}$	C1 = 35 pF		0.9		1.2		1.8	ns
t <sub>OD3</sub>	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		5.9		6.2		6.8	ns
t <sub>ZX1</sub>	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		1.6		2.2		3.4	ns
t <sub>ZX3</sub>	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		6.6		7.2		8.4	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		1.6		2.2		3.4	ns
t <sub>SU</sub>	Register setup time		0.7		1.1		1.6		ns
t <sub>H</sub>	Register hold time		0.4		0.5		0.9		ns
t <sub>FSU</sub>	Register setup time of fast input		0.8		0.8		1.1		ns
t <sub>FH</sub>	Register hold time of fast input		1.2		1.2		1.4		ns
t <sub>RD</sub>	Register delay			0.5		0.6		0.9	ns
t <sub>COMB</sub>	Combinatorial delay			0.2		0.3		0.5	ns
t <sub>IC</sub>	Array clock delay			1.2		1.8		2.8	ns
t <sub>EN</sub>	Register enable time			1.2		1.7		2.6	ns
t <sub>GLOB</sub>	Global control delay			0.7		1.1		1.6	ns
t <sub>PRE</sub>	Register preset time			1.0		1.3		1.9	ns
t <sub>CLR</sub>	Register clear time			1.0		1.3		1.9	ns
t <sub>PIA</sub>	PIA delay	(2)		0.7		1.0		1.4	ns
t <sub>LPA</sub>	Low-power adder	(4)		1.5		2.1		3.2	ns

I/O Standard	Parameter	Speed Grade						Unit
		-	4	-	7		10	
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.6		0.8	ns
	Input to global clock and clear		0.3		0.6		0.8	ns
	Input to fast input register		0.2		0.4		0.5	ns
1.8 V TTL/CMOS	All outputs		0.2		0.4		0.5	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.9		1.3	ns
	Input to global clock and clear		0.5		0.9		1.3	ns
	Input to fast input register		0.4		0.8		1.0	ns
	All outputs		1.2		2.3		3.0	ns
SSTL-2 Class I	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		-0.1		-0.2		-0.3	ns
SSTL-3 Class I	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.7		3.2		4.3	ns
	Input to global clock and clear		1.7		3.2		4.3	ns
	Input to fast input register		1.6		3.0		4.0	ns
	All outputs		0.0		0.0		0.0	ns

Table 27	7. EPM7256B External Ti	ming Parameters	Note	(1)					
Symbol	Parameter	Conditions		Speed Grade					
			-	5	-	7	-1	10	
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	3.3		4.8		6.6		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		1.0		1.5		1.5		ns
t <sub>FH</sub>	Global clock hold time for fast input		1.0		1.0		1.0		ns
t <sub>FZHSU</sub>	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t <sub>FZHH</sub>	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.4		2.0		2.8		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.4		0.8		1.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	5.2	1.0	7.9	1.0	10.5	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t <sub>cnt</sub>	Minimum global clock period	(2)		5.3		7.9		10.6	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (3)	188.7		126.6		94.3		MHz
t <sub>acnt</sub>	Minimum array clock period	(2)		5.3		7.9		10.6	ns
facnt	Maximum internal array clock frequency	(2), (3)	188.7		126.6		94.3		MHz

Table 31.	EPM7512B Internal Timing	Parameters	Note (	1)					
Symbol	Parameter	Conditions	Speed Grade						Unit
			-	5	-	7	-	10	
			Min	Max	Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay			0.3		0.3		0.5	ns
t <sub>IO</sub>	I/O input pad and buffer delay			0.3		0.3		0.5	ns
t <sub>FIN</sub>	Fast input delay			2.2		3.2		4.0	ns
t <sub>FIND</sub>	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t <sub>SEXP</sub>	Shared expander delay			1.5		2.1		2.7	ns
t <sub>PEXP</sub>	Parallel expander delay			0.4		0.5		0.7	ns
t <sub>LAD</sub>	Logic array delay			1.7		2.3		3.0	ns
t <sub>LAC</sub>	Logic control array delay			1.5		2.0		2.6	ns
t <sub>IOE</sub>	Internal output enable delay			0.1		0.2		0.2	ns
t <sub>OD1</sub>	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.9		1.2		1.6	ns
t <sub>OD3</sub>	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.9		6.2		6.6	ns
t <sub>ZX1</sub>	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		2.8		3.8		5.0	ns
t <sub>ZX3</sub>	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		7.8		8.8		10.0	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		2.8		3.8		5.0	ns
t <sub>SU</sub>	Register setup time		1.5		2.0		2.6		ns
t <sub>H</sub>	Register hold time		0.4		0.5		0.7		ns
t <sub>FSU</sub>	Register setup time of fast input		0.8		1.1		1.1		ns
t <sub>FH</sub>	Register hold time of fast input		1.2		1.4		1.4		ns
t <sub>RD</sub>	Register delay			0.5		0.7		1.0	ns
t <sub>COMB</sub>	Combinatorial delay			0.2		0.3		0.4	ns
t <sub>IC</sub>	Array clock delay			1.8		2.4		3.1	ns
t <sub>EN</sub>	Register enable time			1.5		2.0		2.6	ns
t <sub>GLOB</sub>	Global control delay			2.0		2.8		3.6	ns
t <sub>PRE</sub>	Register preset time			1.0		1.4		1.9	ns
t <sub>CLR</sub>	Register clear time			1.0		1.4		1.9	ns
t <sub>PIA</sub>	PIA delay	(2)		2.4		3.4		4.5	ns
t <sub>LPA</sub>	Low-power adder	(4)		2.0		2.7		3.6	ns



Figure 19. I<sub>CC</sub> vs. Frequency for EPM7512B Devices

## Device Pin-Outs

See the Altera web site (http://www.altera.com) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.



Package outlines not drawn to scale.



#### Figure 23. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram





Package outline not drawn to scale.



#### Figure 28. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.

