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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

|                                 |   |
|---------------------------------|---|
| Product Status                  | Obsolete  |
| Programmable Type               | In System Programmable  |
| Delay Time tpd(1) Max           | 7.5 ns  |
| Voltage Supply - Internal       | 2.375V ~ 2.625V   |
| Number of Logic Elements/Blocks | 16  |
| Number of Macrocells            | 256   |
| Number of Gates                 | 5000  |
| Number of I/O                   | 84  |
| Operating Temperature           | -40°C ~ 85°C (TA)   |
| Mounting Type                   | Surface Mount   |
| Package / Case                  | 100-TQFP  |
| Supplier Device Package         | 100-TQFP (14x14)  |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/intel/epm7256bti100-7n">https://www.e-xfl.com/product-detail/intel/epm7256bti100-7n</a> |

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf)-capable in-circuit tester

## General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See [Table 2](#).

| <b>Table 2. MAX 7000B Speed Grades</b> <i>Note (1)</i> |             |    |    |    |     |
|--|-------------|----|----|----|-----|
| Device   | Speed Grade |    |    |    |     |
|  | -3          | -4 | -5 | -7 | -10 |
| EPM7032B   | ✓           |    | ✓  | ✓  |     |
| EPM7064B   | ✓           |    | ✓  | ✓  |     |
| EPM7128B   |             | ✓  |    | ✓  | ✓   |
| EPM7256B   |             |    | ✓  | ✓  | ✓   |
| EPM7512B   |             |    | ✓  | ✓  | ✓   |

### Notes:

- (1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See [Table 3](#).

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000B devices.

## Expander Product Terms

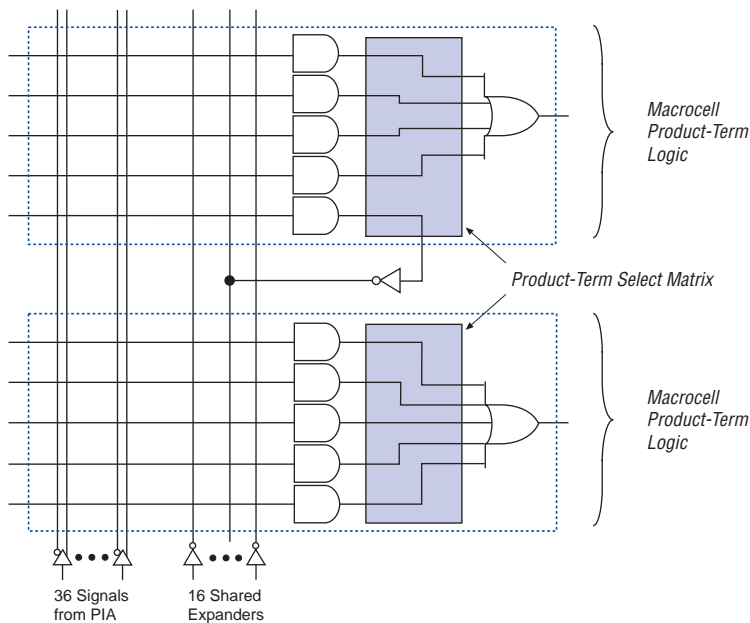
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. [Figure 3](#) shows how shareable expanders can feed multiple macrocells.

**Figure 3. MAX 7000B Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in a LAB.*



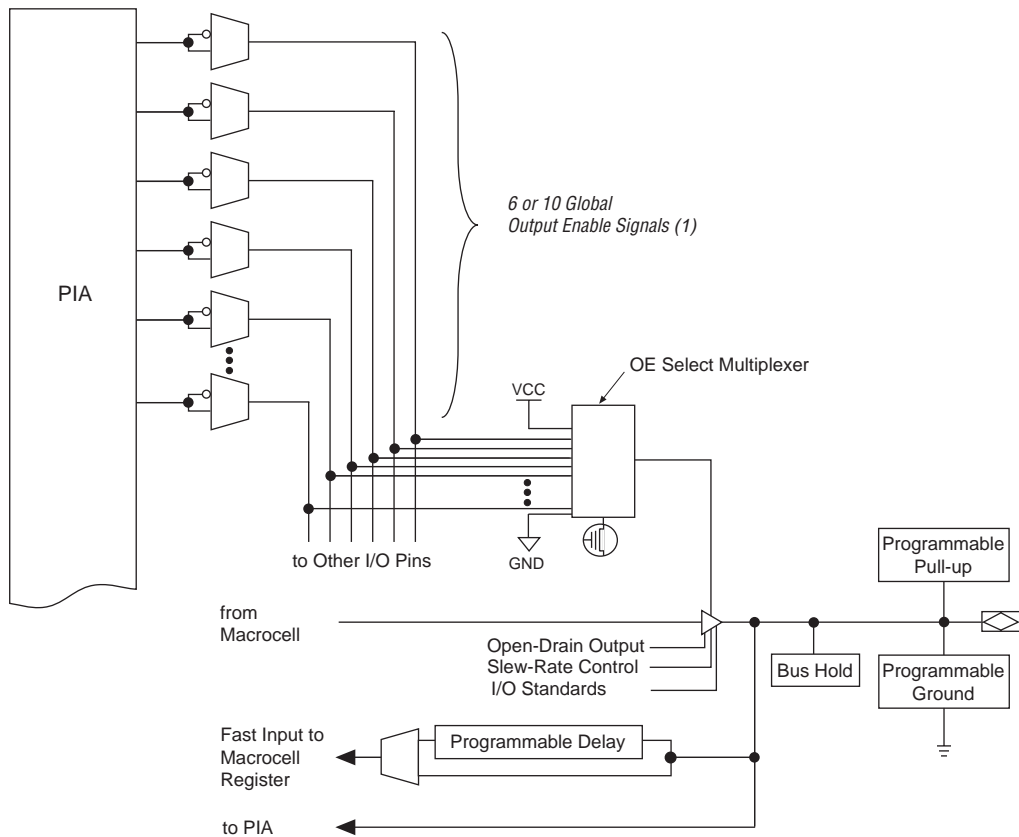
### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. I/O Control Block of MAX 7000B Devices

**Note:**

- (1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

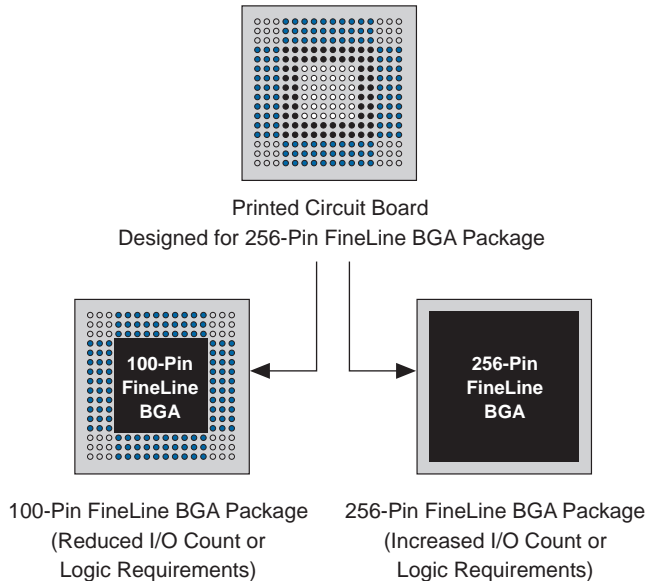
The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see [Figure 7](#)).

**Figure 7. SameFrame Pin-Out Example**



## In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k $\Omega$ .

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP\_Done bit that provides safe operation when in-system programming is interrupted. This ISP\_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam language, see [Application Note 88 \(Using the Jam Language for ISP & ICR via an Embedded Processor\)](#) and [Application Note 122 \(Using STAPL for ISP & ICR via an Embedded Processor\)](#).

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.



By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000B Device*

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

## Programming with External Hardware



MAX 7000B devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see [Programming Hardware Manufacturers](#).

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000B devices include the JTAG boundary-scan test circuitry defined by IEEE Std. 1149.1. [Table 6](#) describes the JTAG instructions supported by MAX 7000B devices. The pin-out tables starting on [page 59](#) of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

**Table 6. MAX 7000B JTAG Instructions**

| JTAG Instruction | Description   |
|------------------|---|
| SAMPLE/PRELOAD   | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.  |
| EXTEST           | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.  |
| BYPASS           | Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary-scan test data to pass synchronously through a selected device to adjacent devices during normal operation.  |
| CLAMP            | Allows the values in the boundary-scan register to determine pin states while placing the 1-bit bypass register between the TDI and TDO pins.   |
| IDCODE           | Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO.  |
| USERCODE         | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO.  |
| ISP Instructions | These instructions are used when programming MAX 7000B devices via the JTAG ports with the MasterBlaster or ByteBlasterMV download cable, or using a Jam File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf) via an embedded processor or test equipment. |

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. [Tables 7 and 8](#) show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

**Table 7. MAX 7000B Boundary-Scan Register Length**

| Device   | Boundary-Scan Register Length |
|----------|-------------------------------|
| EPM7032B | 96                            |
| EPM7064B | 192                           |
| EPM7128B | 288                           |
| EPM7256B | 480                           |
| EPM7512B | 624                           |

**Table 8. 32-Bit MAX 7000B Device IDCODE** *Note (1)*

| Device   | IDCODE (32 Bits) |                       |                                   |               |
|----------|------------------|-----------------------|-----------------------------------|---------------|
|          | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | 1 (1 Bit) (2) |
| EPM7032B | 0010             | 0111 0000 0011 0010   | 00001101110                       | 1             |
| EPM7064B | 0010             | 0111 0000 0110 0100   | 00001101110                       | 1             |
| EPM7128B | 0010             | 0111 0001 0010 1000   | 00001101110                       | 1             |
| EPM7256B | 0010             | 0111 0010 0101 0110   | 00001101110                       | 1             |
| EPM7512B | 0010             | 0111 0101 0001 0010   | 00001101110                       | 1             |

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

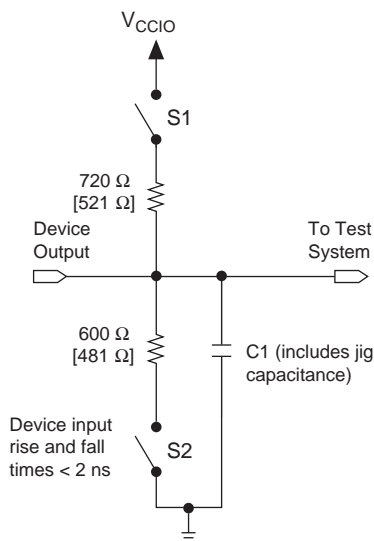


See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG boundary-scan testing.

[Figure 8](#) shows the timing information for the JTAG signals.

**Figure 11. MAX 7000B AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



## Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

**Table 14. MAX 7000B Device Absolute Maximum Ratings** *Note (1)*

| Symbol      | Parameter                  | Conditions | Min  | Max | Unit |
|-------------|----------------------------|------------|------|-----|------|
| $V_{CCINT}$ | Supply voltage             |            | -0.5 | 3.6 | V    |
| $V_{CCIO}$  | Supply voltage             |            | -0.5 | 3.6 | V    |
| $V_I$       | DC input voltage           | (2)        | -2.0 | 4.6 | V    |
| $I_{OUT}$   | DC output current, per pin |            | -33  | 50  | mA   |
| $T_{STG}$   | Storage temperature        | No bias    | -65  | 150 | °C   |
| $T_A$       | Ambient temperature        | Under bias | -65  | 135 | °C   |
| $T_J$       | Junction temperature       | Under bias | -65  | 135 | °C   |

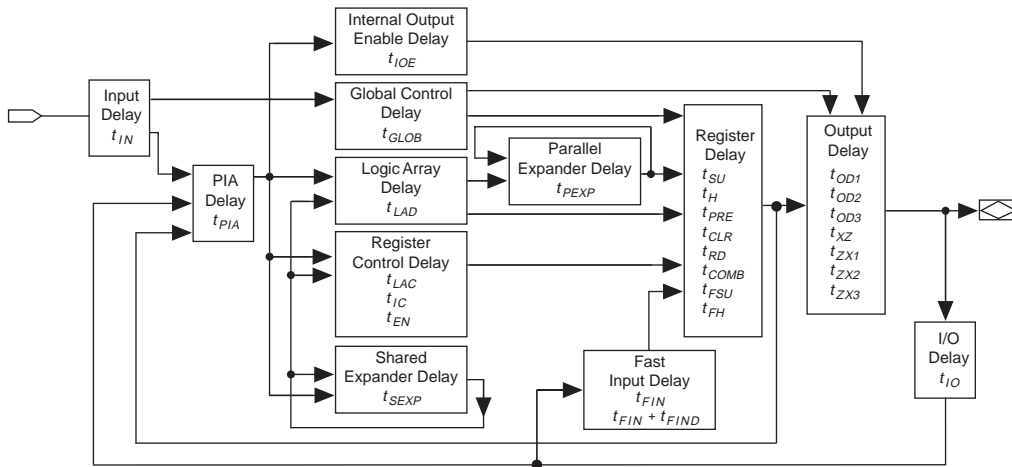
**Table 16. MAX 7000B Device DC Operating Conditions** *Note (4)*

| Symbol    | Parameter   | Conditions  | Min                    | Max                    | Unit          |
|-----------|---|---|------------------------|------------------------|---------------|
| $V_{IH}$  | High-level input voltage for 3.3-V TTL/CMOS                                       |   | 2.0                    | 3.9                    | V             |
|           | High-level input voltage for 2.5-V TTL/CMOS                                       |   | 1.7                    | 3.9                    | V             |
|           | High-level input voltage for 1.8-V TTL/CMOS                                       |   | $0.65 \times V_{CCIO}$ | 3.9                    | V             |
| $V_{IL}$  | Low-level input voltage for 3.3-V TTL/CMOS and PCI compliance                     |   | -0.5                   | 0.8                    | V             |
|           | Low-level input voltage for 2.5-V TTL/CMOS  |   | -0.5                   | 0.7                    | V             |
|           | Low-level input voltage for 1.8-V TTL/CMOS  |   | -0.5                   | $0.35 \times V_{CCIO}$ |               |
| $V_{OH}$  | 3.3-V high-level TTL output voltage   | $I_{OH} = -8 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (5)             | 2.4                    |                        | V             |
|           | 3.3-V high-level CMOS output voltage  | $I_{OH} = -0.1 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (5)           | $V_{CCIO} - 0.2$       |                        | V             |
|           | 2.5-V high-level output voltage   | $I_{OH} = -100 \text{ } \mu\text{A DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (5) | 2.1                    |                        | V             |
|           |   | $I_{OH} = -1 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (5)             | 2.0                    |                        | V             |
|           |   | $I_{OH} = -2 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (5)             | 1.7                    |                        | V             |
|           | 1.8-V high-level output voltage   | $I_{OH} = -2 \text{ mA DC}$ , $V_{CCIO} = 1.65 \text{ V}$ (5)             | 1.2                    |                        | V             |
| $V_{OL}$  | 3.3-V low-level TTL output voltage  | $I_{OL} = 8 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (6)              |                        | 0.4                    | V             |
|           | 3.3-V low-level CMOS output voltage   | $I_{OL} = 0.1 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (6)            |                        | 0.2                    | V             |
|           | 2.5-V low-level output voltage  | $I_{OL} = 100 \text{ } \mu\text{A DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (6)  |                        | 0.2                    | V             |
|           |   | $I_{OL} = 1 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (6)              |                        | 0.4                    | V             |
|           |   | $I_{OL} = 2 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (6)              |                        | 0.7                    | V             |
|           | 1.8-V low-level output voltage  | $I_{OL} = 2 \text{ mA DC}$ , $V_{CCIO} = 1.7 \text{ V}$ (6)               |                        | 0.4                    | V             |
| $I_I$     | Input leakage current   | $V_I = -0.5 \text{ to } 3.9 \text{ V}$ (7)                                | -10                    | 10                     | $\mu\text{A}$ |
| $I_{OZ}$  | Tri-state output off-state current  | $V_I = -0.5 \text{ to } 3.9 \text{ V}$ (7)                                | -10                    | 10                     | $\mu\text{A}$ |
| $R_{ISP}$ | Value of I/O pin pull-up resistor during in-system programming or during power up | $V_{CCIO} = 1.7 \text{ to } 3.6 \text{ V}$ (8)                            | 20                     | 74                     | $k\Omega$     |

## Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 13](#). MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

**Figure 13. MAX 7000B Timing Model**



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. [Figure 14](#) shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

**Table 19. EPM7032B Internal Timing Parameters** *Notes (1)*

| Symbol     | Parameter   | Conditions          | Speed Grade |     |      |     |      |     | Unit |
|------------|---|---------------------|-------------|-----|------|-----|------|-----|------|
|            |   |                     | -3.5        |     | -5.0 |     | -7.5 |     |      |
|            |   |                     | Min         | Max | Min  | Max | Min  | Max |      |
| $t_{IN}$   | Input pad and buffer delay  |                     |             | 0.3 |      | 0.5 |      | 0.7 | ns   |
| $t_{IO}$   | I/O input pad and buffer delay  |                     |             | 0.3 |      | 0.5 |      | 0.7 | ns   |
| $t_{FIN}$  | Fast input delay  |                     |             | 0.9 |      | 1.3 |      | 2.0 | ns   |
| $t_{FIND}$ | Programmable delay adder for fast input   |                     |             | 1.0 |      | 1.5 |      | 1.5 | ns   |
| $t_{SEXP}$ | Shared expander delay   |                     |             | 1.5 |      | 2.1 |      | 3.2 | ns   |
| $t_{PEXP}$ | Parallel expander delay   |                     |             | 0.4 |      | 0.6 |      | 0.9 | ns   |
| $t_{LAD}$  | Logic array delay   |                     |             | 1.4 |      | 2.0 |      | 3.1 | ns   |
| $t_{LAC}$  | Logic control array delay   |                     |             | 1.2 |      | 1.7 |      | 2.6 | ns   |
| $t_{IOE}$  | Internal output enable delay  |                     |             | 0.1 |      | 0.2 |      | 0.3 | ns   |
| $t_{OD1}$  | Output buffer and pad delay<br>slow slew rate = off<br>$V_{CCIO} = 3.3\text{ V}$                  | $C1 = 35\text{ pF}$ |             | 0.9 |      | 1.2 |      | 1.8 | ns   |
| $t_{OD3}$  | Output buffer and pad delay<br>slow slew rate = on<br>$V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$ | $C1 = 35\text{ pF}$ |             | 5.9 |      | 6.2 |      | 6.8 | ns   |
| $t_{ZX1}$  | Output buffer enable delay<br>slow slew rate = off<br>$V_{CCIO} = 3.3\text{ V}$                   | $C1 = 35\text{ pF}$ |             | 1.6 |      | 2.2 |      | 3.4 | ns   |
| $t_{ZX3}$  | Output buffer enable delay<br>slow slew rate = on<br>$V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$  | $C1 = 35\text{ pF}$ |             | 6.6 |      | 7.2 |      | 8.4 | ns   |
| $t_{XZ}$   | Output buffer disable delay   | $C1 = 5\text{ pF}$  |             | 1.6 |      | 2.2 |      | 3.4 | ns   |
| $t_{SU}$   | Register setup time   |                     | 0.7         |     | 1.1  |     | 1.6  |     | ns   |
| $t_H$      | Register hold time  |                     | 0.4         |     | 0.5  |     | 0.9  |     | ns   |
| $t_{FSU}$  | Register setup time of fast input   |                     | 0.8         |     | 0.8  |     | 1.1  |     | ns   |
| $t_{FH}$   | Register hold time of fast input  |                     | 1.2         |     | 1.2  |     | 1.4  |     | ns   |
| $t_{RD}$   | Register delay  |                     |             | 0.5 |      | 0.6 |      | 0.9 | ns   |
| $t_{COMB}$ | Combinatorial delay   |                     |             | 0.2 |      | 0.3 |      | 0.5 | ns   |
| $t_{IC}$   | Array clock delay   |                     |             | 1.2 |      | 1.8 |      | 2.8 | ns   |
| $t_{EN}$   | Register enable time  |                     |             | 1.2 |      | 1.7 |      | 2.6 | ns   |
| $t_{GLOB}$ | Global control delay  |                     |             | 0.7 |      | 1.1 |      | 1.6 | ns   |
| $t_{PRE}$  | Register preset time  |                     |             | 1.0 |      | 1.3 |      | 1.9 | ns   |
| $t_{CLR}$  | Register clear time   |                     |             | 1.0 |      | 1.3 |      | 1.9 | ns   |
| $t_{PIA}$  | PIA delay   | (2)                 |             | 0.7 |      | 1.0 |      | 1.4 | ns   |
| $t_{LPA}$  | Low-power adder   | (4)                 |             | 1.5 |      | 2.1 |      | 3.2 | ns   |

Table 21. EPM7064B External Timing Parameters *Note (1)*

| Symbol             | Parameter   | Conditions     | Speed Grade |     |       |     |       |     | Unit |
|--------------------|---|----------------|-------------|-----|-------|-----|-------|-----|------|
|                    |   |                | -3          |     | -5    |     | -7    |     |      |
|                    |   |                | Min         | Max | Min   | Max | Min   | Max |      |
| t <sub>PD1</sub>   | Input to non-registered output                            | C1 = 35 pF (2) |             | 3.5 |       | 5.0 |       | 7.5 | ns   |
| t <sub>PD2</sub>   | I/O input to non-registered output                        | C1 = 35 pF (2) |             | 3.5 |       | 5.0 |       | 7.5 | ns   |
| t <sub>SU</sub>    | Global clock setup time                                   | (2)            | 2.1         |     | 3.0   |     | 4.5   |     | ns   |
| t <sub>H</sub>     | Global clock hold time                                    | (2)            | 0.0         |     | 0.0   |     | 0.0   |     | ns   |
| t <sub>FSU</sub>   | Global clock setup time of fast input                     |                | 1.0         |     | 1.0   |     | 1.5   |     | ns   |
| t <sub>FH</sub>    | Global clock hold time of fast input                      |                | 1.0         |     | 1.0   |     | 1.0   |     | ns   |
| t <sub>FZHSU</sub> | Global clock setup time of fast input with zero hold time |                | 2.0         |     | 2.5   |     | 3.0   |     | ns   |
| t <sub>FZHH</sub>  | Global clock hold time of fast input with zero hold time  |                | 0.0         |     | 0.0   |     | 0.0   |     | ns   |
| t <sub>CO1</sub>   | Global clock to output delay                              | C1 = 35 pF     | 1.0         | 2.4 | 1.0   | 3.4 | 1.0   | 5.0 | ns   |
| t <sub>CH</sub>    | Global clock high time                                    |                | 1.5         |     | 2.0   |     | 3.0   |     | ns   |
| t <sub>CL</sub>    | Global clock low time                                     |                | 1.5         |     | 2.0   |     | 3.0   |     | ns   |
| t <sub>ASU</sub>   | Array clock setup time                                    | (2)            | 0.9         |     | 1.3   |     | 1.9   |     | ns   |
| t <sub>AH</sub>    | Array clock hold time                                     | (2)            | 0.2         |     | 0.3   |     | 0.6   |     | ns   |
| t <sub>ACO1</sub>  | Array clock to output delay                               | C1 = 35 pF (2) | 1.0         | 3.6 | 1.0   | 5.1 | 1.0   | 7.6 | ns   |
| t <sub>ACH</sub>   | Array clock high time                                     |                | 1.5         |     | 2.0   |     | 3.0   |     | ns   |
| t <sub>ACL</sub>   | Array clock low time                                      |                | 1.5         |     | 2.0   |     | 3.0   |     | ns   |
| t <sub>CPPW</sub>  | Minimum pulse width for clear and preset                  |                | 1.5         |     | 2.0   |     | 3.0   |     | ns   |
| t <sub>CNT</sub>   | Minimum global clock period                               | (2)            |             | 3.3 |       | 4.7 |       | 7.0 | ns   |
| f <sub>CNT</sub>   | Maximum internal global clock frequency                   | (2), (3)       | 303.0       |     | 212.8 |     | 142.9 |     | MHz  |
| t <sub>ACNT</sub>  | Minimum array clock period                                | (2)            |             | 3.3 |       | 4.7 |       | 7.0 | ns   |
| f <sub>ACNT</sub>  | Maximum internal array clock frequency                    | (2), (3)       | 303.0       |     | 212.8 |     | 142.9 |     | MHz  |



**Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

| I/O Standard | Parameter                       | Speed Grade |     |     |     |     |     | Unit |
|--------------|---------------------------------|-------------|-----|-----|-----|-----|-----|------|
|              |                                 | -3          |     | -5  |     | -7  |     |      |
|              |                                 | Min         | Max | Min | Max | Min | Max |      |
| PCI          | Input to PIA                    |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
|              | Input to global clock and clear |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
|              | Input to fast input register    |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
|              | All outputs                     |             | 0.0 |     | 0.0 |     | 0.0 | ns   |

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{EXP}$  parameters for macrocells running in low-power mode.

Table 24. EPM7128B External Timing Parameters *Note (1)*

| Symbol             | Parameter   | Conditions     | Speed Grade |     |       |     |      |      | Unit |
|--------------------|---|----------------|-------------|-----|-------|-----|------|------|------|
|                    |   |                | -4          |     | -7    |     | -10  |      |      |
|                    |   |                | Min         | Max | Min   | Max | Min  | Max  |      |
| t <sub>PD1</sub>   | Input to non-registered output                            | C1 = 35 pF (2) |             | 4.0 |       | 7.5 |      | 10.0 | ns   |
| t <sub>PD2</sub>   | I/O input to non-registered output                        | C1 = 35 pF (2) |             | 4.0 |       | 7.5 |      | 10.0 | ns   |
| t <sub>SU</sub>    | Global clock setup time                                   | (2)            | 2.5         |     | 4.5   |     | 6.1  |      | ns   |
| t <sub>H</sub>     | Global clock hold time                                    | (2)            | 0.0         |     | 0.0   |     | 0.0  |      | ns   |
| t <sub>FSU</sub>   | Global clock setup time of fast input                     |                | 1.0         |     | 1.5   |     | 1.5  |      | ns   |
| t <sub>FH</sub>    | Global clock hold time of fast input                      |                | 1.0         |     | 1.0   |     | 1.0  |      | ns   |
| t <sub>FZHSU</sub> | Global clock setup time of fast input with zero hold time |                | 2.0         |     | 3.0   |     | 3.0  |      | ns   |
| t <sub>FZHH</sub>  | Global clock hold time of fast input with zero hold time  |                | 0.0         |     | 0.0   |     | 0.0  |      | ns   |
| t <sub>CO1</sub>   | Global clock to output delay                              | C1 = 35 pF     | 1.0         | 2.8 | 1.0   | 5.7 | 1.0  | 7.5  | ns   |
| t <sub>CH</sub>    | Global clock high time                                    |                | 1.5         |     | 3.0   |     | 4.0  |      | ns   |
| t <sub>CL</sub>    | Global clock low time                                     |                | 1.5         |     | 3.0   |     | 4.0  |      | ns   |
| t <sub>ASU</sub>   | Array clock setup time                                    | (2)            | 1.2         |     | 2.0   |     | 2.8  |      | ns   |
| t <sub>AH</sub>    | Array clock hold time                                     | (2)            | 0.2         |     | 0.7   |     | 0.9  |      | ns   |
| t <sub>ACO1</sub>  | Array clock to output delay                               | C1 = 35 pF (2) | 1.0         | 4.1 | 1.0   | 8.2 | 1.0  | 10.8 | ns   |
| t <sub>ACH</sub>   | Array clock high time                                     |                | 1.5         |     | 3.0   |     | 4.0  |      | ns   |
| t <sub>ACL</sub>   | Array clock low time                                      |                | 1.5         |     | 3.0   |     | 4.0  |      | ns   |
| t <sub>CPPW</sub>  | Minimum pulse width for clear and preset                  |                | 1.5         |     | 3.0   |     | 4.0  |      | ns   |
| t <sub>CNT</sub>   | Minimum global clock period                               | (2)            |             | 4.1 |       | 7.9 |      | 10.6 | ns   |
| f <sub>CNT</sub>   | Maximum internal global clock frequency                   | (2), (3)       | 243.9       |     | 126.6 |     | 94.3 |      | MHz  |
| t <sub>ACNT</sub>  | Minimum array clock period                                | (2)            |             | 4.1 |       | 7.9 |      | 10.6 | ns   |
| f <sub>ACNT</sub>  | Maximum internal array clock frequency                    | (2), (3)       | 243.9       |     | 126.6 |     | 94.3 |      | MHz  |

**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

| I/O Standard | Parameter                       | Speed Grade |     |     |     |     |     | Unit |
|--------------|---------------------------------|-------------|-----|-----|-----|-----|-----|------|
|              |                                 | -5          |     | -7  |     | -10 |     |      |
|              |                                 | Min         | Max | Min | Max | Min | Max |      |
| PCI          | Input to PIA                    |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
|              | Input to global clock and clear |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
|              | Input to fast input register    |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
|              | All outputs                     |             | 0.0 |     | 0.0 |     | 0.0 | ns   |

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$ , in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

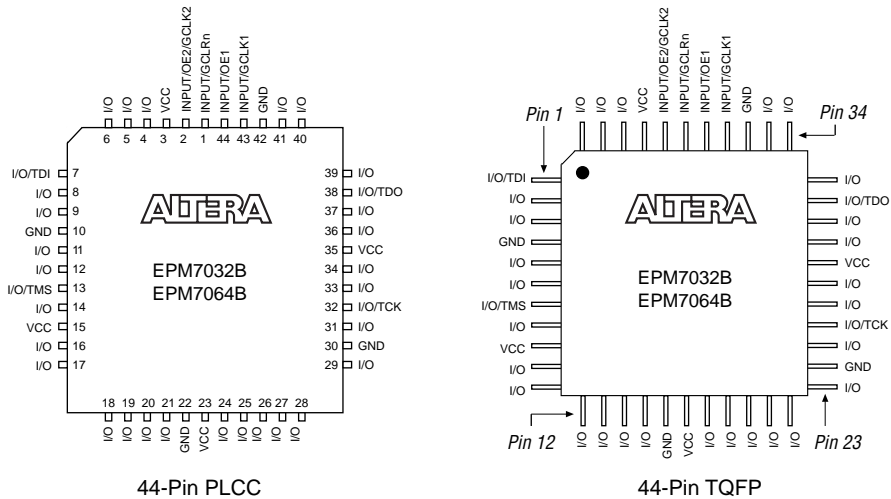
## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

**Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram**

*Package outlines not drawn to scale.*



**Figure 27. 208-Pin PQFP Package Pin-Out Diagram**

*Package outline not drawn to scale.*

