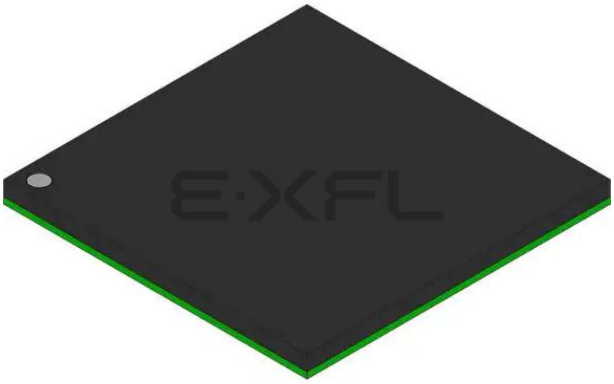
Altera - EPM7512BBC256-10 Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	10000
Number of I/O	212
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-BGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm7512bbc256-10

...and More Features

- System-level features
  - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
  - Programmable power-saving mode for 50% or greater power reduction in each macrocell
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
  - Bus-hold option on I/O pins
  - PCI compatible
  - Bus-friendly architecture including programmable slew-rate control
  - Open-drain output option
  - Programmable security bit for protection of proprietary designs
  - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
  - Supports hot-socketing operation
  - Programmable ground pins
- Advanced architecture features
  - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
  - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
  - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
  - Two global clock signals with optional inversion
  - Programmable power-up states for macrocell registers
  - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
  - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
  - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
  - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

  - Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
  - Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See Table 2.

Table 2. MAX 7000B Speed Grades *Note (1)*

Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

Notes:

(1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See Table 3.

Table 3. MAX 7000B Maximum User I/O Pins Note (1)

Device	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP *(2)*	49-Pin 0.8-mm Ultra FineLine BGA *(3)*	100-Pin TQFP	100-Pin FineLine BGA *(4)*	144-Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA *(3)*	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA *(4)*
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B				41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B							120	141	176	212	212

Notes:

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) Contact Altera for up-to-date information on available device package options.

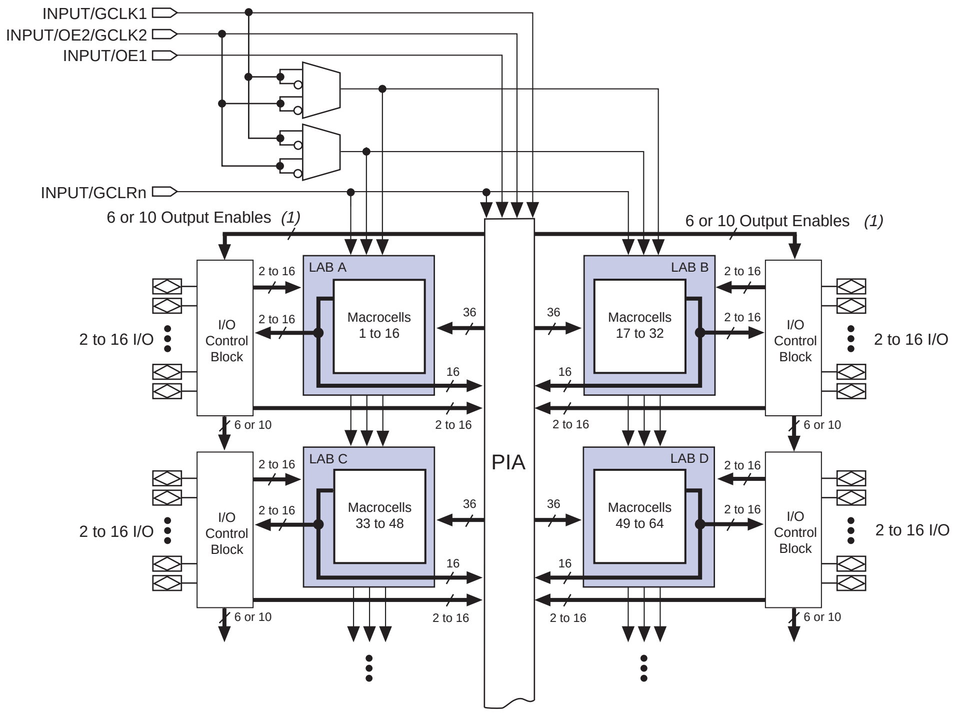
(3) All 0.8-mm Ultra FineLine BGA packages are footprint-compatible via the SameFrame$^{\text{TM}}$ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

(4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-`AND`/fixed-`OR` array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

Figure 1. MAX 7000B Device Block Diagram



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

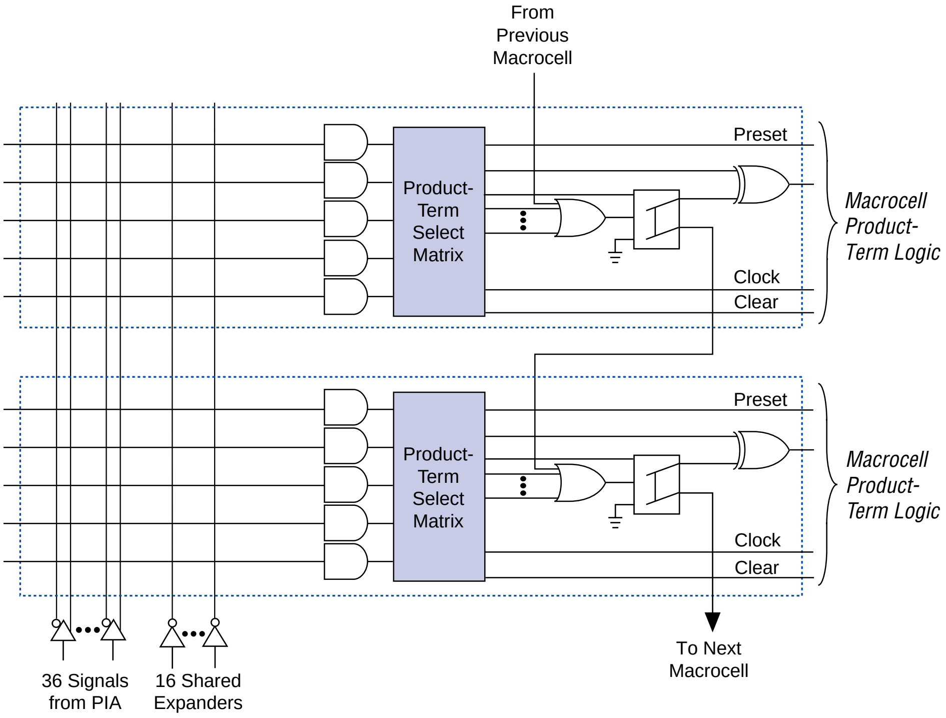
Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Figure 4. MAX 7000B Parallel Expanders

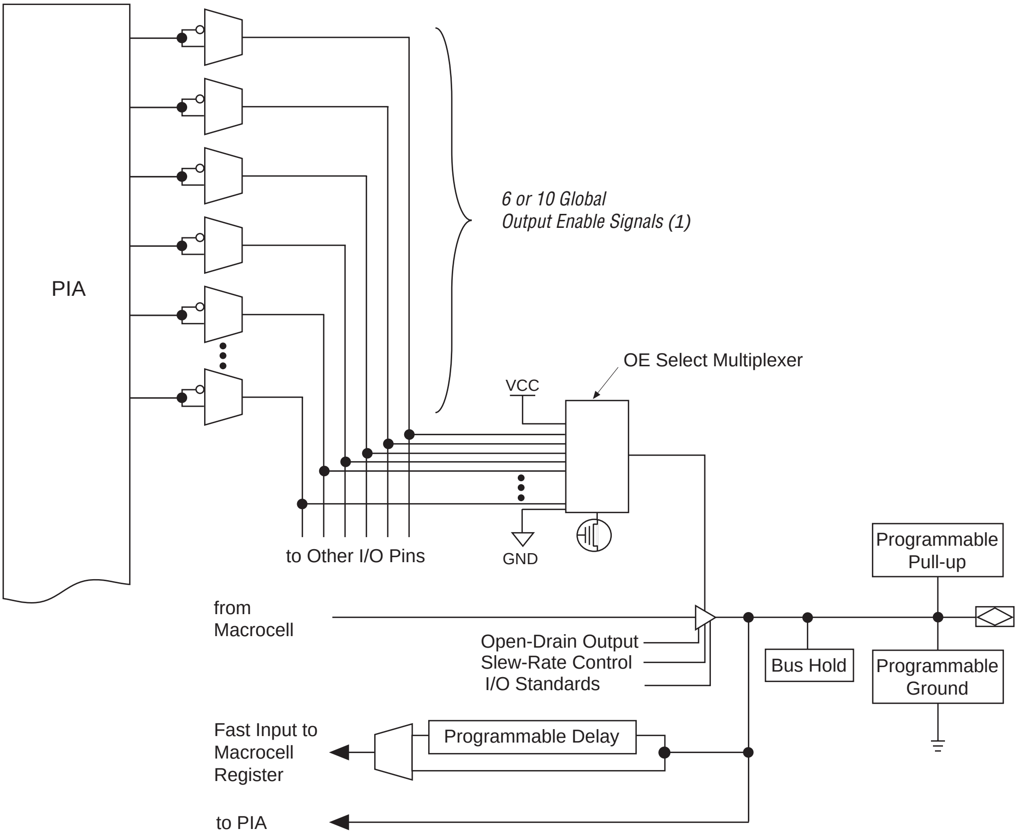
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 6. I/O Control Block of MAX 7000B Devices



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Programming with External Hardware

MAX 7000B devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000B devices include the JTAG boundary-scan test circuitry defined by IEEE Std. 1149.1. Table 6 describes the JTAG instructions supported by MAX 7000B devices. The pin-out tables starting on page 59 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 6. MAX 7000B JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary-scan test data to pass synchronously through a selected device to adjacent devices during normal operation.
CLAMP	Allows the values in the boundary-scan register to determine pin states while placing the 1-bit bypass register between the `TDI` and `TDO` pins.
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`.
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`.
ISP Instructions	These instructions are used when programming MAX 7000B devices via the JTAG ports with the MasterBlaster or ByteBlasterMV download cable, or using a Jam File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**) via an embedded processor or test equipment.

Figure 8. MAX 7000B JTAG Waveforms

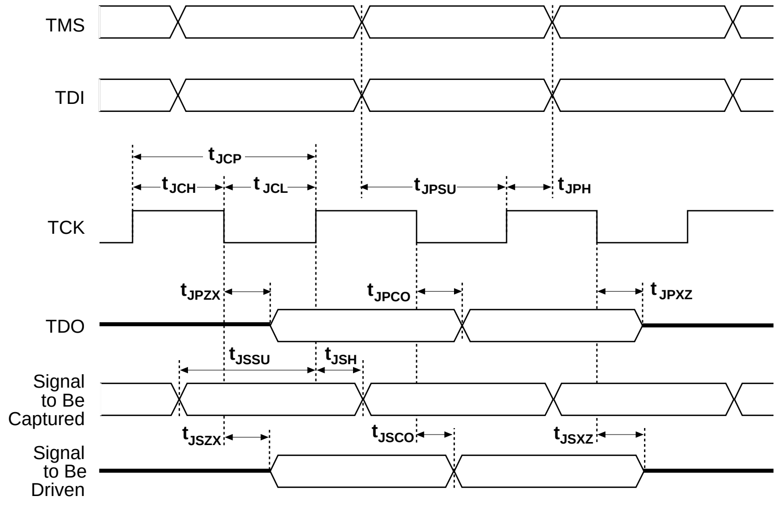


Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

Table 9. JTAG Timing Parameters & Values for MAX 7000B Devices
Note (1)

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Note:

(1) Timing parameters in this table apply to all V_{CCIO} levels.

Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

MAX 7000B device I/O pins will not source or sink more than 300 μA of DC current during power-up. All pins can be driven up to 4.1 V during hot-socketing.

Design Security

All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during early stages of the production flow.

Table 15. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(10)*	2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(3)*	–0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use *(11)*	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use *(11)*	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 17. MAX 7000B Device Capacitance *Note (9)*

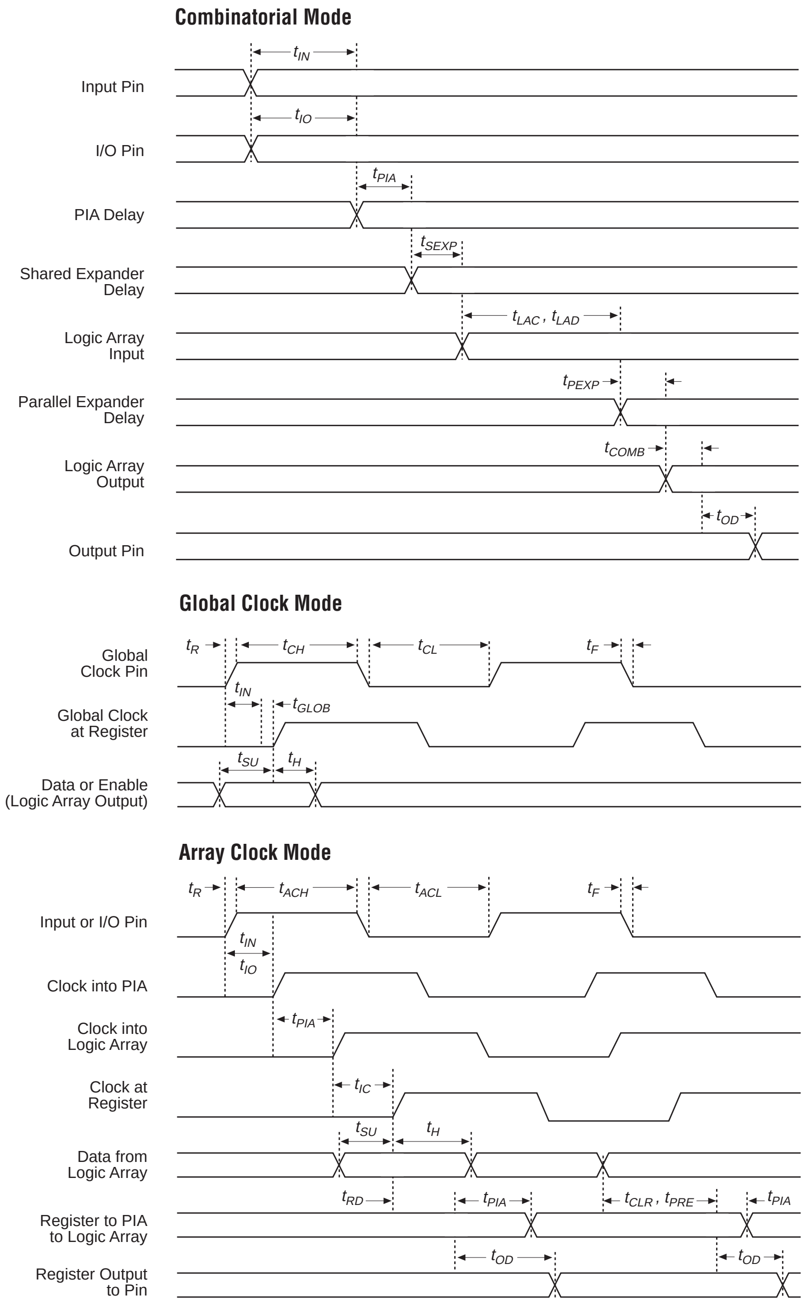
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(4) These values are specified under the Recommended Operating Conditions in Table 15 on page 29.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
(7) This value is specified for normal device operation. During power-up, the maximum leakage current is ±300 μA.
(8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V_{CCIO}.
(9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.
(10) The POR time for all 7000B devices does not exceed 100 µs. The sufficient V_{CCINT} voltage level for POR is 2.375 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

Figure 14. MAX 7000B Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Combinatorial Mode

Global Clock Mode

Array Clock Mode

Table 25. EPM7128B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.6		0.8	ns
t_{FIN}	Fast input delay			1.3		2.9		3.7	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.8		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.8		1.0	ns
t_{LAD}	Logic array delay			1.6		2.9		3.8	ns
t_{LAC}	Logic control array delay			1.4		2.6		3.4	ns
t_{IOE}	Internal output enable delay			0.1		0.3		0.4	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.7		2.2	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.7		7.2	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.8		3.3		4.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.8		8.3		9.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.8		3.3		4.4	ns
t_{SU}	Register setup time		1.0		1.9		2.6		ns
t_{H}	Register hold time		0.4		0.8		1.1		ns
t_{FSU}	Register setup time of fast input		0.8		0.9		0.9		ns
t_{FH}	Register hold time of fast input		1.2		1.6		1.6		ns
t_{RD}	Register delay			0.5		1.1		1.4	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.4		2.8		3.6	ns
t_{EN}	Register enable time			1.4		2.6		3.4	ns
t_{GLOB}	Global control delay			1.1		2.3		3.1	ns
t_{PRE}	Register preset time			1.0		1.9		2.6	ns
t_{CLR}	Register clear time			1.0		1.9		2.6	ns
t_{PIA}	PIA delay	*(2)*		1.0		2.0		2.8	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.8		3.8	ns

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) Note (1)

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 30. EPM7512B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	3.6		4.9		6.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	5.0	1.0	6.7	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.4		1.9		2.5		ns
t_{AH}	Array clock hold time	*(2)*	0.5		0.6		0.8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.9	1.0	8.0	1.0	10.7	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		3.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		6.1		8.4		11.1	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	163.9		119.0		90.1		MHz
t_{ACNT}	Minimum array clock period	*(2)*		6.1		8.4		11.1	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	163.9		119.0		90.1		MHz

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

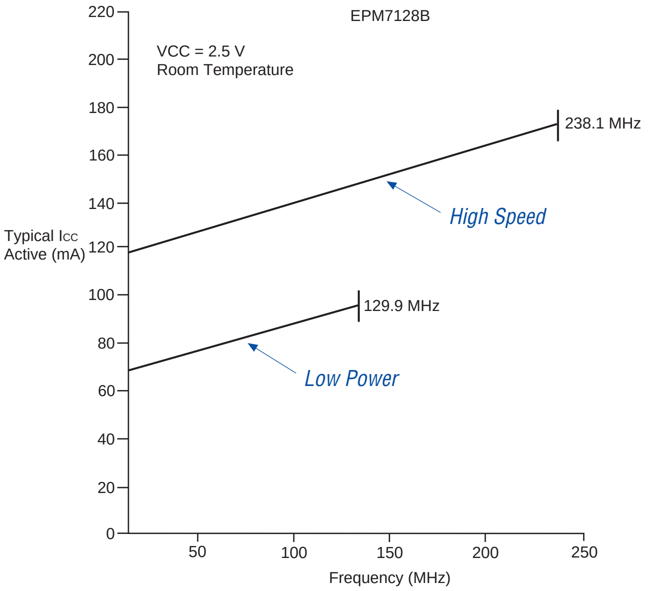


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices

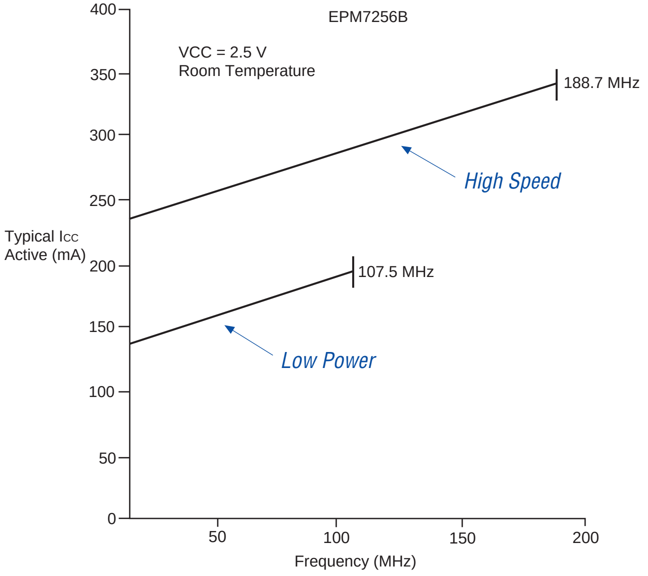


Figure 28. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.

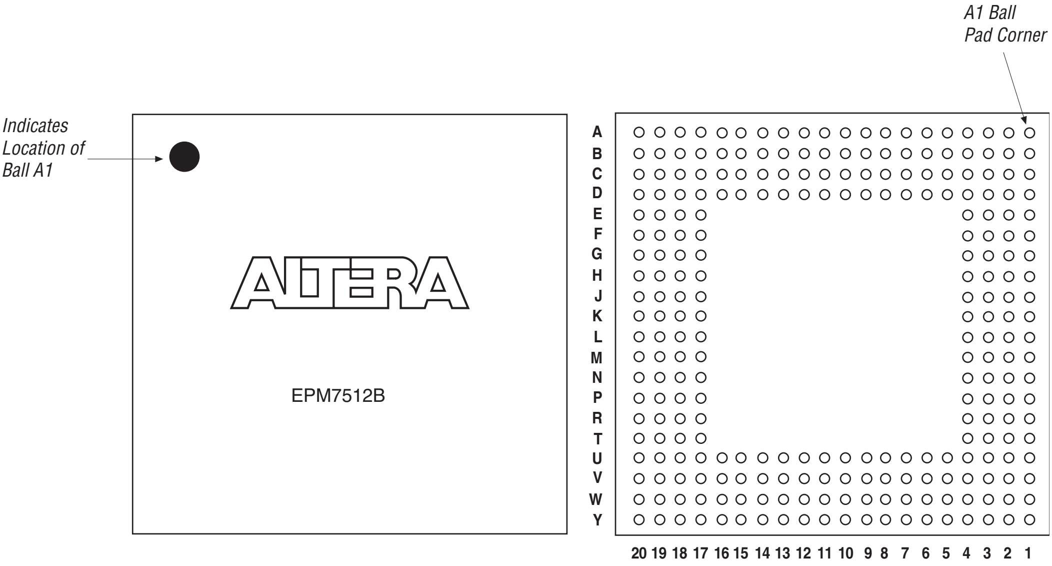
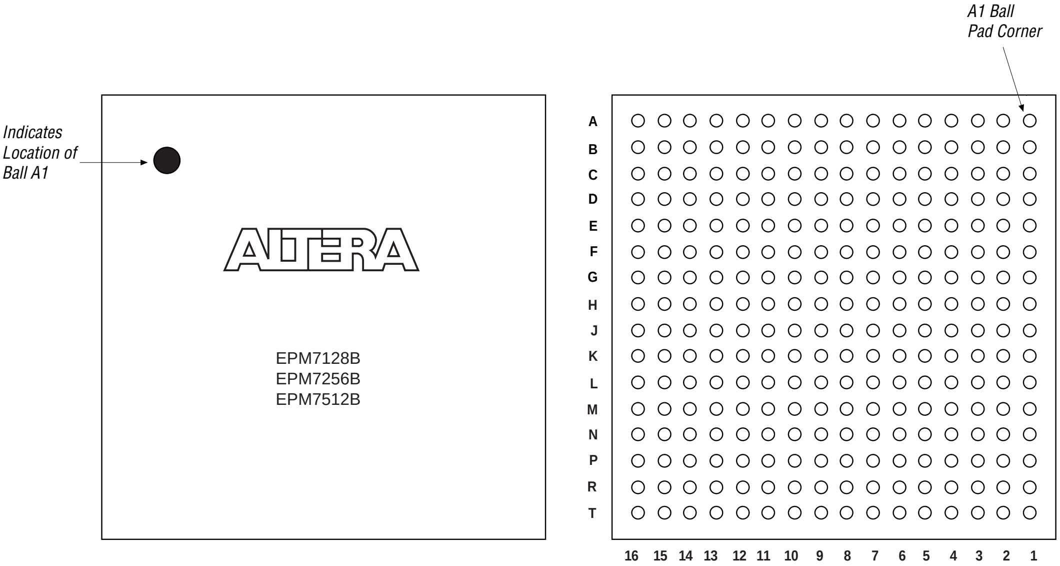


Figure 29. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.5 supersedes information published in previous versions.

Version 3.5

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.5:

- Updated Figure 28.

Version 3.4

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.4:

- Updated text in the “Power Sequencing & Hot-Socketing” section.