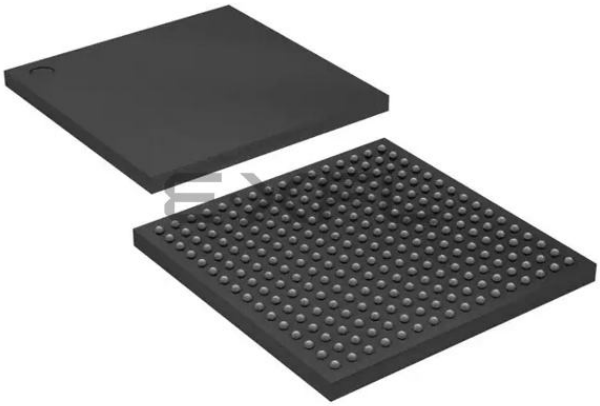


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	10000
Number of I/O	212
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7512bfi256-7

…and More Features

- System-level features
  - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
  - Programmable power-saving mode for 50% or greater power reduction in each macrocell
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
  - Bus-hold option on I/O pins
  - PCI compatible
  - Bus-friendly architecture including programmable slew-rate control
  - Open-drain output option
  - Programmable security bit for protection of proprietary designs
  - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
  - Supports hot-socketing operation
  - Programmable ground pins
- Advanced architecture features
  - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
  - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
  - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
  - Two global clock signals with optional inversion
  - Programmable power-up states for macrocell registers
  - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
  - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
  - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
  - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

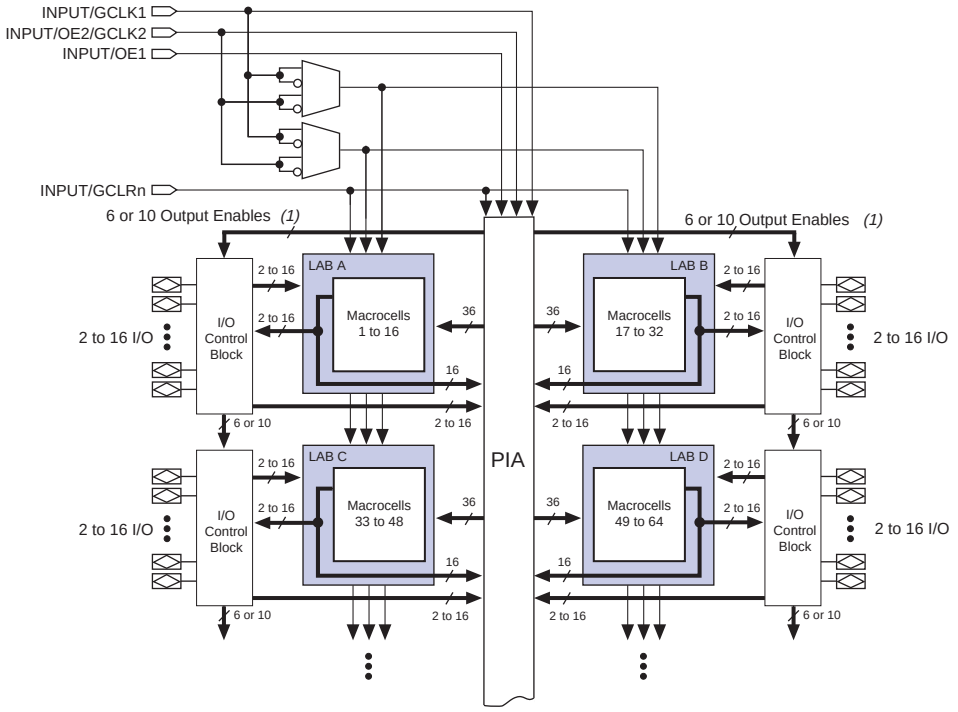
Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000B devices.

Figure 1. MAX 7000B Device Block Diagram



Note:
(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Expander Product Terms

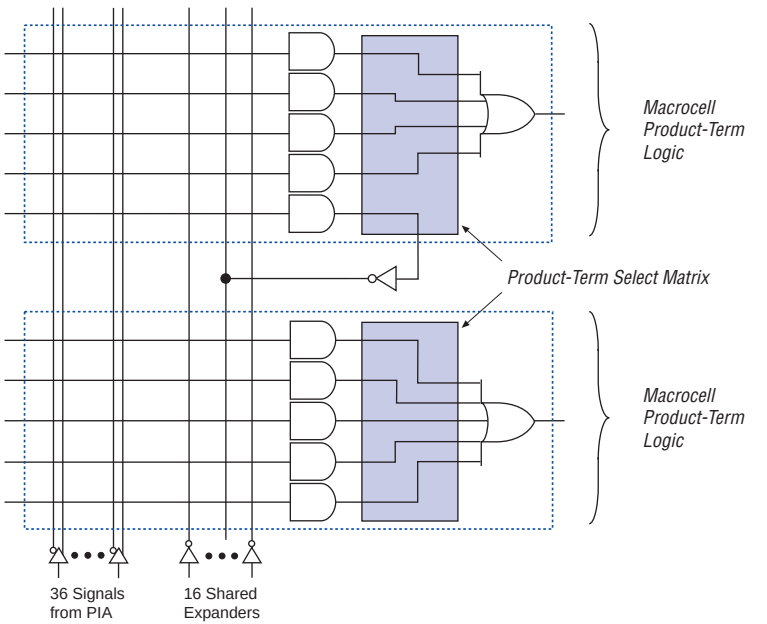
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000B Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

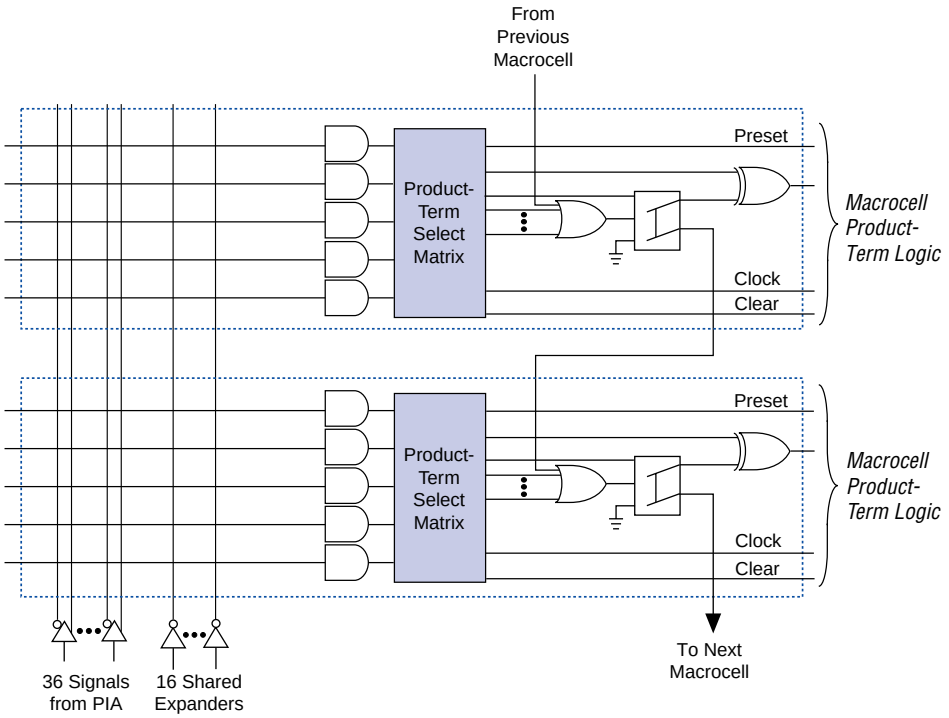
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000B Parallel Expanders

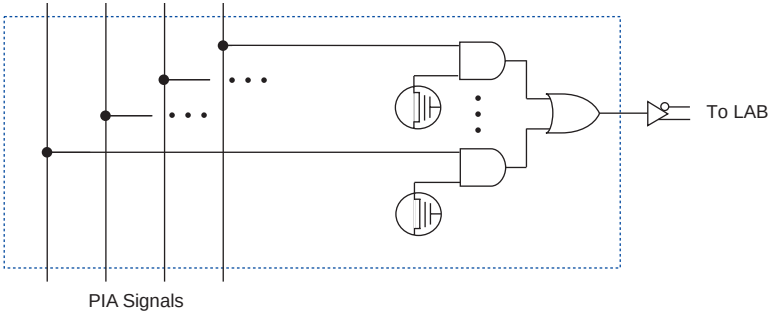
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000B PIA Routing



While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

MAX 7000B device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 4.1 V during hot-socketing.

Design Security

All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during early stages of the production flow.

Figure 14. MAX 7000B Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

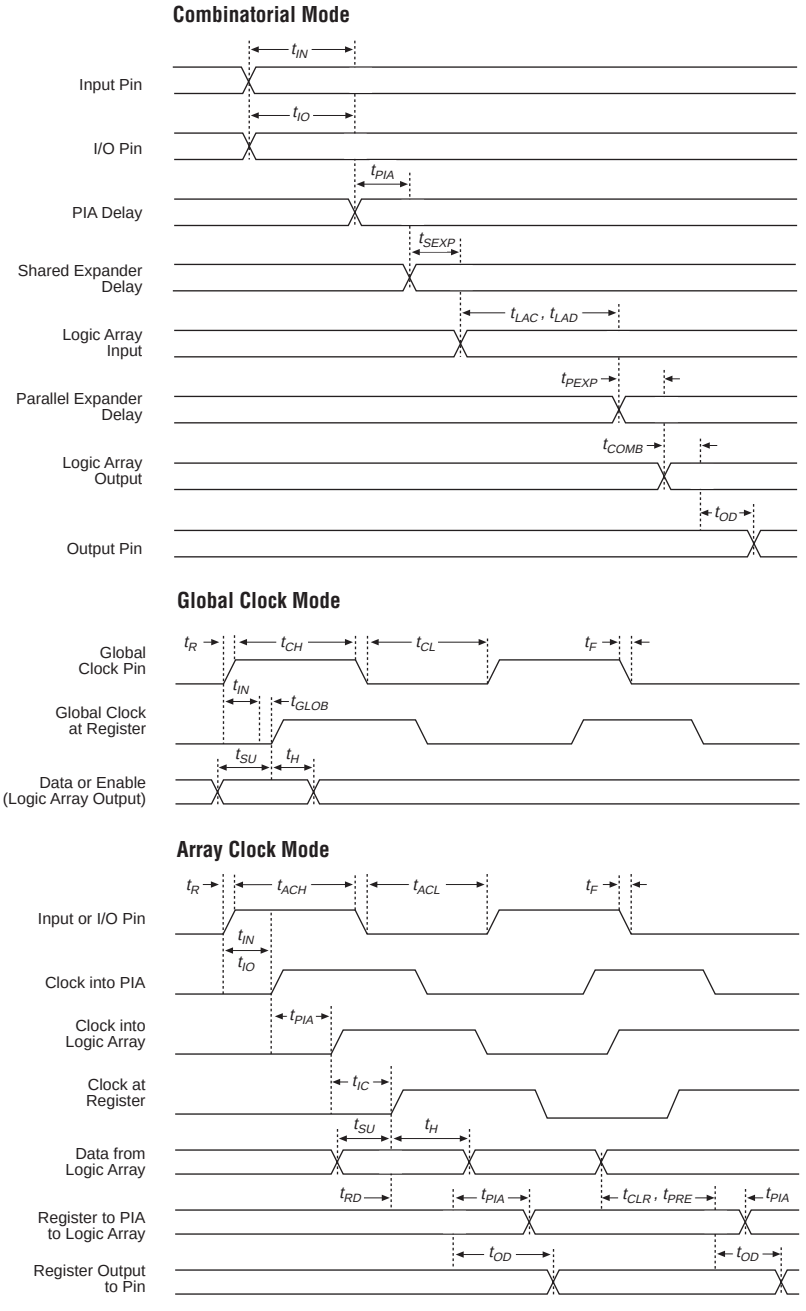


Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays *Notes (1)*								
I/O Standard	**Parameter**	**Speed Grade**						**Unit**
		-3.5		**-5.0**		**-7.5**		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of all LABs.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 25. EPM7128B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.6		0.8	ns
t_{FIN}	Fast input delay			1.3		2.9		3.7	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.8		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.8		1.0	ns
t_{LAD}	Logic array delay			1.6		2.9		3.8	ns
t_{LAC}	Logic control array delay			1.4		2.6		3.4	ns
t_{IOE}	Internal output enable delay			0.1		0.3		0.4	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.7		2.2	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.7		7.2	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.8		3.3		4.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.8		8.3		9.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.8		3.3		4.4	ns
t_{SU}	Register setup time		1.0		1.9		2.6		ns
t_{H}	Register hold time		0.4		0.8		1.1		ns
t_{FSU}	Register setup time of fast input		0.8		0.9		0.9		ns
t_{FH}	Register hold time of fast input		1.2		1.6		1.6		ns
t_{RD}	Register delay			0.5		1.1		1.4	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.4		2.8		3.6	ns
t_{EN}	Register enable time			1.4		2.6		3.4	ns
t_{GLOB}	Global control delay			1.1		2.3		3.1	ns
t_{PRE}	Register preset time			1.0		1.9		2.6	ns
t_{CLR}	Register clear time			1.0		1.9		2.6	ns
t_{PIA}	PIA delay	*(2)*		1.0		2.0		2.8	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.8		3.8	ns

Table 27. EPM7256B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	3.3		4.8		6.6		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.4		2.0		2.8		ns
t_{AH}	Array clock hold time	*(2)*	0.4		0.8		1.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.2	1.0	7.9	1.0	10.5	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.3		7.9		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	188.7		126.6		94.3		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.3		7.9		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	188.7		126.6		94.3		MHz

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		–0.1		–0.2		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

Table 31. EPM7512B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.3		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.3		0.5	ns
t_{FIN}	Fast input delay			2.2		3.2		4.0	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		2.7	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.7	ns
t_{LAD}	Logic array delay			1.7		2.3		3.0	ns
t_{LAC}	Logic control array delay			1.5		2.0		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.2	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.6	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		2.8		3.8		5.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		7.8		8.8		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.8		3.8		5.0	ns
t_{SU}	Register setup time		1.5		2.0		2.6		ns
t_{H}	Register hold time		0.4		0.5		0.7		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.5		0.7		1.0	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.8		2.4		3.1	ns
t_{EN}	Register enable time			1.5		2.0		2.6	ns
t_{GLOB}	Global control delay			2.0		2.8		3.6	ns
t_{PRE}	Register preset time			1.0		1.4		1.9	ns
t_{CLR}	Register clear time			1.0		1.4		1.9	ns
t_{PIA}	PIA delay	*(2)*		2.4		3.4		4.5	ns
t_{LPA}	Low-power adder	*(4)*		2.0		2.7		3.6	ns

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

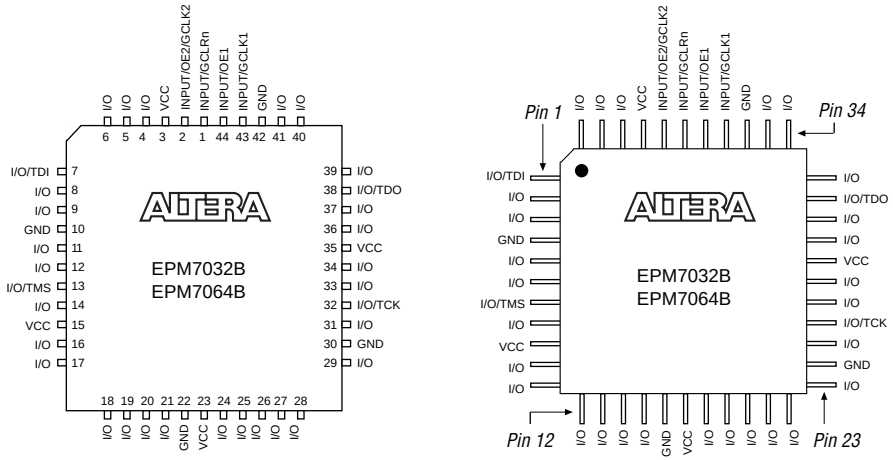
Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TQFP

Figure 25. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

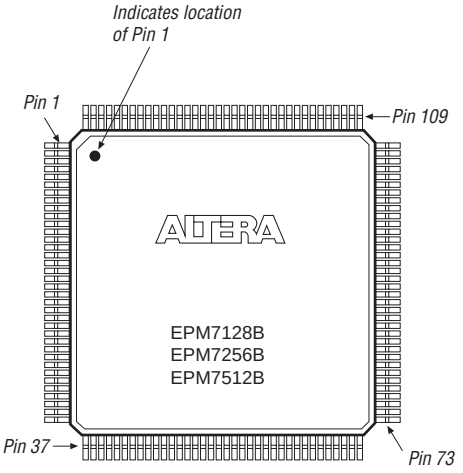


Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram

Package outline not drawn to scale.

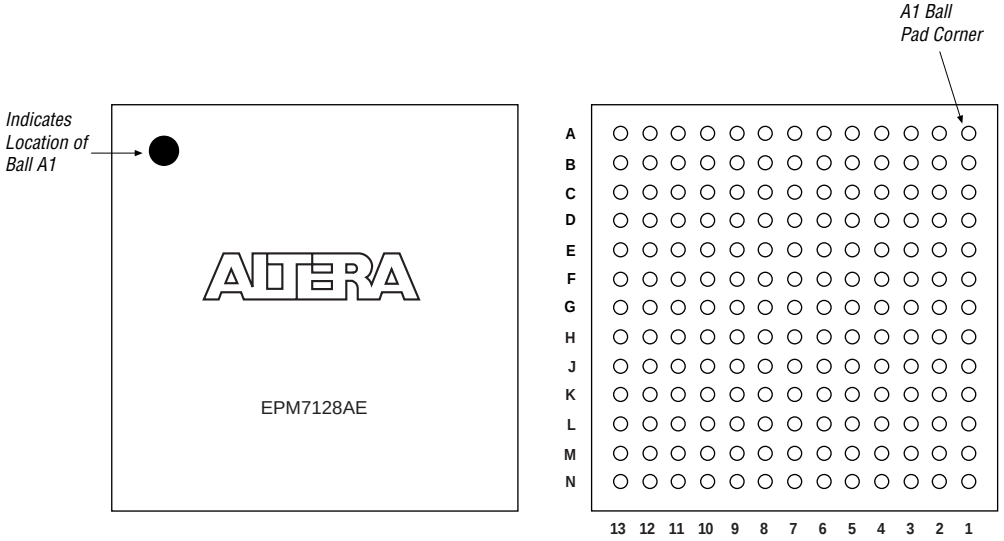


Figure 28. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.