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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	10000
Number of I/O	141
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-UBGA (11x11)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7512buc169-10">https://www.e-xfl.com/product-detail/intel/epm7512buc169-10</a>

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf)-capable in-circuit tester

## General Description

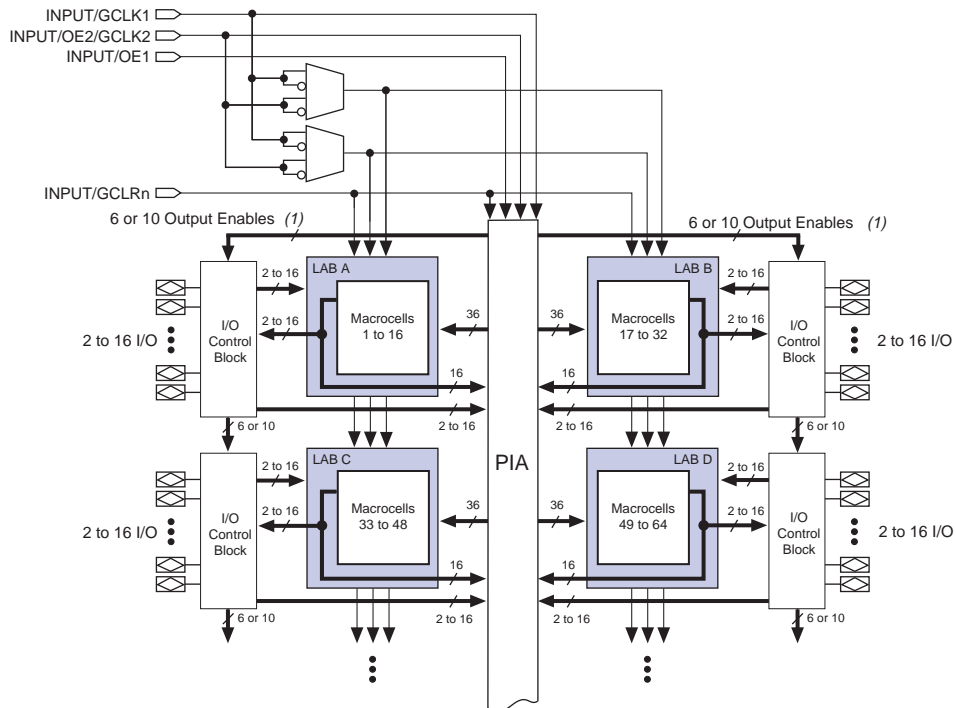
MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 303.0 MHz. See [Table 2](#).

<b>Table 2. MAX 7000B Speed Grades</b> <i>Note (1)</i>					
Device	Speed Grade				
	-3	-4	-5	-7	-10
EPM7032B	✓		✓	✓	
EPM7064B	✓		✓	✓	
EPM7128B		✓		✓	✓
EPM7256B			✓	✓	✓
EPM7512B			✓	✓	✓

### Notes:

- (1) Contact Altera Marketing for up-to-date information on available device speed grades.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and TQFP packages. See [Table 3](#).

**Figure 1. MAX 7000B Device Block Diagram****Note:**

- (1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

## Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in [Figure 1](#). Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

## Expander Product Terms

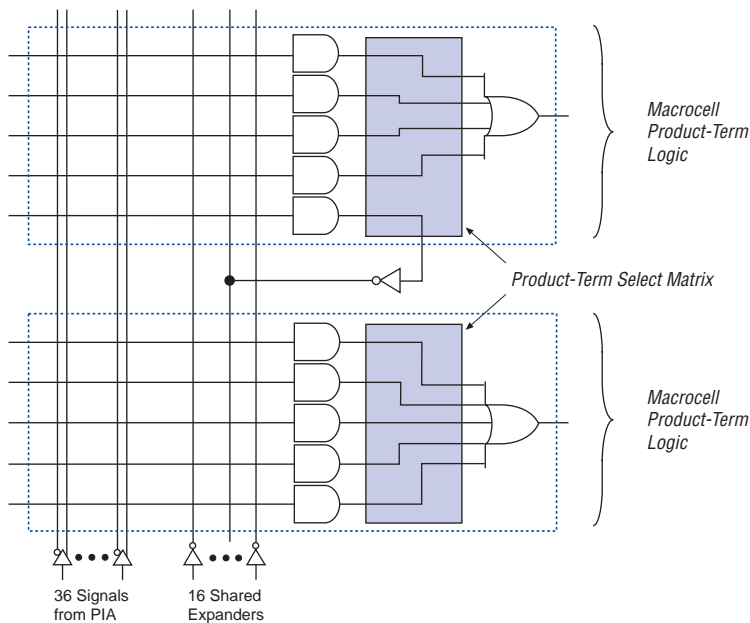
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. [Figure 3](#) shows how shareable expanders can feed multiple macrocells.

**Figure 3. MAX 7000B Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in a LAB.*



### *Parallel Expanders*

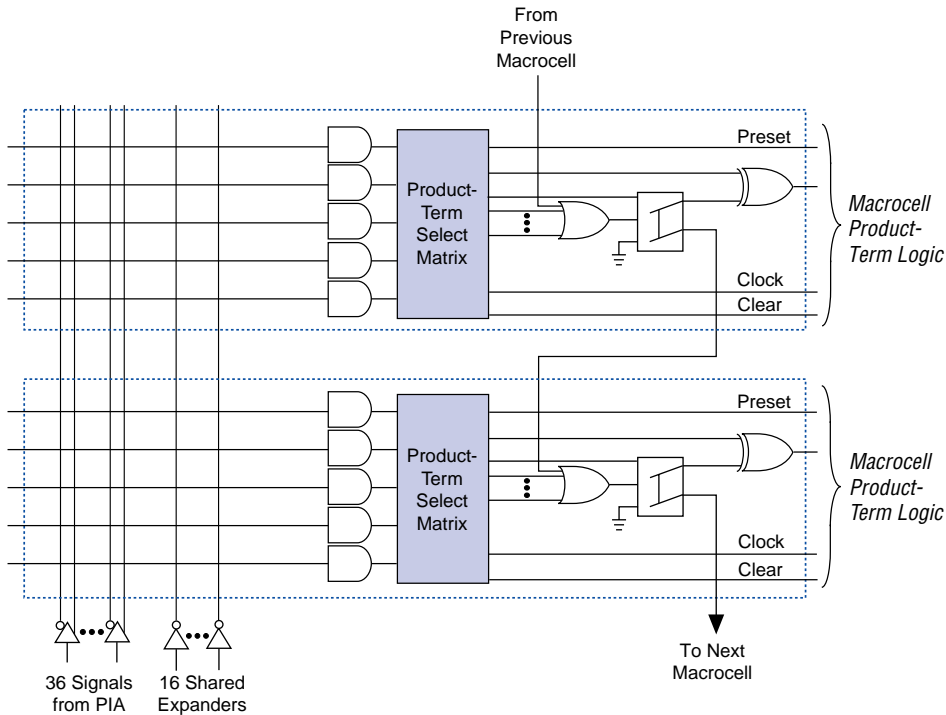
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

**Figure 4. MAX 7000B Parallel Expanders**

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



## Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

## In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k $\Omega$ .

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP\_Done bit that provides safe operation when in-system programming is interrupted. This ISP\_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam language, see [Application Note 88 \(Using the Jam Language for ISP & ICR via an Embedded Processor\)](#) and [Application Note 122 \(Using STAPL for ISP & ICR via an Embedded Processor\)](#).

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000B Device*

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device



The programming times described in [Tables 4 through 6](#) are associated with the worst-case method using the enhanced ISP algorithm.

**Table 4. MAX 7000B  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PPULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EMP7032B	2.12	70,000	0.002	18,000
EMP7064B	2.12	120,000	0.002	35,000
EMP7128B	2.12	222,000	0.002	69,000
EMP7256B	2.12	466,000	0.002	151,000
EMP7512B	2.12	914,000	0.002	300,000

[Tables 5 and 6](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 5. MAX 7000B In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	2.13	2.13	2.15	2.19	2.26	2.47	2.82	3.52	s
EMP7064B	2.13	2.14	2.18	2.24	2.36	2.72	3.32	4.52	s
EMP7128B	2.14	2.16	2.23	2.34	2.56	3.23	4.34	6.56	s
EMP7256B	2.17	2.21	2.35	2.58	3.05	4.45	6.78	11.44	s
EMP7512B	2.21	2.30	2.58	3.03	3.95	6.69	11.26	20.40	s

**Table 1. MAX 7000B Stand-Alone Verification Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EMP7064B	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EMP7128B	0.01	0.02	0.04	0.07	0.14	0.35	0.69	1.38	s
EMP7256B	0.02	0.03	0.08	0.15	0.30	0.76	1.51	3.02	s
EMP7512B	0.03	0.06	0.15	0.30	0.60	1.50	3.00	6.00	s

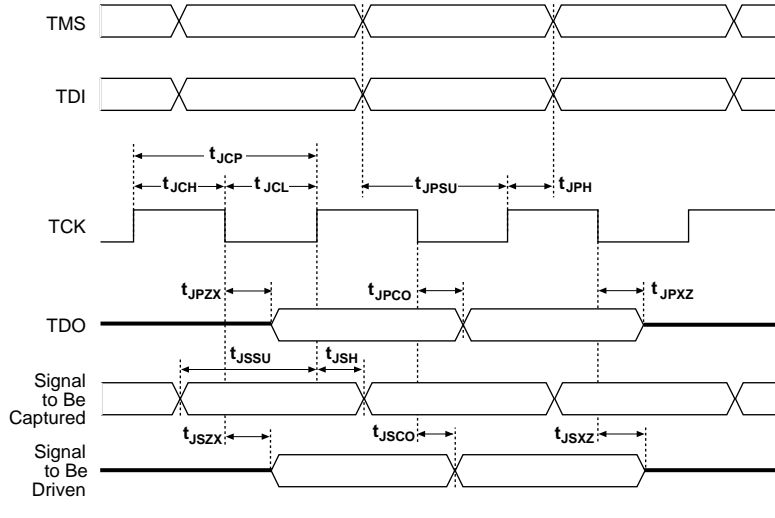
**Figure 8. MAX 7000B JTAG Waveforms**

Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

<b>Table 9. JTAG Timing Parameters &amp; Values for MAX 7000B Devices</b> <i>Note (1)</i>				
Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns

**Note:**

(1) Timing parameters in this table apply to all  $V_{CCIO}$  levels.

**Table 10. MAX 7000B MultiVolt I/O Support**

V <sub>CCIO</sub> (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

### Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

### Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

### Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

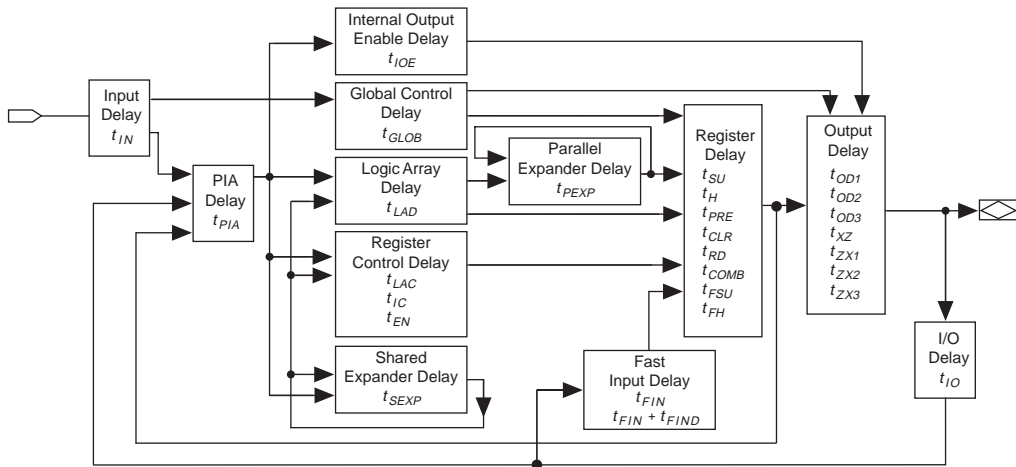
### Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

## Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 13](#). MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

**Figure 13. MAX 7000B Timing Model**



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. [Figure 14](#) shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

**Table 19. EPM7032B Internal Timing Parameters** *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.5		0.7	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.5		0.7	ns
$t_{FIN}$	Fast input delay			0.9		1.3		2.0	ns
$t_{FIND}$	Programmable delay adder for fast input			1.0		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.1		3.2	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.6		0.9	ns
$t_{LAD}$	Logic array delay			1.4		2.0		3.1	ns
$t_{LAC}$	Logic control array delay			1.2		1.7		2.6	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.3	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.8	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.8	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.6		2.2		3.4	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.6		7.2		8.4	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		1.6		2.2		3.4	ns
$t_{SU}$	Register setup time		0.7		1.1		1.6		ns
$t_H$	Register hold time		0.4		0.5		0.9		ns
$t_{FSU}$	Register setup time of fast input		0.8		0.8		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.2		1.4		ns
$t_{RD}$	Register delay			0.5		0.6		0.9	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.5	ns
$t_{IC}$	Array clock delay			1.2		1.8		2.8	ns
$t_{EN}$	Register enable time			1.2		1.7		2.6	ns
$t_{GLOB}$	Global control delay			0.7		1.1		1.6	ns
$t_{PRE}$	Register preset time			1.0		1.3		1.9	ns
$t_{CLR}$	Register clear time			1.0		1.3		1.9	ns
$t_{PIA}$	PIA delay	(2)		0.7		1.0		1.4	ns
$t_{LPA}$	Low-power adder	(4)		1.5		2.1		3.2	ns

**Table 22. EPM7064B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.5		0.7	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.5		0.7	ns
$t_{FIN}$	Fast input delay			0.9		1.3		2.0	ns
$t_{FIND}$	Programmable delay adder for fast input			1.0		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.1		3.2	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.6		0.9	ns
$t_{LAD}$	Logic array delay			1.4		2.0		3.1	ns
$t_{LAC}$	Logic control array delay			1.2		1.7		2.6	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.3	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.8	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.8	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.6		2.2		3.4	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.6		7.2		8.4	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		1.6		2.2		3.4	ns
$t_{SU}$	Register setup time		0.7		1.1		1.6		ns
$t_H$	Register hold time		0.4		0.5		0.9		ns
$t_{FSU}$	Register setup time of fast input		0.8		0.8		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.2		1.4		ns
$t_{RD}$	Register delay			0.5		0.6		0.9	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.5	ns
$t_{IC}$	Array clock delay			1.2		1.8		2.8	ns
$t_{EN}$	Register enable time			1.2		1.7		2.6	ns
$t_{GLOB}$	Global control delay			0.7		1.1		1.6	ns
$t_{PRE}$	Register preset time			1.0		1.3		1.9	ns
$t_{CLR}$	Register clear time			1.0		1.3		1.9	ns
$t_{PIA}$	PIA delay	(2)		0.7		1.0		1.4	ns
$t_{LPA}$	Low-power adder	(4)		1.5		2.1		3.2	ns

**Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.7		1.1	ns
	Input to global clock and clear		0.5		0.7		1.1	ns
	Input to fast input register		0.4		0.6		0.9	ns
	All outputs		1.2		1.7		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.6		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

**Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.



Table 27. EPM7256B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	3.3		4.8		6.6		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		1.0		1.5		1.5		ns
t <sub>FH</sub>	Global clock hold time for fast input		1.0		1.0		1.0		ns
t <sub>FZHSU</sub>	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t <sub>FZHH</sub>	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.4		2.0		2.8		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.4		0.8		1.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	5.2	1.0	7.9	1.0	10.5	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		5.3		7.9		10.6	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (3)	188.7		126.6		94.3		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		5.3		7.9		10.6	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (3)	188.7		126.6		94.3		MHz

**Table 28. EPM7256B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.4		0.6		0.8	ns
$t_{IO}$	I/O input pad and buffer delay			0.4		0.6		0.8	ns
$t_{FIN}$	Fast input delay			1.5		2.5		3.1	ns
$t_{FIND}$	Programmable delay adder for fast input			1.5		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.3		3.0	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.6		0.8	ns
$t_{LAD}$	Logic array delay			1.7		2.5		3.3	ns
$t_{LAC}$	Logic control array delay			1.5		2.2		2.9	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.3	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.4		1.9	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.4		6.9	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.2		3.3		4.5	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		7.2		8.3		9.5	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		2.2		3.3		4.5	ns
$t_{SU}$	Register setup time		1.2		1.8		2.5		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.4		1.4		ns
$t_{RD}$	Register delay			0.7		1.0		1.3	ns
$t_{COMB}$	Combinatorial delay			0.3		0.4		0.5	ns
$t_{IC}$	Array clock delay			1.5		2.3		3.0	ns
$t_{EN}$	Register enable time			1.5		2.2		2.9	ns
$t_{GLOB}$	Global control delay			1.3		2.1		2.7	ns
$t_{PRE}$	Register preset time			1.0		1.6		2.1	ns
$t_{CLR}$	Register clear time			1.0		1.6		2.1	ns
$t_{PIA}$	PIA delay	(2)		1.7		2.6		3.3	ns
$t_{LPA}$	Low-power adder	(4)		2.0		3.0		4.0	ns

**Table 31. EPM7512B Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.3		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.3		0.5	ns
$t_{FIN}$	Fast input delay			2.2		3.2		4.0	ns
$t_{FIND}$	Programmable delay adder for fast input			1.5		1.5		1.5	ns
$t_{SEXP}$	Shared expander delay			1.5		2.1		2.7	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5		0.7	ns
$t_{LAD}$	Logic array delay			1.7		2.3		3.0	ns
$t_{LAC}$	Logic control array delay			1.5		2.0		2.6	ns
$t_{IOE}$	Internal output enable delay			0.1		0.2		0.2	ns
$t_{OD1}$	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.6	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.8		3.8		5.0	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		7.8		8.8		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		2.8		3.8		5.0	ns
$t_{SU}$	Register setup time		1.5		2.0		2.6		ns
$t_H$	Register hold time		0.4		0.5		0.7		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.2		1.4		1.4		ns
$t_{RD}$	Register delay			0.5		0.7		1.0	ns
$t_{COMB}$	Combinatorial delay			0.2		0.3		0.4	ns
$t_{IC}$	Array clock delay			1.8		2.4		3.1	ns
$t_{EN}$	Register enable time			1.5		2.0		2.6	ns
$t_{GLOB}$	Global control delay			2.0		2.8		3.6	ns
$t_{PRE}$	Register preset time			1.0		1.4		1.9	ns
$t_{CLR}$	Register clear time			1.0		1.4		1.9	ns
$t_{PIA}$	PIA delay	(2)		2.4		3.4		4.5	ns
$t_{LPA}$	Low-power adder	(4)		2.0		2.7		3.6	ns

**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

**Notes to tables:**

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{CPW}$ ,  $t_{EN}$ , and  $t_{SEXP}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$ , in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

**Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram**

*Package outlines not drawn to scale.*

