# Intel - EPM7512BUC169-7N Datasheet

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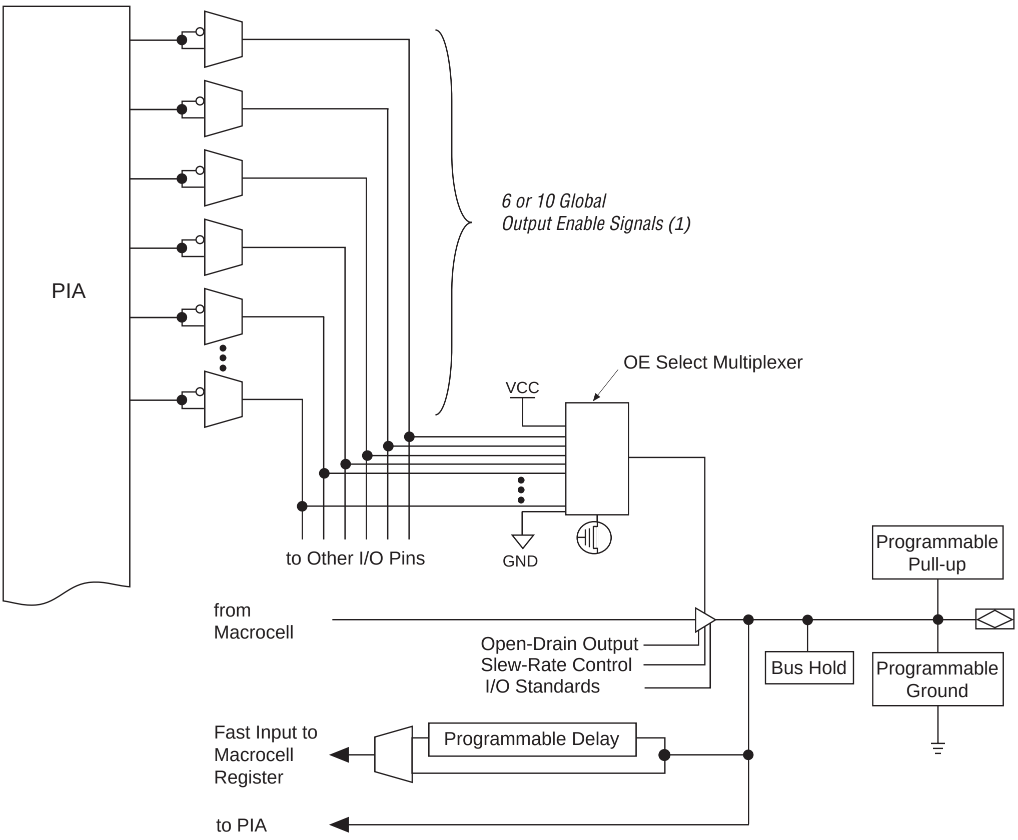
## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 2.375V ~ 2.625V |
| Number of Logic Elements/Blocks | 32 |
| Number of Macrocells | 512 |
| Number of Gates | 10000 |
| Number of I/O | 141 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 169-LFBGA |
| Supplier Device Package | 169-UBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7512buc169-7n |

*Figure 6. I/O Control Block of MAX 7000B Devices*



*Note:*

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to $V_{CC}$, the output is enabled.

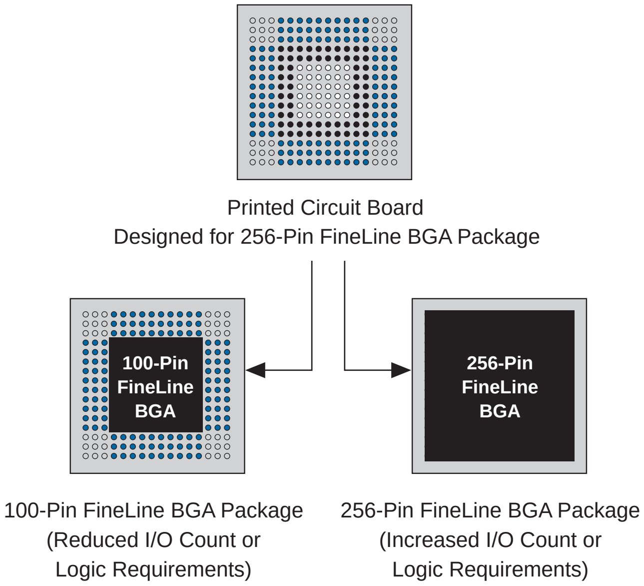
The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see Figure 7).

*Figure 7. SameFrame Pin-Out Example*



By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the `TCK` frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### Programming a Single MAX 7000B Device

The time required to program a single MAX 7000B device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: $t_{PROG}$ = Programming time
$t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of `TCK` cycles to program a device
$f_{TCK}$ = `TCK` frequency

The ISP times for a stand-alone verification of a single MAX 7000B device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: $t_{VER}$ = Verify time
$t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of `TCK` cycles to verify a device

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. Tables 7 and 8 show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

*Table 7. MAX 7000B Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EPM7032B | 96 |
| EPM7064B | 192 |
| EPM7128B | 288 |
| EPM7256B | 480 |
| EPM7512B | 624 |

*Table 8. 32-Bit MAX 7000B Device IDCODE* *Note (1)*

| Device | IDCODE (32 Bits) | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EPM7032B | 0010 | 0111 0000 0011 0010 | 00001101110 | 1 |
| EPM7064B | 0010 | 0111 0000 0110 0100 | 00001101110 | 1 |
| EPM7128B | 0010 | 0111 0001 0010 1000 | 00001101110 | 1 |
| EPM7256B | 0010 | 0111 0010 0101 0110 | 00001101110 | 1 |
| EPM7512B | 0010 | 0111 0101 0001 0010 | 00001101110 | 1 |

*Notes:*

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG boundary-scan testing.

Figure 8 shows the timing information for the JTAG signals.

MAX 7000B devices contain two I/O banks. Both banks support all standards. Each I/O bank has its own `VCCIO` pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Within a bank, any one of the terminated standards can be supported.

Figure 9 shows the arrangement of the MAX 7000B I/O banks.

*Figure 9. MAX 7000B I/O Banks for Various Advanced I/O Standards*

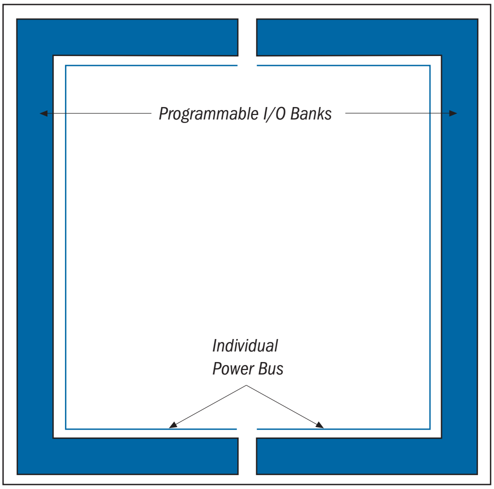


Table 11 shows which macrocells have pins in each I/O bank.

*Table 11. Macrocell Pins Contained in Each I/O Bank*

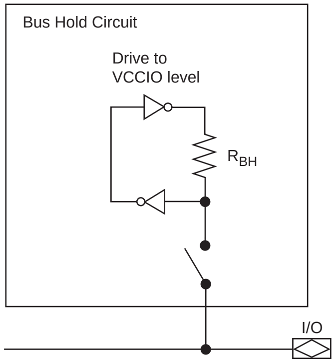
| Device | Bank 1 | Bank 2 |
|---|---|---|
| EPM7032B | 1-16 | 17-32 |
| EPM7064B | 1-32 | 33-64 |
| EPM7128B | 1-64 | 65-128 |
| EPM7256B | 1-128, 177-181 | 129-176, 182-256 |
| EPM7512B | 1-265 | 266-512 |

Each MAX 7000B device has two VREF pins. Each can be set to a separate $V_{REF}$ level. Any I/O pin that uses one of the voltage-referenced standards (GTL+, SSTL-2, or SSTL-3) may use either of the two VREF pins. If these pins are not required as VREF pins, they may be individually programmed to function as user I/O pins.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

*Figure 10. Bus-Hold Circuit*



## PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the ***PCI Local Bus Specification Revision 2.2*** except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

*Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications*

| Device | Specification | |
|---|---|---|
| | 33-MHz PCI | 66-MHz PCI |
| EPM7032B | All speed grades | -3 |
| EPM7064B | All speed grades | -3 |
| EPM7128B | All speed grades | -4 |
| EPM7256B | All speed grades | -5 *(1)* |
| EPM7512B | All speed grades | -5 *(1)* |

*Note:*

(1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

## Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The $V_{CCIO}$ and $V_{CCINT}$ power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

MAX 7000B device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 4.1 V during hot-socketing.

## Design Security

All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during early stages of the production flow.

### Table 15. MAX 7000B Device Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(10)* | 2.375 | 2.625 | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 3.3-V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers, 2.5-V operation | | 2.375 | 2.625 | V |
| | Supply voltage for output drivers, 1.8-V operation | | 1.71 | 1.89 | V |
| $V_{CCISP}$ | Supply voltage during in-system programming | | 2.375 | 2.625 | V |
| $V_I$ | Input voltage | *(3)* | –0.5 | 3.9 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use *(11)* | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use *(11)* | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

***Table 16. MAX 7000B Device DC Operating Conditions*** *Note (4)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage for 3.3-V TTL/CMOS | | 2.0 | 3.9 | V |
| | High-level input voltage for 2.5-V TTL/CMOS | | 1.7 | 3.9 | V |
| | High-level input voltage for 1.8-V TTL/CMOS | | $0.65 \times V_{CCIO}$ | 3.9 | V |
| $V_{IL}$ | Low-level input voltage for 3.3-V TTL/CMOS and PCI compliance | | –0.5 | 0.8 | V |
| | Low-level input voltage for 2.5-V TTL/CMOS | | –0.5 | 0.7 | V |
| | Low-level input voltage for 1.8-V TTL/CMOS | | –0.5 | $0.35 \times V_{CCIO}$ | |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | $V_{CCIO} - 0.2$ | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –100 μA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 1.7 | | V |
| | 1.8-V high-level output voltage | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ =1.65 V *(5)* | 1.2 | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.4 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.2 | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 100 μA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.7 | V |
| | 1.8-V low-level output voltage | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 1.7 V *(6)* | | 0.4 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 3.9 V *(7)* | –10 | 10 | μA |
| $I_{OZ}$ | Tri-state output off-state current | $V_I$ = –0.5 to 3.9 V *(7)* | –10 | 10 | μA |
| $R_{ISP}$ | Value of I/O pin pull-up resistor during in-system programming or during power up | $V_{CCIO}$ = 1.7 to 3.6 V *(8)* | 20 | 74 | k¾ |

Tables 18 through 32 show MAX 7000B device timing parameters.

**Table 18. EPM7032B External Timing Parameters** *Notes (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3.5 | | -5.0 | | -7.5 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 3.5 | | 5.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 3.5 | | 5.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.1 | | 3.0 | | 4.5 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.0 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 2.4 | 1.0 | 3.4 | 1.0 | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 0.9 | | 1.3 | | 1.9 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | 0.6 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 3.6 | 1.0 | 5.1 | 1.0 | 7.6 | ns |
| $t_{ACH}$ | Array clock high time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 1.5 | | 2.0 | | 3.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 3.3 | | 4.7 | | 7.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 303.0 | | 212.8 | | 142.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 3.3 | | 4.7 | | 7.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 303.0 | | 212.8 | | 142.9 | | MHz |

**Table 19. EPM7032B Internal Timing Parameters** *Notes (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3.5 | | -5.0 | | -7.5 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{FIN}$ | Fast input delay | | | 0.9 | | 1.3 | | 2.0 | ns |
| $t_{FIND}$ | Programmable delay adder for fast input | | | 1.0 | | 1.5 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.5 | | 2.1 | | 3.2 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.6 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.4 | | 2.0 | | 3.1 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.2 | | 1.7 | | 2.6 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.9 | | 1.2 | | 1.8 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>slow slew rate = on<br>$V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.9 | | 6.2 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.6 | | 2.2 | | 3.4 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>slow slew rate = on<br>$V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.6 | | 7.2 | | 8.4 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 1.6 | | 2.2 | | 3.4 | ns |
| $t_{SU}$ | Register setup time | | 0.7 | | 1.1 | | 1.6 | | ns |
| $t_{H}$ | Register hold time | | 0.4 | | 0.5 | | 0.9 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 0.8 | | 0.8 | | 1.1 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.2 | | 1.2 | | 1.4 | | ns |
| $t_{RD}$ | Register delay | | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.8 | | 2.8 | ns |
| $t_{EN}$ | Register enable time | | | 1.2 | | 1.7 | | 2.6 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.7 | | 1.1 | | 1.6 | ns |
| $t_{PRE}$ | Register preset time | | | 1.0 | | 1.3 | | 1.9 | ns |
| $t_{CLR}$ | Register clear time | | | 1.0 | | 1.3 | | 1.9 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 0.7 | | 1.0 | | 1.4 | ns |
| $t_{LPA}$ | Low-power adder | *(4)* | | 1.5 | | 2.1 | | 3.2 | ns |

**Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays** *Notes (1)*

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -3.5 | | -5.0 | | -7.5 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of all LABs.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

**Table 24. EPM7128B External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 4.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 4.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.5 | | 4.5 | | 6.1 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.0 | | 3.0 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 2.8 | 1.0 | 5.7 | 1.0 | 7.5 | ns |
| $t_{CH}$ | Global clock high time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.2 | | 2.0 | | 2.8 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.7 | | 0.9 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.1 | 1.0 | 8.2 | 1.0 | 10.8 | ns |
| $t_{ACH}$ | Array clock high time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 1.5 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 4.1 | | 7.9 | | 10.6 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 243.9 | | 126.6 | | 94.3 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 4.1 | | 7.9 | | 10.6 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 243.9 | | 126.6 | | 94.3 | | MHz |

**Table 27. EPM7256B External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 5.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 5.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 3.3 | | 4.8 | | 6.6 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time for fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.3 | 1.0 | 5.1 | 1.0 | 6.7 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.4 | | 2.0 | | 2.8 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.4 | | 0.8 | | 1.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 5.2 | 1.0 | 7.9 | 1.0 | 10.5 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 5.3 | | 7.9 | | 10.6 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 188.7 | | 126.6 | | 94.3 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 5.3 | | 7.9 | | 10.6 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 188.7 | | 126.6 | | 94.3 | | MHz |

*Table 30. EPM7512B External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 5.5 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 5.5 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 3.6 | | 4.9 | | 6.5 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{FZHSU}$ | Global clock setup time of fast input with zero hold time | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{FZHH}$ | Global clock hold time of fast input with zero hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.7 | 1.0 | 5.0 | 1.0 | 6.7 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.4 | | 1.9 | | 2.5 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 5.9 | 1.0 | 8.0 | 1.0 | 10.7 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | | 3.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 6.1 | | 8.4 | | 11.1 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(3)* | 163.9 | | 119.0 | | 90.1 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 6.1 | | 8.4 | | 11.1 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(3)* | 163.9 | | 119.0 | | 90.1 | | MHz |

**Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2)** Note (1)

| I/O Standard | Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -5 | | -7 | | -10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| PCI | Input to PIA | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to global clock and clear | | 0.0 | | 0.0 | | 0.0 | ns |
| | Input to fast input register | | 0.0 | | 0.0 | | 0.0 | ns |
| | All outputs | | 0.0 | | 0.0 | | 0.0 | ns |

*Notes to tables:*

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{CPPW}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

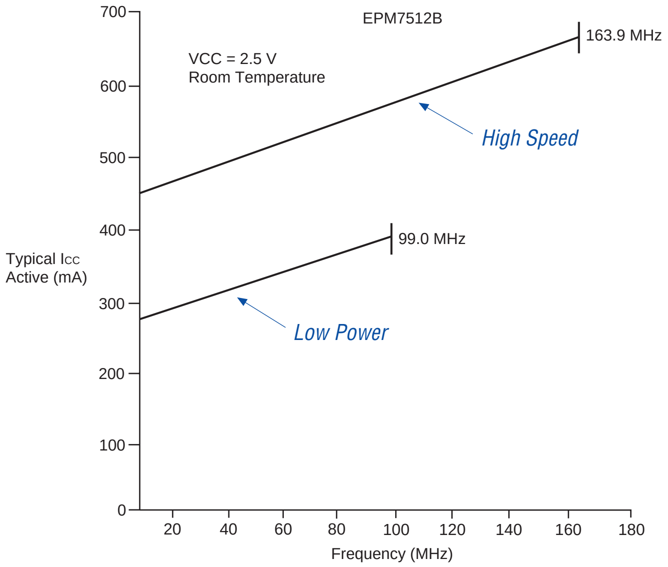
## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

*Figure 19. $I_{CC}$ vs. Frequency for EPM7512B Devices*



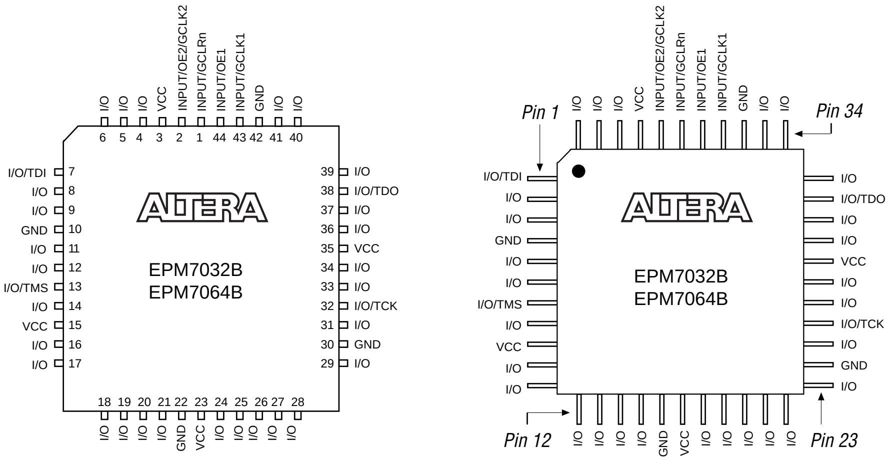
## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

### *Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram*

*Package outlines not drawn to scale.*



44-Pin PLCC

44-Pin TQFP

*Figure 23. 100-Pin TQFP Package Pin-Out Diagram*

*Package outline not drawn to scale.*

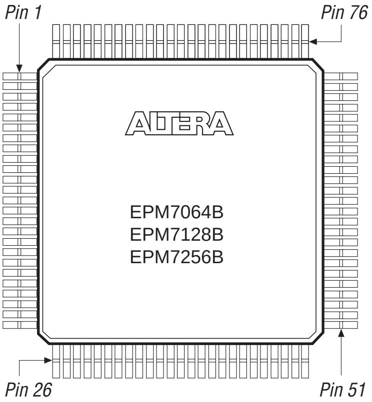
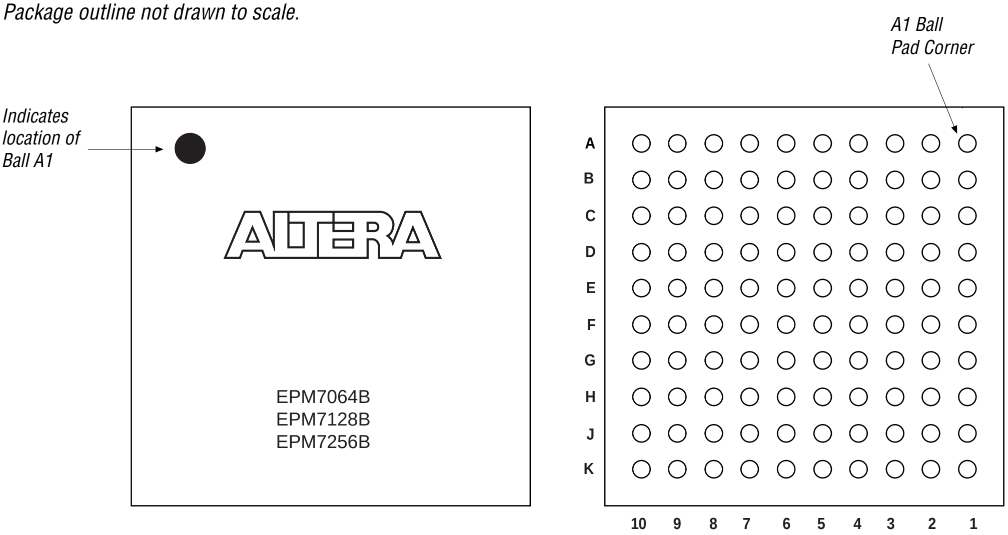


*Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram*

*Package outline not drawn to scale.*



## Version 3.3

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.3:

- Updated Table 3.
- Added Tables 4 through 6.

## Version 3.2

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.2:

- Updated *Note (10)* and added ambient temperature ($T_A$) information to Table 15.

## Version 3.1

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.1:

- Updated $V_{IH}$ and $V_{IL}$ specifications in Table 16.
- Updated leakage current conditions in Table 16.

## Version 3.0

The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 3.0:

- Updated timing numbers in Table 1.
- Updated Table 16.
- Updated timing in Tables 18, 19, 21, 22, 24, 25, 27, 28, 30, and 31.

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