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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	88
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xhy128f0clm

1.2.1 MC9S12XHY Family Comparison

Table 1-1 provides a summary of different members of the MC9S12XHY family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1-1. MC9S12XHY Family

Feature	MC9S12XHY128		MC9S12XHY256	
CPU	HCS12X V1			
Flash memory (ECC)	128Kbytes		256 Kbytes	
Data flash (ECC)	8 Kbytes			
RAM	8 Kbytes		12kbyte	
Pin Quantity	100	112	100	112
CAN	2			
SCI	2			
SPI	1			
IIC	1			
Timer 0	8 ch x 16-bit			
Timer 1	8 ch x 16-bit			
PWM	8 ch x 8-bit or 4ch x16-bit			
ADC (10-bit)	8 ch	12ch	8ch	12 ch
Stepper Motor Controller	4			
Stepper Stall Detecter	4			
LCD Driver (FPxBP)	38x4	40x4	38x4	40x4
Key Wakeup Pins	23	25	23	25
Frequency Modulated PLL	Yes			
External osc (4–16 MHz Pierce with loop control)	Yes			

Table 1-11. Interrupt Vector Locations (Sheet 2 of 3)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable
Vector base + $C0	IIC bus	I bit	IBCR(IBIE)
Vector base + $BE to Vector base + $BC	Reserved		
Vector base + $BA	FLASH Fault Detect	I bit	FCNFG2 (SFDIE, DFDIE)
Vector base + $B8	FLASH	I bit	FCNFG (CCIE)
Vector base + $B6	CAN0 wake-up	I bit	CANRIER (WUPIE)
Vector base + $B4	CAN0 errors	I bit	CANRIER (CSCIE, OVRIE)
Vector base + $B2	CAN0 receive	I bit	CANRIER (RXFIE)
Vector base + $B0	CAN0 transmit	I bit	CANTIER (TXEIE[2:0])
Vector base+ $AE	TIM1 timer channel 0	I bit	TIM1TIE (C0I)
Vector base + $AC	TIM1 timer channel 1	I bit	TIM1TIE (C1I)
Vector base+ $AA	TIM1 timer channel 2	I bit	TIM1TIE (C2I)
Vector base+ $A8	TIM1 timer channel 3	I bit	TIM1TIE (C3I)
Vector base+ $A6	TIM1 timer channel 4	I bit	TIM1TIE (C4I)
Vector base + $A4	TIM1 timer channel 5	I bit	TIM1TIE (C5I)
Vector base+ $A2	TIM1 timer channel 6	I bit	TIM1TIE (C6I)
Vector base+ $A0	TIM1 timer channel 7	I bit	TIM1TIE (C7I)
Vector base+ $9E	TIM1 timer overflow	I bit	TIM1TSRC2 (TOF)
Vector base+ $9C	TIM1 Pulse accumulator A overflow	I bit	TIM1PACTL (PAOVI)
Vector base + $9A	TIM1 Pulse accumulator input edge	I bit	TIM1PACTL (PAI)
Vector base+ $98	Reserved		
Vector base + $96	Motor Control Timer Overflow	I-Bit	MCCTL1 (MCOCIE)
Vector base + $94 to Vector base + $90	Reserved		
Vector base + $8E	Port T	I bit	PIET (PIET7-PIET0)
Vector base+ $8C	PWM emergency shutdown	I bit	PWMSDN (PWMIE)
Vector base + $8A	SSD0	I bit	MDC0CTL(MCZIE,AOVIE)
Vector base + $88	SSD1	I bit	MDC1CTL(MCZIE,AOVIE)
Vector base + $86	SSD2	I bit	MDC2CTL(MCZIE,AOVIE)
Vector base + $84	SSD3	I bit	MDC3CTL(MCZIE,AOVIE)
Vector base + $82	Reserved		
Vector base + $80	Low-voltage interrupt (LVI)	I bit	VREGCTRL (LVIE)
Vector base + $7E	Autonomous periodical interrupt (API)	I bit	VREGAPICTRL (APIE)

2.3.10 ECLK Control Register (ECLKCTL)

Address 0x001C (PRR) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	NECLK	0	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
W								
Reset:	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-8. ECLK Control Register (ECLKCTL)

[1] Read: Anytime
Write: Anytime

Table 2-9. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	**No ECLK**—Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. This clock has a fixed rate of equivalent to the internal bus clock. 1 ECLK disabled 0 ECLK enabled
5 DIV16	**Free-running ECLK predivider**—Divide by 16 This bit enables a divide-by-16 stage on the selected EDIV rate. 1 Divider enabled: ECLK rate = EDIV rate divided by 16 0 Divider disabled: ECLK rate = EDIV rate
4-0 EDIV	**Free-running ECLK Divider**—Configure ECLK rate These bits determine the rate of the free-running clock on the ECLK pin. 00000 ECLK rate = bus clock rate[1] 00001 ECLK rate = bus clock rate divided by 2 00010 ECLK rate = bus clock rate divided by 3,... 11111 ECLK rate = bus clock rate divided by 32

[1] when EDIV=00000 DIV16-0,and bus clock>=32MHz, ECLK output maybe cannot work

2.3.11 PIM Reserved Register

Address 0x001D (PRR) Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-9. PIM Reserved Register

2.3.38 PIM Reserved Register

Address 0x0257 Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-35. PIM Reserved Register

1 Read: Anytime
Write: Anytime

2.3.39 Port P Data Register (PTP)

Address 0x0258 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Altern. Function	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset	0	0	0	0	0	0	0	0

Figure 2-36. Port P Data Register (PTP)

1 Read: Anytime.
Write: Anytime.

Table 2-31. PTP Register Field Descriptions

Field	Description
7-0 PTP	**Port P general purpose input/output data**—Data Register, LCD segment driver output, PWM channel output Port P pins are associated with the PWM channel output and LCD segment driver output. When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The LCD segment takes precedence over the PWM function and the general purpose I/O function is LCD segment output is enabled • The PWM function takes precedence over the general purpose I/O function if the PWM channel is enabled.

2.3.50 PIM Reserved Registers

Address 0x0263 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-47. PIM Reserved Register)

1 Read: Anytime.
Write: Anytime.

2.3.51 Port H Pull Device Enable Register (PERH)

Address 0x0264 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
W								
Reset	1	1	1	1	1	1	1	1

Figure 2-48. Port H Pull Device Enable Register (PERH)

1 Read: Anytime.
Write: Anytime.

Table 2-42. PERH Register Field Descriptions

Field	Description
7-0 PERH	**Port H pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset all pull device is enabled. 1 Pull device enabled. 0 Pull device disabled.

2.3.52 Port H Polarity Select Register (PPSH)

Address 0x0265 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
W								
Reset	1	1	1	1	1	1	1	1

Figure 2-49. Port H Polarity Select Register (PPSH)

3.4 Functional Description

The MMC block performs several basic functions of the S12X sub-system operation: MCU operation modes, priority control, address mapping, select signal generation and access limitations for the system. Each aspect is described in the following subsections.

3.4.1 MCU Operating Mode

- Normal single-chip mode

  There is no external bus in this mode. The MCU program is executed from the internal memory and no external accesses are allowed.
- Special single-chip mode

  This mode is generally used for debugging single-chip operation, boot-strapping or security related operations. The active background debug mode is in control of the CPU code execution and the BDM firmware is waiting for serial commands sent through the BKGD pin. There is no external bus in this mode.

3.4.2 Memory Map Scheme

3.4.2.1 CPU and BDM Memory Map Scheme

The BDM firmware lookup tables and BDM register memory locations share addresses with other modules; however they are not visible in the global memory map during user's code execution. The BDM memory resources are enabled only during the READ_BD and WRITE_BD access cycles to distinguish between accesses to the BDM memory area and accesses to the other modules. (Refer to BDM Block Guide for further details).

When the MCU enters active BDM mode, the BDM firmware lookup tables and the BDM registers become visible in the local memory map in the range 0xFF00-0xFFFF (global address 0x7F_FF00 - 0x7F_FFFF) and the CPU begins execution of firmware commands or the BDM begins execution of hardware commands. The resources which share memory space with the BDM module will not be visible in the global memory map during active BDM mode.

Please note that after the MCU enters active BDM mode the BDM firmware lookup tables and the BDM registers will also be visible between addresses 0xBF00 and 0xBFFF if the PPAGE register contains value of 0xFF.

4.1.3 Modes of Operation

- Run mode

  This is the basic mode of operation.

- Wait mode

  In wait mode, the XINT module is frozen. It is however capable of either waking up the CPU if an interrupt occurs or waking up the XGATE if an XGATE request occurs. Please refer to Section 4.5.3, “Wake Up from Stop or Wait Mode” for details.

- Stop Mode

  In stop mode, the XINT module is frozen. It is however capable of either waking up the CPU if an interrupt occurs or waking up the XGATE if an XGATE request occurs. Please refer to Section 4.5.3, “Wake Up from Stop or Wait Mode” for details.

- Freeze mode (BDM active)

  In freeze mode (BDM active), the interrupt vector base register is overridden internally. Please refer to Section 4.3.2.1, “Interrupt Vector Base Register (IVBR)” for details.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

5.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (the lowest serial communication frequency is determined by the crystal oscillator or the clock chosen by CLKSW.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic one.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed

Table 7-11. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	**001 ($2x10^3$)**	**010 ($5x10^3$)**	**011 ($10x10^3$)**	**100 ($20x10^3$)**	**101 ($50x10^3$)**	**110 ($100x10^3$)**	**111 ($200x10^3$)**
0110 (÷7)	$7x10^3$	$14x10^3$	$35x10^3$	$70x10^3$	$140x10^3$	$350x10^3$	$700x10^3$	$1.4x10^6$
0111 (÷8)	$8x10^3$	$16x10^3$	$40x10^3$	$80x10^3$	$160x10^3$	$400x10^3$	$800x10^3$	$1.6x10^6$
1000 (÷9)	$9x10^3$	$18x10^3$	$45x10^3$	$90x10^3$	$180x10^3$	$450x10^3$	$900x10^3$	$1.8x10^6$
1001 (÷10)	$10 x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$	$500x10^3$	$1x10^6$	$2x10^6$
1010 (÷11)	$11 x10^3$	$22x10^3$	$55x10^3$	$110x10^3$	$220x10^3$	$550x10^3$	$1.1x10^6$	$2.2x10^6$
1011 (÷12)	$12x10^3$	$24x10^3$	$60x10^3$	$120x10^3$	$240x10^3$	$600x10^3$	$1.2x10^6$	$2.4x10^6$
1100 (÷13)	$13x10^3$	$26x10^3$	$65x10^3$	$130x10^3$	$260x10^3$	$650x10^3$	$1.3x10^6$	$2.6x10^6$
1101 (÷14)	$14x10^3$	$28x10^3$	$70x10^3$	$140x10^3$	$280x10^3$	$700x10^3$	$1.4x10^6$	$2.8x10^6$
1110 (÷15)	$15x10^3$	$30x10^3$	$75x10^3$	$150x10^3$	$300x10^3$	$750x10^3$	$1.5x10^6$	$3x10^6$
1111 (÷16)	$16x10^3$	$32x10^3$	$80x10^3$	$160x10^3$	$320x10^3$	$800x10^3$	$1.6x10^6$	$3.2x10^6$

7.3.2.9 S12XECRG COP Control Register (COPCTL)

This register controls the COP (Computer Operating Properly) watchdog.

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W			WRTMASK					
Reset[1]	0	0	0	0	0	0	0	0

1. Refer to Device User Guide (Section: S12XECRG) for reset values of WCOP, CR2, CR1 and CR0.

= Unimplemented or Reserved

Figure 7-11. S12XECRG COP Control Register (COPCTL)

Read: Anytime

Write:

1. RSBCK: anytime in special modes; write to “1” but not to “0” in all other modes
2. WCOP, CR2, CR1, CR0:
   - — Anytime in special modes
   - — Write once in all other modes
     - – Writing CR[2:0] to “000” has no effect, but counts for the “write once” condition.
     - – Writing WCOP to “0” has no effect, but counts for the “write once” condition.

10.3.2 Register Descriptions

This section describes in address order all the ADC12B12C registers and their individual bits.

10.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 10-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 10-1. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 10-2.

Table 10-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved[1]
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN11
1	1	0	1	AN11
1	1	1	0	AN11
1	1	1	1	AN11

11.3.3.1.2 IDR0–IDR3 for Standard Identifier Mapping

Module Base + 0x00X0

	7	6	5	4	3	2	1	0
R W	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
Reset:	x	x	x	x	x	x	x	x

Figure 11-30. Identifier Register 0 — Standard Mapping

Table 11-31. IDR0 Register Field Descriptions — Standard

Field	Description
7-0 ID[10:3]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 11-32.

Module Base + 0x00X1

	7	6	5	4	3	2	1	0
R W	ID2	ID1	ID0	RTR	IDE (=0)			
Reset:	x	x	x	x	x	x	x	x

= Unused; always read 'x'

Figure 11-31. Identifier Register 1 — Standard Mapping

Table 11-32. IDR1 Register Field Descriptions

Field	Description
7-5 ID[2:0]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 11-31.
4 RTR	**Remote Transmission Request** — This flag reflects the status of the Remote Transmission Request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)

Module Base + 0x00X2

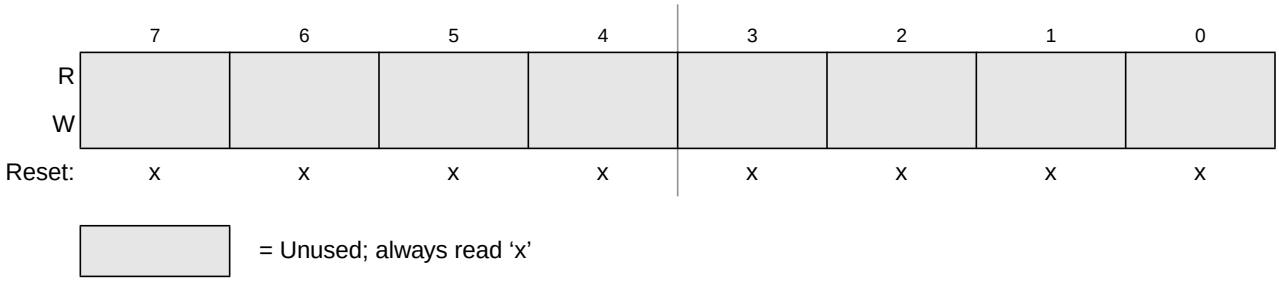

Figure 11-32. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

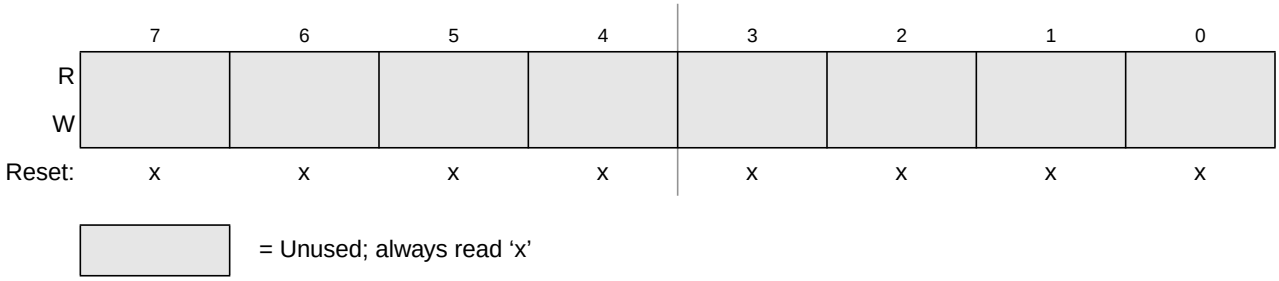

Figure 11-33. Identifier Register 3 — Standard Mapping

11.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

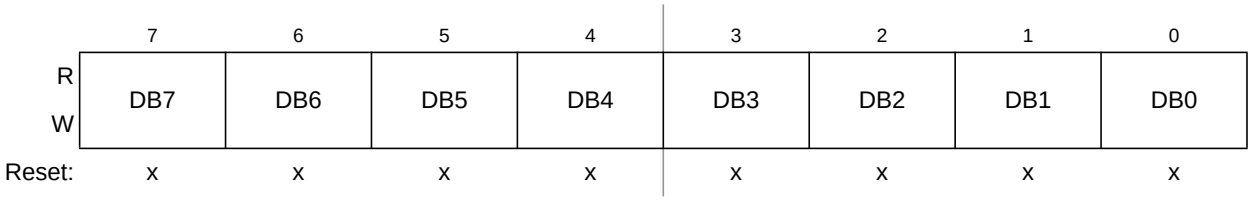

Figure 11-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 11-33. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	**Data bits 7-0**

12.2 External Signal Description

The IICV3 module has two external pins.

12.2.1 IIC_SCL — Serial Clock Line Pin

This is the bidirectional serial clock line (SCL) of the module, compatible to the IIC bus specification.

12.2.2 IIC_SDA — Serial Data Line Pin

This is the bidirectional serial data line (SDA) of the module, compatible to the IIC bus specification.

12.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers for the IIC module.

12.3.1 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
	W								
0x0001 IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
	W								
0x0002 IBCR	R	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
	W						RSTA		
0x0003 IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
	W								
0x0004 IBDR	R	D7	D6	D5	D4	D3	D2	D1	D0
	W								
0x0005 IBCR2	R	GCEN	ADTYPE	0	0	0	ADR10	ADR9	ADR8
	W								

= Unimplemented or Reserved

Figure 12-2. IIC Register Summary

Table 17-7. LCD RAM Field Descriptions

Field	Description
39:0 3:0 FP[39:0] BP[3:0]	**LCD Segment ON** — The FP[39:0]BP[3:0] bit displays (turns on) the LCD segment connected between FP[39:0] and BP[3:0]. 0 LCD segment OFF 1 LCD segment ON

17.4 Functional Description

This section provides a complete functional description of the LCD40F4BV2 block, detailing the operation of the design from the end user perspective in a number of subsections.

17.4.1 LCD Driver Description

17.4.1.1 Frontplane, Backplane, and LCD System During Reset

During a reset the following conditions exist:

- The LCD40F4BV2 system is configured in the default mode, 1/4 duty and 1/3 bias, that means all backplanes are used.
- All frontplane enable bits, FP[39:0]EN are cleared and the ON/OFF control for the display, the LCDEN bit is cleared, thereby forcing all frontplane and backplane driver outputs to the high impedance state. The MCU pin state during reset is defined by the port integration module (PIM).

17.4.1.2 LCD Clock and Frame Frequency

The frequency of the source clock (IRCCLK) and divider determine the LCD clock frequency. The divider is set by the LCD clock prescaler bits, LCLK[2:0], in the LCD control register 0 (LCDCR0). Table 17-8 shows the LCD clock and frame frequency for some multiplexed mode at IRCCLK = 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, and 0.5 MHz.

Table 17-8. LCD Clock and Frame Frequency

Source clock Frequency in MHz	LCD Clock Prescaler			Divider	LCD Clock Frequency [Hz]	Frame Frequency [Hz]			
	LCLK2	LCLK1	LCLK0			1/1 Duty	1/2 Duty	1/3 Duty	1/4 Duty
IRCCLK = 0.5	0 0	0 0	0 1	1024 2048	488 244	488 244	244 122	163 81	122 61
IRCCLK = 1.0	0 0	0 1	1 0	2048 4096	488 244	488 244	244 122	163 81	122 61
IRCCLK = 2.0	0 0	1 1	0 1	4096 8192	488 244	488 244	244 122	163 81	122 61
IRCCLK = 4.0	0 1	1 0	1 0	8192 16384	488 244	488 244	244 122	163 81	122 61
IRCCLK = 8.0	1 1	0 0	0 1	16384 32768	488 244	488 244	244 122	163 81	122 61

Table 18-5. FDIV vs OSCCLK Frequency

OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]
MIN[1]	MAX[2]		MIN[1]	MAX[2]	
1.60	2.10	0x01	33.60	34.65	0x20
2.40	3.15	0x02	34.65	35.70	0x21
3.20	4.20	0x03	35.70	36.75	0x22
4.20	5.25	0x04	36.75	37.80	0x23
5.25	6.30	0x05	37.80	38.85	0x24
6.30	7.35	0x06	38.85	39.90	0x25
7.35	8.40	0x07	39.90	40.95	0x26
8.40	9.45	0x08	40.95	42.00	0x27
9.45	10.50	0x09	42.00	43.05	0x28
10.50	11.55	0x0A	43.05	44.10	0x29
11.55	12.60	0x0B	44.10	45.15	0x2A
12.60	13.65	0x0C	45.15	46.20	0x2B
13.65	14.70	0x0D	46.20	47.25	0x2C
14.70	15.75	0x0E	47.25	48.30	0x2D
15.75	16.80	0x0F	48.30	49.35	0x2E
16.80	17.85	0x10	49.35	50.40	0x2F
17.85	18.90	0x11			
18.90	19.95	0x12			
19.95	21.00	0x13			
21.00	22.05	0x14			
22.05	23.10	0x15			
23.10	24.15	0x16			
24.15	25.20	0x17			
25.20	26.25	0x18			
26.25	27.30	0x19			
27.30	28.35	0x1A			
28.35	29.40	0x1B			
29.40	30.45	0x1C			
30.45	31.50	0x1D			
31.50	32.55	0x1E			
32.55	33.60	0x1F			

1 FDIV shown generates an FCLK frequency of >0.8 MHz

2 FDIV shown generates an FCLK frequency of 1.05 MHz

19.2.1.13 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-16. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

19.2.1.14 Flash ECC Error Results Register (FECCR)

The FECCR registers contain the result of a detected ECC fault for both single bit and double bit faults. The FECCR register provides access to several ECC related fields as defined by the ECCRIX index bits in the FECCRIX register (see Section 19.2.1.4). Once ECC fault information has been stored, no other fault information will be recorded until the specific ECC fault flag has been cleared. In the event of simultaneous ECC faults the priority for fault recording is double bit fault over single bit fault.

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	ECCR[15:8]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-17. Flash ECC Error Results High Register (FECCRHI)

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	ECCR[7:0]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-18. Flash ECC Error Results Low Register (FECCRLO)

All FECCR bits are readable but not writable.

Table 19-37. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 19-25)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [22:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

19.3.2.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash block 0. The Program Once reserved field can be read using the Read Once command as described in Section 19.3.2.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash block 0 cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 19-38. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

RECIRC bit must be changed only while no PWM channel is operated in (dual) full H-bridge mode.

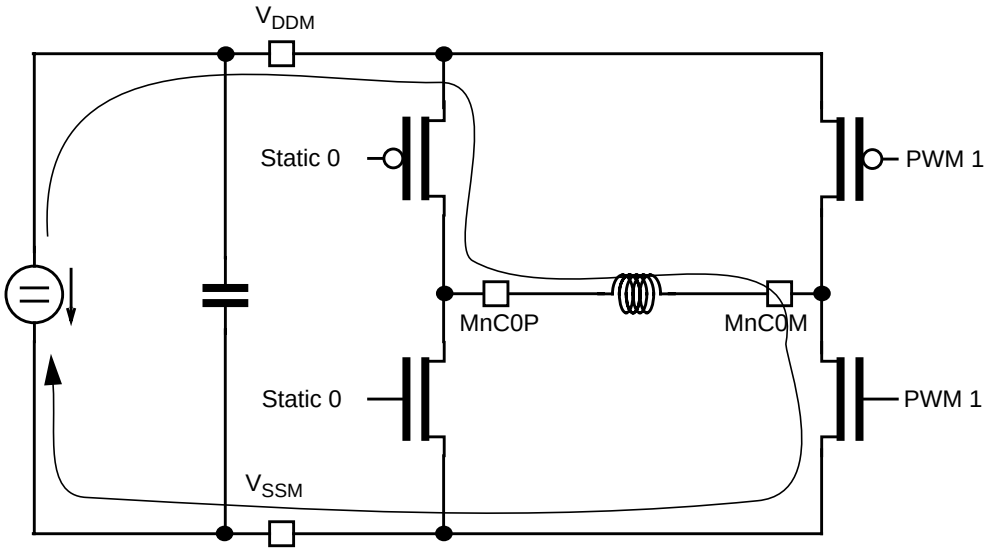

Figure 20-12. PWM Active Phase, RECIRC = 0, S = 0

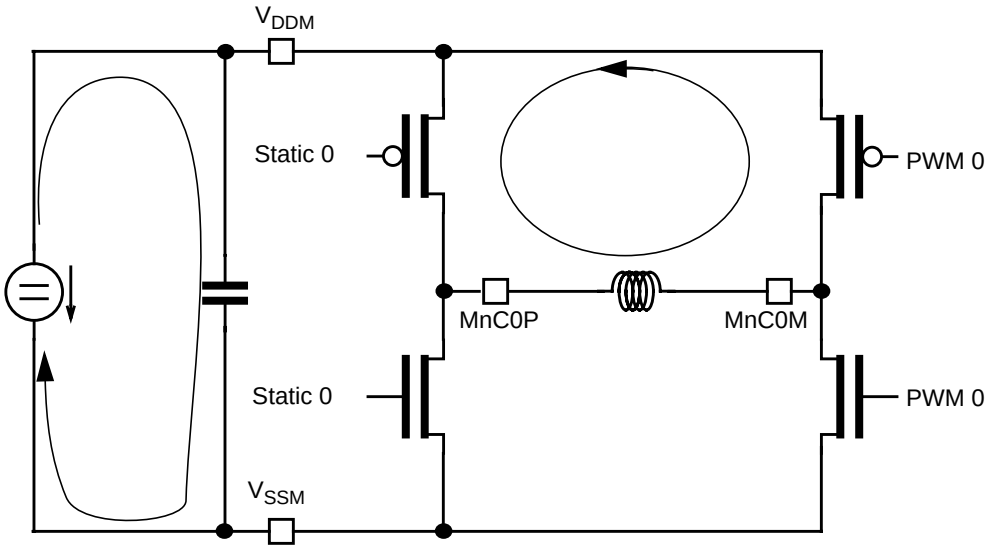

Figure 20-13. PWM Passive Phase, RECIRC = 0, S = 0

Table A-9. Module Run Supply Currents

Conditions are shown in Table A-7 at ambient temperature unless otherwise noted						
Num	**C**	**Rating**	**Min**	**Typ**	**Max**	**Unit**
1	T	S12XCPU	—	5.9	—	mA
2	T	MSCAN	—	0.7	—	
3	T	SPI	—	0.3	—	
4	T	SCI	—	0.1	—	
5	T	PWM	—	0.4	—	
6	T	IIC	—	0.2	—	
7	T	LCD	—	0.3	—	
8	T	MC	—	0.4	—	
9	T	SSD	—	0.7		
10	T	TIM	—	0.3	—	
11	T	ATD	—	0.7	—	
12	T	Overhead	—	10.7	—	

Table A-10. Run and Wait Current Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Run supply current (No external load, Peripheral Configuration see Table A-8.)							
1	P	Peripheral Set[1] f_{osc}=4MHz, f_{bus}=40MHz	I_{DD35}	—	24.9	31.9	mA
Wait supply current							
2	P	Peripheral Set[1] ,PLL on	I_{DDW}	—	16.35	19.9	mA

Figure B-6. 100-pin LQFP(case no.983) - page 3