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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xhy128f0mll

Appendix B
Package and Die Information

Appendix C
PCB Layout Guidelines

Appendix D
Derivative Differences

Appendix E
Detailed Register Address Map

Appendix F
Ordering Information

Table 1-7. Pin-Out Summary[1]

Package Pin		Function								Power Supply	Internal Pull Resistor		Description
LQFP 100	LQFP 64	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.	8th Func.		CTRL	Reset State	
109	97	PAD01	AN01	KWAD1						VDDA	PERAD	Disabled	Port AD I/O, analog input of ATD, key wakeup
110	98	PAD02	AN02	KWAD2						VDDA	PERAD	Disabled	Port AD I/O, analog input of ATD, key wakeup
111	99	PAD03	AN03	KWAD3						VDDA	PERAD	Disabled	Port AD I/O, analog input of ATD, key wakeup
112	100	PAD04	AN04	KWAD4						VDDA	PERAD	Disabled	Port AD I/O, analog input of ATD, key wakeup

1. Table shows a superset of pin functions. Not all functions are available on all derivatives
2. When Routing the IIC to PR/PH port, in order to overwrite the internal pull-down during reset, the external IIC pull-up resistor should be < =4.7K
3. When $\overline{\text{IRQ}}$/XIRQ is enabled, the internal pulldown function will be disabled, the external pullup resistor is required

NOTE

For devices assembled in 100-pin package all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to Table 1-7 for affected pins.

1.7.3.33 PT[7:4] / IOC0[7:4] / KWT[7:4] / FP[16:13] — Port T I/O Pins [7:4]

PT[7:4] are a general-purpose input or output pins. They can be configured as frontplane segment driver output FP[16:13]. They can be configured as timer (TIM0) channel 7-4. They can be configured as key wakeup inputs.

1.7.3.34 PM3 / PMW7 / IOC1_3 — Port M I/O Pins [3]

PM3 is a general-purpose input or output pin. . It can be configured as timer (TIM1) channels 3.It can be configured as PWM channel7.

1.7.3.35 PM2 / PMW6 / IOC1_2 — Port M I/O Pins [2]

PM2 is a general-purpose input or output pin. .It can be configured as timer (TIM1) channels 2. It can be configured as PWM channel6.

1.7.3.36 PM1 / PMW5 / IOC0_3 / TXD1— Port M I/O Pins [1]

PM1 is a general-purpose input or output pin. It can be configured as the transmitpin TXD of serial communication interface(SCI). It can be configured as timer (TIM0) channels 3.It can be configured as PWM channel5.

1.7.3.37 PM0 / PMW4 / IOC0_2 / RXD1— Port M I/O Pins [0]

PM0 is a general-purpose input or output pin. It can be configured as the receive pin RXD of serial communication interface(SCI).It can be configured as timer (TIM0) channels 2. It can be configured as PWM channel4.

1.7.3.38 PT[3:0] / IOC1[7:4] /KWT [3:0] / FP[11:8] — Port T I/O Pin [3:0]

PT[3:0] are a general-purpose input or output pins. They can be configured as frontplane segment driver output FP[11:8]. They can be configured as timer (TIM1) channels 7-4. They can be configured as key wakeup inputs.

1.7.3.39 PU[7] / M1C1P / M1SINP — Port U I/O Pin [7]

PU[7] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive or to measure the back EMF to calibrate the pointer reset position. The pin interfaces to the coils of motor 1.

1.7.3.40 PU[6] / IOC0_3 / M1C1M / M1SINM — Port U I/O Pin [6]

PU[6] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive or to measure the back EMF to calibrate the pointer reset position. The pin interfaces to the coils of motor 1. It can aslo be configured as timer (TIM0) channel 3

The ATD module includes external trigger inputs ETRIG[3:0]. The external trigger allows the user to synchronize ATD conversion to external trigger events. Table 1-14 shows the connection of the external trigger inputs.

Table 1-14. ATD External Trigger Sources

External Trigger Input	Connectivity
ETRIG0	PP1(PWM channel 1)[1]
ETRIG1	PP3(PWM channel 3)[1]
ETRIG2	TIM0 Channel output 2[2]
ETRIG3	TIM0 Channel output 3[2]

1. When LCD segment output driver is enabled on PP1/PP3, the ATD external trigger function will be unavailable
2. Independ on the TIM0OCPD3/2 bit setting

Consult the ATD section for information about the analog-to-digital converter module. References to freeze mode are equivalent to active BDM mode.

1.14 ATD Channel[17] Connection

Further to the 12 externally available channels, ATD0 features an extra channel[17] that is connected to the internal temperature sensor at device level. To access this channel ATD must use the channel encoding SC:CD:CC:CB:CA = 1:0:0:0:1 in ATDCTL5. For more temperature sensor information, please refer to 1.15.1 Temperature Sensor Configuration.

1.15 VREG Configuration

The device must be configured with the internal voltage regulator enabled. Operation in conjunction with an external voltage regulator is not supported.

The API trimming register APITR is loaded from the Flash IFR option field at global address 0x40_00F0 bits[5:0] during the reset sequence. Currently factory programming of this IFR range is not supported.

Read access to reserved VREG register space returns “0”. Write accesses have no effect. This device does not support access abort of reserved VREG register space.

1.15.1 Temperature Sensor Configuration

The VREG high temperature trimming register bits VREGHTTR[3:0] are loaded from the internal Flash during the reset sequence. To use the high temperature interrupt within the specified limits (T_{HTIA} and T_{HTID}) these bits must be loaded with 0x8. Currently factory programming is not supported.

The device temperature can be monitored on ATD0 channel[17]. The internal bandgap reference voltage can also be mapped to ATD0 analog input channel[17]. The voltage regulator VSEL bit when set, maps the bandgap and, when clear, maps the temperature sensor to ATD0 channel[17].

Table 2-23. Module Routing Summary

Module	PTSRR				Related Pins			
IIC	x	x	0	0	PS4		PS7	
	x	x	0	1	PS4		PS7	
	x	x	1	0	PR6		PR5	
	x	x	1	1	PV0		PV3	
					MISO	**MOSI**	**SCK**	**$\overline{\text{SS}}$**
SPI	0	0	x	x	PS4	PS5	PS6	PS7
	0	1	x	x	PH0	PH1	PH2	PH3
	1	0	x	x	PV0	PV1	PV2	PV3
	1	1	x	x	Reserved			

2.3.30 PIM Reserved Register

2.3.59 Port AD Data Direction Register (DDR1AD)

Address 0x0273 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDR1AD7	DDR1AD6	DDR1AD5	DDR1AD4	DDR1AD3	DDR1AD2	DDR1AD1	DDR1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-56. Port AD Data Direction Register (DDR1AD)

1 Read: Anytime
Write: Anytime

Table 2-49. DDR1AD Register Field Descriptions

Field	Description
7-0 DDR1AD	**Port AD data direction**— This bit determines whether the associated pin is an input or output. To use the digital input function the ATD Digital Input Enable Register (ATDDIEN) has to be set to logic level “1”. 1 Associated pin is configured as output 0 Associated pin is configured as input

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PT1AD registers, when changing the DDR1AD register.

2.3.60 PIM Reserved Register

Address 0x0274 Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-57. PIM Reserved Register

1 Read: Always reads 0x00
Write: Unimplemented

Table 5-3. BDMSTS Field Descriptions (continued)

Field	Description
2 CLKSW	**Clock Switch** — The CLKSW bit controls which clock the BDM operates with. It is only writable from a hardware BDM command. A minimum delay of 150 cycles at the clock speed that is active during the data portion of the command send to change the clock source should occur before the next command can be send. The delay should be obtained no matter which bit is modified to effectively change the clock source (either PLLSEL bit or CLKSW bit). This guarantees that the start of the next BDM command uses the new clock for timing subsequent BDM communications. Table 5-4 shows the resulting BDM clock source based on the CLKSW and the PLLSEL (PLL select in the CRG module, the bit is part of the CLKSEL register) bits. **Note:** The BDM alternate clock source can only be selected when CLKSW = 0 and PLLSEL = 1. The BDM serial interface is now fully synchronized to the alternate clock source, when enabled. This eliminates frequency restriction on the alternate clock which was required on previous versions. Refer to the device specification to determine which clock connects to the alternate clock source input. **Note:** If the acknowledge function is turned on, changing the CLKSW bit will cause the ACK to be at the new rate for the write command which changes it. **Note:** In emulation modes (if modes available), the CLKSW bit will be set out of RESET.
1 UNSEC	**Unsecure** — If the device is secured this bit is only writable in special single chip mode from the BDM secure firmware. It is in a zero state as secure mode is entered so that the secure BDM firmware lookup table is enabled and put into the memory map overlapping the standard BDM firmware lookup table. The secure BDM firmware lookup table verifies that the non-volatile memories (e.g. on-chip EEPROM and/or Flash EEPROM) are erased. This being the case, the UNSEC bit is set and the BDM program jumps to the start of the standard BDM firmware lookup table and the secure BDM firmware lookup table is turned off. If the erase test fails, the UNSEC bit will not be asserted. 0 System is in a secured mode. 1 System is in a unsecured mode. **Note:** When UNSEC is set, security is off and the user can change the state of the secure bits in the on-chip Flash EEPROM. Note that if the user does not change the state of the bits to “unsecured” mode, the system will be secured again when it is next taken out of reset.After reset this bit has no meaning or effect when the security byte in the Flash EEPROM is configured for unsecure mode.

Table 5-4. BDM Clock Sources

PLLSEL	CLKSW	BDMCLK
0	0	Bus clock dependent on oscillator
0	1	Bus clock dependent on oscillator
1	0	Alternate clock (refer to the device specification to determine the alternate clock source)
1	1	Bus clock dependent on the PLL

Table 9-10. Selectable Autonomous Periodical Interrupt Periods

APICLK	APIR[15:0]	Selected Period
0	0000	0.2 ms[1]
0	0001	0.4 ms[1]
0	0002	0.6 ms[1]
0	0003	0.8 ms[1]
0	0004	1.0 ms[1]
0	0005	1.2 ms[1]
0	.....	.....
0	FFFD	13106.8 ms[1]
0	FFFE	13107.0 ms[1]
0	FFFF	13107.2 ms[1]
1	0000	2 * bus clock period
1	0001	4 * bus clock period
1	0002	6 * bus clock period
1	0003	8 * bus clock period
1	0004	10 * bus clock period
1	0005	12 * bus clock period
1	.....	.....
1	FFFD	131068 * bus clock period
1	FFFE	131070 * bus clock period
1	FFFF	131072 * bus clock period

[1] When trimmed within specified accuracy. See electrical specifications for details.

The period can be calculated as follows depending of APICLK:

Period = 2*(APIR[15:0] + 1) * 0.1 ms or period = 2*(APIR[15:0] + 1) * bus clock period

10.1.3 Block Diagram

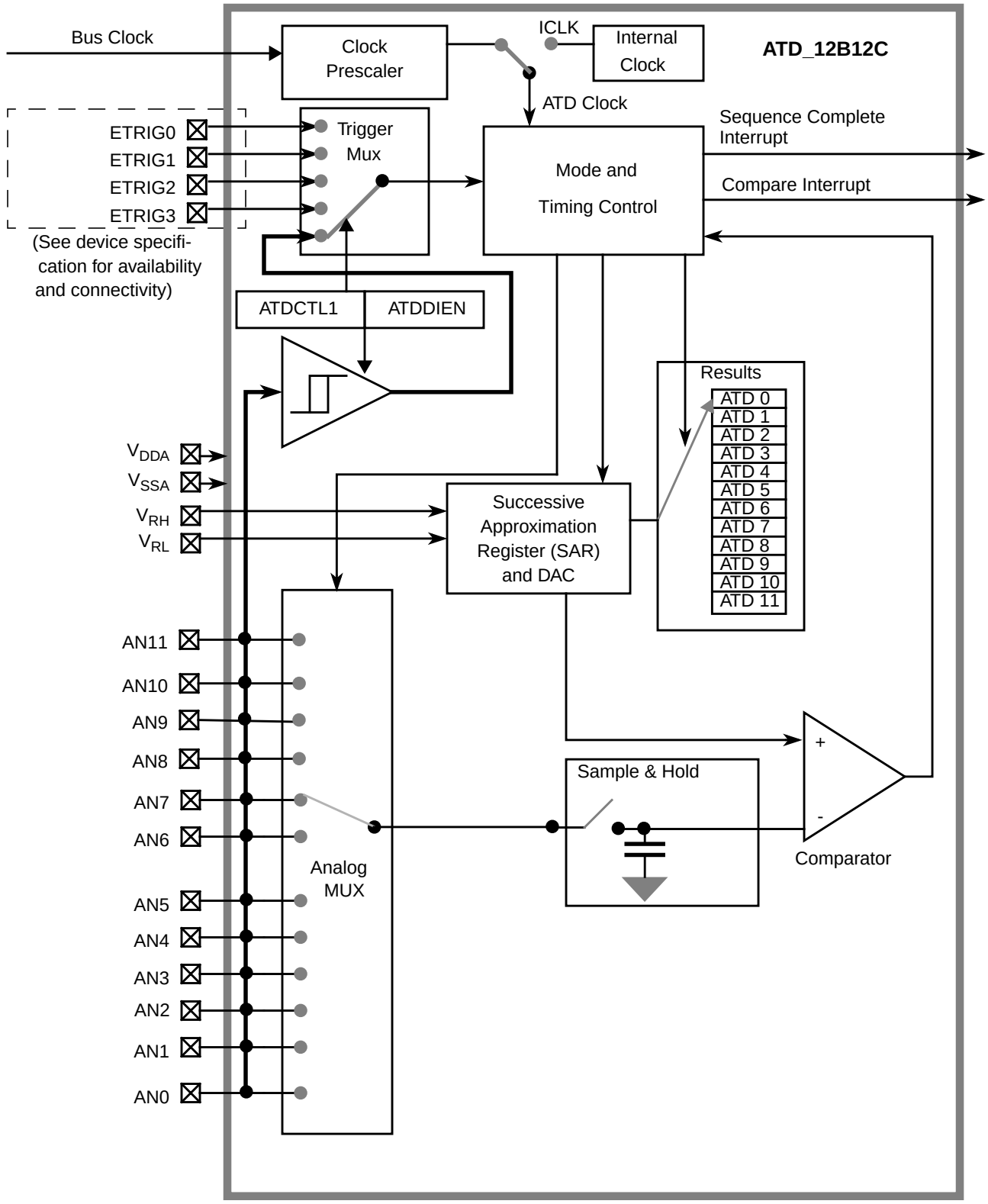

Figure 10-1. ADC12B12C Block Diagram

Write: Anytime (any value written causes PWM counter to be reset to $00).

13.3.2.13 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

See Section 13.4.2.3, “PWM Period and Duty” for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)
- PWMx Period = Channel Clock Period * PWMPERx Center Aligned Output (CAEx = 1)

  PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 13.4.2.8, “PWM Boundary Cases”.

Module Base + 0x0014 = PWMPER0, 0x0015 = PWMPER1, 0x0016 = PWMPER2, 0x0017 = PWMPER3
Module Base + 0x0018 = PWMPER4, 0x0019 = PWMPER5, 0x001A = PWMPER6, 0x001B = PWMPER7

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 13-15. PWM Channel Period Registers (PWMPERx)

Read: Anytime

Write: Anytime

13.4 Functional Description

13.4.1 PWM Clock Select

There are four available clocks: clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the bus clock.

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of two clocks, either the pre-scaled clock (clock A or B) or the scaled clock (clock SA or SB).

The block diagram in Figure 13-18 shows the four different clocks and how the scaled clocks are created.

13.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode (freeze mode signal active) the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all eight PWM channels are disabled (PWME7-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

13.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

13.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register and a duty register (each are 8-bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Shown below in Figure 13-19 is the block diagram for the PWM timer.

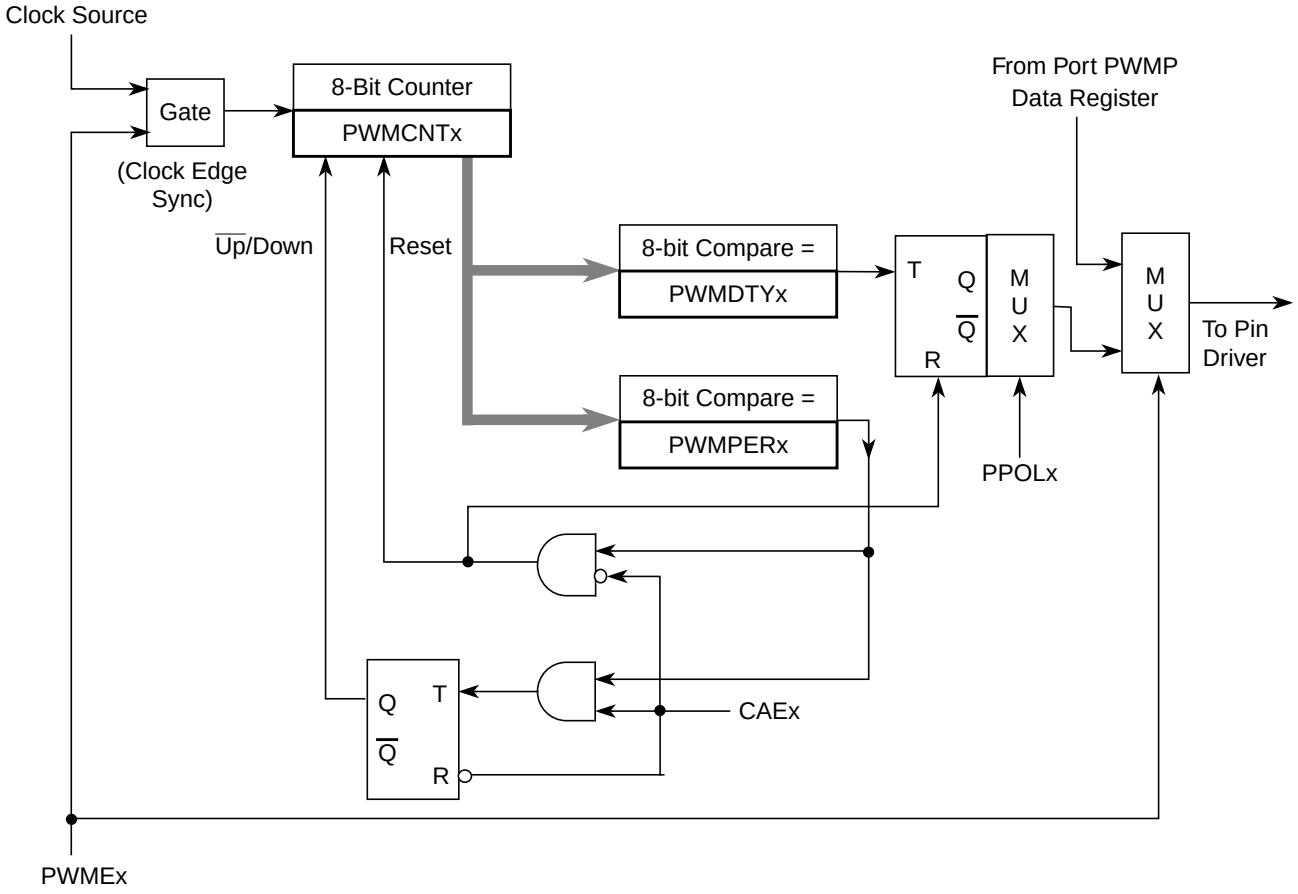

Figure 13-19. PWM Timer Channel Block Diagram

13.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 13.4.2.7, “PWM 16-Bit Functions” for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

Table 14-4. SCICR1 Field Descriptions (continued)

Field	Description
2 ILT	**Idle Line Type Bit** — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
1 PE	**Parity Enable Bit** — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	**Parity Type Bit** — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 14-5. Loop Functions

LOOPS	RSRC	Function
0	x	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

14.4.6.3 Data Sampling

The RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 14-21) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

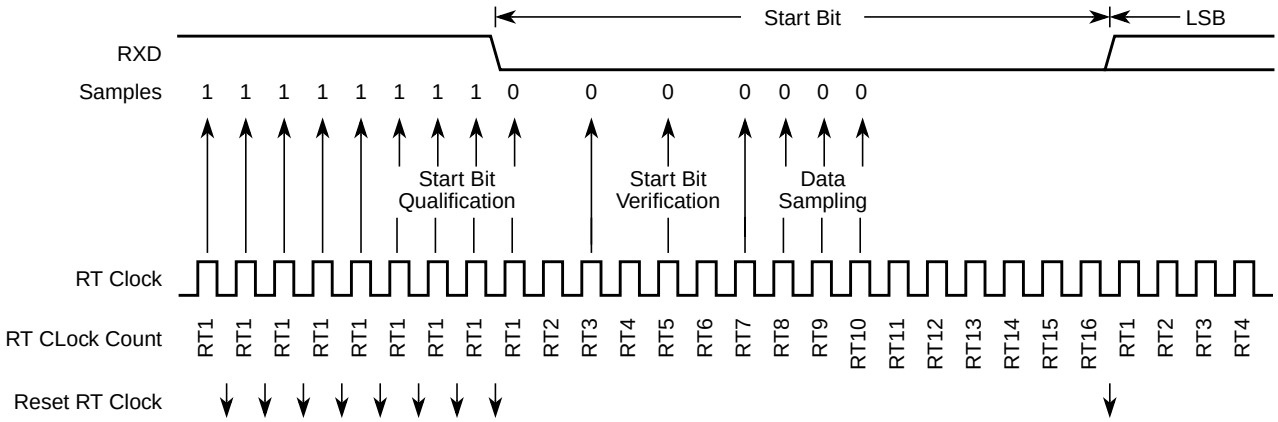

Figure 14-21. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Figure 14-17 summarizes the results of the start bit verification samples.

Table 14-17. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

14.5.3.1 Description of Interrupt Operation

The SCI only originates interrupt requests. The following is a description of how the SCI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent. The SCI only has a single interrupt line (SCI Interrupt Signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

14.5.3.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission.Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

14.5.3.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed. Transmission is completed when all bits including the stop bit (if transmitted) have been shifted out and no data is queued to be transmitted. No stop bit is transmitted when sending a break character and the TC flag is set (providing there is no more data queued for transmission) when the break character has been shifted out. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL).TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

14.5.3.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

14.5.3.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

14.5.3.1.5 IDLE Description

The IDLE interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. Once the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

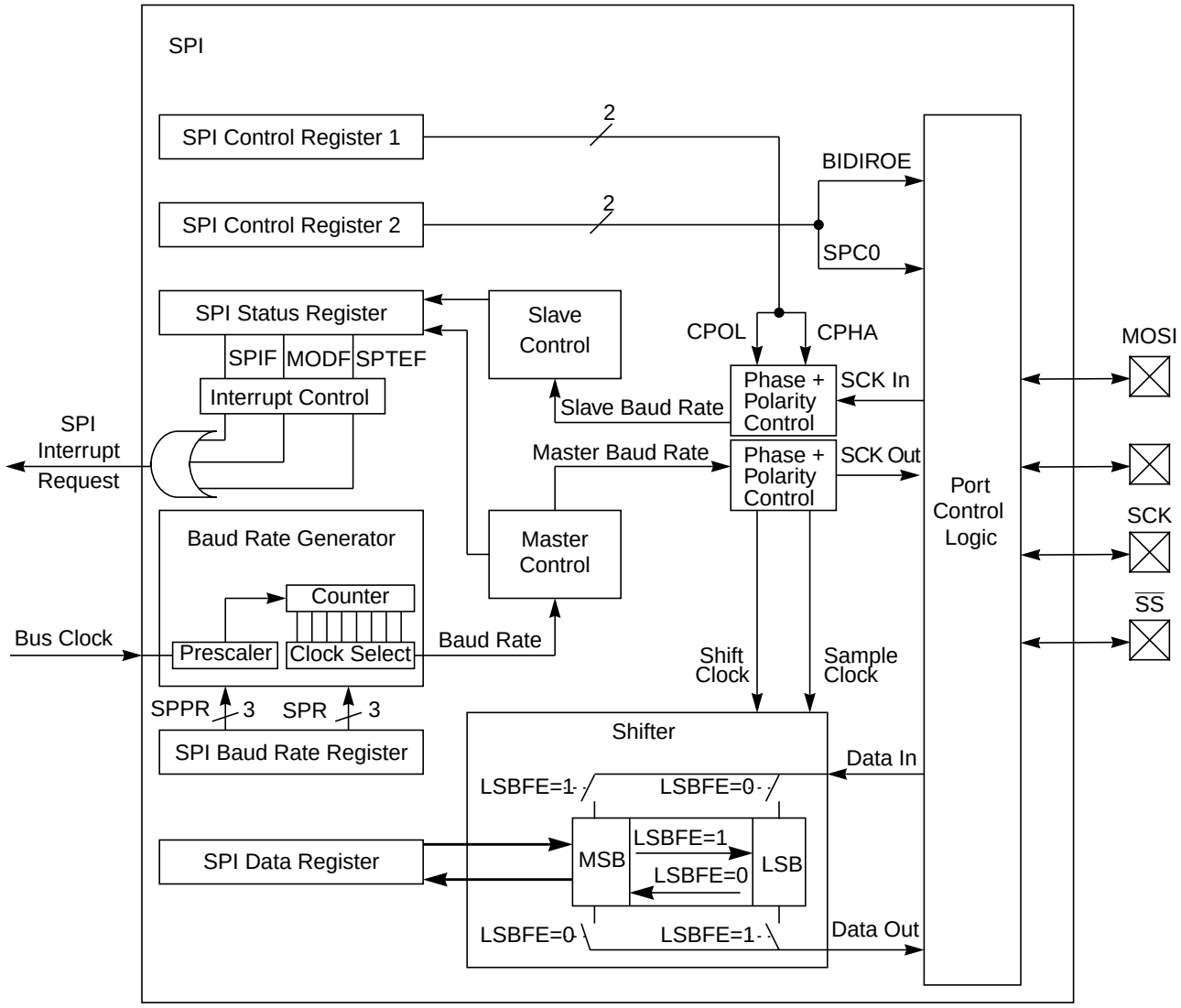

Figure 15-1. SPI Block Diagram

15.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

15.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

15.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

Table 15-1. SPICR1 Field Descriptions (continued)

Field	Description
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 15-2. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in the highest bit position. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 15-2. $\overline{SS}$ Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
0	1	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
1	0	$\overline{SS}$ input with MODF feature	$\overline{SS}$ input
1	1	$\overline{SS}$ is slave select output	$\overline{SS}$ input

15.3.2.2 SPI Control Register 2 (SPICR2)

Module Base +0x0001

	7	6	5	4	3	2	1	0
R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-4. SPI Control Register 2 (SPICR2)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block will return invalid data.

Table 18-36. Read Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 18-26)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

18.4.2.5 Program P-Flash Command

The Program P-Flash operation will program a previously erased phrase in the P-Flash memory using an embedded algorithm.

CAUTION

A P-Flash phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash phrase is not allowed.

Table 18-37. Program P-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x06	Global address [22:16] to identify P-Flash block
001	Global address [15:0] of phrase location to be programmed[1]	
010	Word 0 program value	
011	Word 1 program value	
100	Word 2 program value	
101	Word 3 program value	

1 Global address [2:0] must be 000

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.

Table 19-37. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 19-25)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [22:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

19.3.2.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash block 0. The Program Once reserved field can be read using the Read Once command as described in Section 19.3.2.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash block 0 cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 19-38. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

0x0240–0x029F Port Integration Module (PIM) Map 4 of 4

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0285	PPSR	R	PPSR7	PPSR6	PPSR5	PPSR4	PPSR3	PPSR2	PPSR1	PPSR0
		W								
0x0286	WOMR	R	WOMR7	WOMR6	WOMR5	WOMR4	WOMR3	WOMR2	WOMR1	WOMR0
		W								
0x0287	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0288	PIET	R	PIET7	PIET6	PIET5	PIET4	PIET3	PIET2	PIET1	PIET0
		W								
0x0289	PIFT	R	PIFT7	PIFT6	PIFT5	PIFT4	PIFT3	PIFT2	PIFT1	PIFT0
		W								
0x028A	PIES	R	0	PIES6	PIES5	0	PIES3	PIES2	0	0
		W								
0x028B	PIFS	R	0	PIFS6	PIFS5	0	PIFS3	PIFS2	0	0
		W								
0x028C	PIE1AD	R	PIE1AD7	PIE1AD6	PIE1AD5	PIE1AD4	PIE1AD3	PIE1AD2	PIE1AD1	PIE1AD0
		W								
0x028D	PIF1AD	R	PIF1AD7	PIF1AD6	PIF1AD5	PIF1AD4	PIF1AD3	PIF1AD2	PIF1AD1	PIF1AD0
		W								
0x028E	PIER	R	0	0	0	PIER4	PIER3	PIER2	PIER1	PIER0
		W								
0x028F	PIFR	R	0	0	0	PIFR4	PIFR3	PIFR2	PIFR1	PIFR0
		W								
0x0290	PTU	R	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		W								
0x0291	PTIU	R	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		W								
0x0292	DDRU	R	DDRU7	DDRU6	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		W								
0x0293	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0294	PERU	R	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		W								
0x0295	PPSU	R	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		W								
0x0296	SRRU	R	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		W								
0x0297	PTURR	R	0	0	0	0	PTURR3	PTURR2	0	0
		W								
0x0298	PTV	R	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
		W								
0x0299	PTIV	R	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
		W								
0x029A	DDRV	R	DDRV7	DDRV6	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
		W								
0x029B	Reserved	R	0	0	0	0	0	0	0	0
		W								