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Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	76
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12К х 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xhy256f0mll

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- 16-bit free-running counter with 8-bit precision prescaler
- 1 x 16-bit pulse accumulator

1.3.10 Liquid crystal display driver (LCD)

- Configurable for up to 40 frontplanes and 4 backplanes or general-purpose input or output
- 5 modes of operation allow for different display sizes to meet application requirements
- Unused frontplane and backplane pins can be used as general-purpose I/O

1.3.11 Motor Controller (MC)

- PWM motor controller (MC) with up to 16 high current drivers
- Each PWM channel switchable between two drivers in an H-bridge configuration
- Left, right and center aligned outputs
- Support for sine and cosine drive
- Dithering
- Output slew rate control

1.3.12 Pulse Width Modulation Module (PWM)

- 8channel x 8-bit or 4channel x 16-bit pulse width modulator
 - Programmable period and duty cycle per channel
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies

1.3.13 Inter-IC bus Module (IIC)

- 1 Inter-IC (IIC) bus module which has following feature
 - Multi-master operation
 - Soft programming for one of 256 different serial clock frequencies
 - General Call(Broadcast) mode support
 - 10-bit address support

1.3.14 Controller Area Network Module (MSCAN)

- 1 Mbit per second, CAN 2.0 A, B software compatible
 - Standard and extended data frames
 - 0–8 bytes data length
 - Programmable bit rate up to 1 Mbps
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization
- Flexible identifier acceptance filter programmable as:

Background Debug Module (S12XBDMV2)

16-bit misaligned reads and writes are generally not allowed. If attempted by BDM hardware command, the BDM will ignore the least significant bit of the address and will assume an even address from the remaining bits.

For devices with external bus:

The following cycle count information is only valid when the external wait function is not used (see wait bit of EBI sub-block). During an external wait the BDM can not steal a cycle. Hence be careful with the external wait function if the BDM serial interface is much faster than the bus, because of the BDM soft-reset after time-out (see Section 5.4.11, "Serial Communication Time Out").

For hardware data read commands, the external host must wait at least 150 bus clock cycles after sending the address before attempting to obtain the read data. This is to be certain that valid data is available in the BDM shift register, ready to be shifted out. For hardware write commands, the external host must wait 150 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed. The 150 bus clock cycle delay in both cases includes the maximum 128 cycle delay that can be incurred as the BDM waits for a free cycle before stealing a cycle.

For firmware read commands, the external host should wait at least 48 bus clock cycles after sending the command opcode and before attempting to obtain the read data. This includes the potential of extra cycles when the access is external and stretched (+1 to maximum +7 cycles) or to registers of the PRU (port replacement unit) in emulation modes (if modes available). The 48 cycle wait allows enough time for the requested data to be made available in the BDM shift register, ready to be shifted out.

NOTE

This timing has increased from previous BDM modules due to the new capability in which the BDM serial interface can potentially run faster than the bus. On previous BDM modules this extra time could be hidden within the serial time.

For firmware write commands, the external host must wait 36 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed.

The external host should wait at least for 76 bus clock cycles after a TRACE1 or GO command before starting any new serial command. This is to allow the CPU to exit gracefully from the standard BDM firmware lookup table and resume execution of the user code. Disturbing the BDM shift register prematurely may adversely affect the exit from the standard BDM firmware lookup table.

NOTE

If the bus rate of the target processor is unknown or could be changing or the external wait function is used, it is recommended that the ACK (acknowledge function) is used to indicate when an operation is complete. When using ACK, the delay times are automated.

Table 6-4. DBGC1 Field Descriptions (continued)

Field	Description
3 DBGBRK	 S12XDBG Breakpoint Enable Bit — The DBGBRK bit controls whether the debugger will request a breakpoint to S12XCPU upon reaching the state sequencer Final State. If tracing is enabled, the breakpoint is generated on completion of the tracing session. If tracing is not enabled, the breakpoint is generated immediately. Please refer to Section 6.4.7 for further details. No breakpoint on trigger. Breakpoint on trigger
1–0 COMRV	Comparator Register Visibility Bits — These bits determine which bank of comparator register is visible in the 8-byte window of the S12XDBG module address map, located between 0x0028 to 0x002F. Furthermore these bits determine which register is visible at the address 0x0027. See Table 6-5.

Table 6-5. COMRV Encoding

COMRV	Visible Comparator	Visible Register at 0x0027
00	Comparator A	DBGSCR1
01	Comparator B	DBGSCR2
10	Comparator C	DBGSCR3
11	Comparator D	DBGMFR

6.3.2.2 Debug Status Register (DBGSR)

Address: 0x0021



Figure 6-4. Debug Status Register (DBGSR)

Read: Anytime

Write: Never

Table 6-6. DBGSR Field Descriptions

Field	Description
7 TBF	Trace Buffer Full — The TBF bit indicates that the trace buffer has stored 64 or more lines of data since it was last armed. If this bit is set, then all 64 lines will be valid data, regardless of the value of DBGCNT bits CNT[6:0]. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit
2–0 SSF[2:0]	State Sequencer Flag Bits — The SSF bits indicate in which state the State Sequencer is currently in. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal trigger, then the state sequencer returns to state0 and these bits are cleared to indicate that state0 was entered during the session. On arming the module the state sequencer enters state1 and these bits are forced to SSF[2:0] = 001. See Table 6-7.

SC[3:0]	Description	
0111	Match1 triggers to State3 Match0 triggers Final State Other matches have no effect	
1000	Match0 triggers to State2 Match2 triggers to State3 Other matches have no effect	
1001	Match2 triggers to State3 Match0 triggers Final State Other matches have no effect	
1010	Match1 triggers to State2 Match3 triggers to State3 Other matches have no effect	
1011	Match3 triggers to State3 Match1 triggers to Final State Other matches have no effect	
1100	Match3 has no effect All other matches (M0,M1,M2) trigger to State2	
1101	Reserved. (No match triggers state sequencer transition)	
1110	Reserved. (No match triggers state sequencer transition)	
1111	Reserved. (No match triggers state sequencer transition)	

The trigger priorities described in Table 6-39 dictate that in the case of simultaneous matches, the match on the lower channel number (0,1,2,3) has priority. The SC[3:0] encoding ensures that a match leading to final state has priority over all other matches.

6.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Address: 0x0027



Figure 6-10. Debug State Control Register 2 (DBGSCR2)

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and S12XDBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.8.1". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-21. DBGSCR2 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 6-22. State2 — Sequencer Next State Selection

SC[3:0]	Description	
0000	Any match triggers to state1	
0001	Any match triggers to state3	
0010	Any match triggers to Final State	
0011	Match3 triggers to State1 Other matches have no effect	
0100	Match3 triggers to State3 Other matches have no effect	

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unimplemented bus, thus preventing proper operation.

The DBGC1_COMRV bits determine which comparator control, address, data and datamask registers are visible in the 8-byte window from 0x0028 to 0x002F as shown in Section Table 6-26.

Table 6-26. Comparator Address Register Visibility

COMRV	Visible Comparator	
00	DBGACTL, DBGAAH ,DBGAAM, DBGAAL, DBGADH, DBGADL, DBGADHM, DBGADLM	
01	DBGBCTL, DBGBAH, DBGBAM, DBGBAL	
10	DBGCCTL, DBGCAH, DBGCAM, DBGCAL, DBGCDH, DBGCDL, DBGCDHM, DBGCDLM	
11	DBGDCTL, DBGDAH, DBGDAM, DBGDAL	

Table 6-27. DBGXCTL Field Descriptions

Field	Description
7 SZE (Comparators B and D)	 Size Comparator Enable Bit — The SZE bit controls whether access size comparison is enabled for the associated comparator. This bit is ignored if the TAG bit in the same register is set. 0 Word/Byte access size is not used in comparison 1 Word/Byte access size is used in comparison
6 NDB (Comparators A and C	 Not Data Bus — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. Furthermore data bus bits can be individually masked using the comparator data mask registers. This bit is only available for comparators A and C. This bit is ignored if the TAG bit in the same register is set. This bit position has an SZ functionality for comparators B and D. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
6 SZ (Comparators B and D)	Size Comparator Value Bit — The SZ bit selects either word or byte access size in comparison for the associated comparator. This bit is ignored if the SZE bit is cleared or if the TAG bit in the same register is set. This bit position has NDB functionality for comparators A and C 0 Word access size will be compared 1 Byte access size will be compared
5 TAG	 Tag Select — This bit controls whether the comparator match will cause a trigger or tag the opcode at the matched address. Tagged opcodes trigger only if they reach the execution stage of the instruction queue. 0 Trigger immediately on match 1 On match, tag the opcode. If the opcode is about to be executed a trigger is generated
4 BRK	 Break — This bit controls whether a channel match terminates a debug session immediately, independent of state sequencer state. To generate an immediate breakpoint the module breakpoints must be enabled using DBGBRK. 0 The debug session termination is dependent upon the state sequencer and trigger conditions. 1 A match on this channel terminates the debug session immediately; breakpoints if active are generated, tracing, if active, is terminated and the module disarmed.
3 RW	 Read/Write Comparator Value Bit — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is not used if RWE = 0. 0 Write cycle will be matched 1 Read cycle will be matched
2 RWE	Read/Write Enable Bit — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is not used for tagged operations. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison



7.5 Resets

All reset sources are listed in Table 7-16. Refer to MCU specification for related vector addresses and priorities.

Reset Source	Local Enable
Power on Reset	None
Low Voltage Reset	None
External Reset	None
Illegal Address Reset	None
Clock Monitor Reset	PLLCTL (CME=1, SCME=0)

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Freescale's Scalable Controller Area Network (S12MSCANV3)

generates a receive interrupt¹² (see Section 11.4.7.3, "Receive Interrupt") to the CPU. The user's receive handler must read the received message from the RxFG and then reset the RXF flag to acknowledge the interrupt and to release the foreground buffer. A new message, which can follow immediately after the IFS field of the CAN frame, is received into the next available RxBG. If the MSCAN receives an invalid message in its RxBG (wrong identifier, transmission errors, etc.) the actual contents of the buffer will be over-written by the next message. The buffer will then not be shifted into the FIFO.

When the MSCAN module is transmitting, the MSCAN receives its own transmitted messages into the background receive buffer, RxBG, but does not shift it into the receiver FIFO, generate a receive interrupt, or acknowledge its own messages on the CAN bus. The exception to this rule is in loopback mode (see Section 11.3.2.2, "MSCAN Control Register 1 (CANCTL1)") where the MSCAN treats its own messages exactly like all other incoming messages. The MSCAN receives its own transmitted messages in the event that it loses arbitration. If arbitration is lost, the MSCAN must be prepared to become a receiver.

An overrun condition occurs when all receive message buffers in the FIFO are filled with correctly received messages with accepted identifiers and another message is correctly received from the CAN bus with an accepted identifier. The latter message is discarded and an error interrupt with overrun indication is generated if enabled (see Section 11.4.7.5, "Error Interrupt"). The MSCAN remains able to transmit messages while the receiver FIFO is being filled, but all incoming messages are discarded. As soon as a receive buffer in the FIFO is available again, new valid messages will be accepted.

11.4.3 Identifier Acceptance Filter

The MSCAN identifier acceptance registers (see Section 11.3.2.12, "MSCAN Identifier Acceptance Control Register (CANIDAC)") define the acceptable patterns of the standard or extended identifier (ID[10:0] or ID[28:0]). Any of these bits can be marked 'don't care' in the MSCAN identifier mask registers (see Section 11.3.2.18, "MSCAN Identifier Mask Registers (CANIDMR0–CANIDMR7)").

A filter hit is indicated to the application software by a set receive buffer full flag (RXF = 1) and three bits in the CANIDAC register (see Section 11.3.2.12, "MSCAN Identifier Acceptance Control Register (CANIDAC)"). These identifier hit flags (IDHIT[2:0]) clearly identify the filter section that caused the acceptance. They simplify the application software's task to identify the cause of the receiver interrupt. If more than one hit occurs (two or more filters match), the lower hit has priority.

A very flexible programmable generic identifier acceptance filter has been introduced to reduce the CPU interrupt loading. The filter is programmable to operate in four different modes:

- Two identifier acceptance filters, each to be applied to:
 - The full 29 bits of the extended identifier and to the following bits of the CAN 2.0B frame:
 - Remote transmission request (RTR)
 - Identifier extension (IDE)
 - Substitute remote request (SRR)
 - The 11 bits of the standard identifier plus the RTR and IDE bits of the CAN 2.0A/B messages. This mode implements two filters for a full length CAN 2.0B compliant extended identifier. Although this mode can be used for standard identifiers, it is recommended to use the four or eight identifier acceptance filters.

12. The receive interrupt occurs only if not masked. A polling scheme can be applied on RXF also.

Freescale's Scalable Controller Area Network (S12MSCANV3)

11.4.5.7 Disabled Mode

The MSCAN is in disabled mode out of reset (CANE=0). All module clocks are stopped for power saving, however the register map can still be accessed as specified.

11.4.5.8 Programmable Wake-Up Function

The MSCAN can be programmed to wake up from sleep or power down mode as soon as CAN bus activity is detected (see control bit WUPE in MSCAN Control Register 0 (CANCTL0). The sensitivity to existing CAN bus action can be modified by applying a low-pass filter function to the RXCAN input line (see control bit WUPM in Section 11.3.2.2, "MSCAN Control Register 1 (CANCTL1)").

This feature can be used to protect the MSCAN from wake-up due to short glitches on the CAN bus lines. Such glitches can result from—for example—electromagnetic interference within noisy environments.

11.4.6 Reset Initialization

The reset state of each individual bit is listed in Section 11.3.2, "Register Descriptions," which details all the registers and their bit-fields.

11.4.7 Interrupts

This section describes all interrupts originated by the MSCAN. It documents the enable bits and generated flags. Each interrupt is listed and described separately.

11.4.7.1 Description of Interrupt Operation

The MSCAN supports four interrupt vectors (see Table 11-39), any of which can be individually masked (for details see Section 11.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)" to Section 11.3.2.8, "MSCAN Transmitter Interrupt Enable Register (CANTIER)").

Refer to the device overview section to determine the dedicated interrupt vector addresses.

Interrupt Source	CCR Mask	Local Enable
Wake-Up Interrupt (WUPIF)	l bit	CANRIER (WUPIE)
Error Interrupts Interrupt (CSCIF, OVRIF)	l bit	CANRIER (CSCIE, OVRIE)
Receive Interrupt (RXF)	l bit	CANRIER (RXFIE)
Transmit Interrupts (TXE[2:0])	l bit	CANTIER (TXEIE[2:0])

Table 11-39. Interrupt Vectors

11.4.7.2 Transmit Interrupt

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXEx flag of the empty message buffer is set.

12.1.2 Modes of Operation

The IIC functions the same in normal, special, and emulation modes. It has two low power modes: wait and stop modes.

12.1.3 Block Diagram

The block diagram of the IIC module is shown in Figure 12-1.



Figure 12-1. IIC Block Diagram

Pulse-Width Modulator (S12PWM8B8CV1)

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to \$00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing "0" to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new "clean" PWM waveform without any "history" from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 13.4.2.5, "Left Aligned Outputs" and Section 13.4.2.6, "Center Aligned Outputs" for more details).

Counter Clears (\$00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in	When PWM channel is disabled (PWMEx = 0)
Effective period ends	PWMCNTx.	

13.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 13-19. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 13-19, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 13.4.2.3, "PWM Period and Duty". The counter counts from 0 to the value in the period register -1.

14.3.2.1 SCI Baud Rate Registers (SCIBDH, SCIBDL)

Module Base + 0x0000



SBR7 SBR6 SBR5 SBR4 SBR3 SBR2 SBR1 SBR0 W 0 0 0 0 0 0 Reset 1 0

Figure 14-4. SCI Baud Rate Register (SCIBDL)

Read: Anytime, if AMAP = 0. If only SCIBDH is written to, a read will not return the correct data until SCIBDL is written to as well, following a write to SCIBDH.

Write: Anytime, if AMAP = 0.

NOTE

Those two registers are only visible in the memory map if AMAP = 0 (reset condition).

The SCI baud rate register is used by to determine the baud rate of the SCI, and to control the infrared modulation/demodulation submodule.

Table 14-2.	SCIBDH	and	SCIBDL	Field	Descriptions
-------------	--------	-----	--------	-------	--------------

Field	Description
7 IREN	 Infrared Enable Bit — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	Transmitter Narrow Pulse Bits — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 14-3.
4:0 7:0 SBR[12:0]	 SCI Baud Rate Bits — The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit. The formulas for calculating the baud rate are: When IREN = 0 then, SCI baud rate = SCI bus clock / (16 x SBR[12:0]) When IREN = 1 then, SCI baud rate = SCI bus clock / (32 x SBR[12:1]) Note: The baud rate generator is disabled after reset and not started until the TE bit or the RE bit is set for the first time. The baud rate generator is disabled when (SBR[12:0] = 0 and IREN = 0) or (SBR[12:1] = 0 and IREN = 1). Note: Writing to SCIBDH has no effect without writing to SCIBDL, because writing to SCIBDH puts the data in a temporary location until SCIBDL is written to.

14.4.1 Infrared Interface Submodule

This module provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI. The IrDA physical layer specification defines a half-duplex infrared communication link for exchange data. The full standard includes data rates up to 16 Mbits/s. This design covers only data rates between 2.4 Kbits/s and 115.2 Kbits/s.

The infrared submodule consists of two major blocks: the transmit encoder and the receive decoder. The SCI transmits serial bits of data which are encoded by the infrared submodule to transmit a narrow pulse for every zero bit. No pulse is transmitted for every one bit. When receiving data, the IR pulses should be detected using an IR photo diode and transformed to CMOS levels by the IR receive decoder (external from the MCU). The narrow pulses are then stretched by the infrared submodule to get back to a serial bit stream to be received by the SCI. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct connection can be made to external IrDA transceiver modules that uses active low pulses.

The infrared submodule receives its clock sources from the SCI. One of these two clocks are selected in the infrared submodule in order to generate either 3/16, 1/16, 1/32 or 1/4 narrow pulses during transmission. The infrared block receives two clock sources from the SCI, R16XCLK and R32XCLK, which are configured to generate the narrow pulse width during transmission. The R16XCLK and R32XCLK are internal clocks with frequencies 16 and 32 times the baud rate respectively. Both R16XCLK and R32XCLK clocks are used for transmitting data. The receive decoder uses only the R16XCLK clock.

14.4.1.1 Infrared Transmit Encoder

The infrared transmit encoder converts serial bits of data from transmit shift register to the TXD pin. A narrow pulse is transmitted for a zero bit and no pulse for a one bit. The narrow pulse is sent in the middle of the bit with a duration of 1/32, 1/16, 3/16 or 1/4 of a bit time. A narrow high pulse is transmitted for a zero bit when TXPOL is cleared, while a narrow low pulse is transmitted for a zero bit when TXPOL is set.

14.4.1.2 Infrared Receive Decoder

The infrared receive block converts data from the RXD pin to the receive shift register. A narrow pulse is expected for each zero received and no pulse is expected for each one received. A narrow high pulse is expected for a zero bit when RXPOL is cleared, while a narrow low pulse is expected for a zero bit when RXPOL is set. This receive decoder meets the edge jitter requirement as defined by the IrDA serial infrared physical layer specification.

14.4.2 LIN Support

This module provides some basic support for the LIN protocol. At first this is a break detect circuitry making it easier for the LIN software to distinguish a break character from an incoming data stream. As a further addition is supports a collision detection at the bit level as well as cancelling pending transmissions.

Serial Peripheral Interface (S12SPIV5)

SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPICR2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in run mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of data continues, so that the slave stays synchronized to the master.

• Stop mode

The SPI is inactive in stop mode for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of data continues, so that the slave stays synchronized to the master.

For a detailed description of operating modes, please refer to Section 15.4.7, "Low Power Mode Options".

15.1.4 Block Diagram

Figure 15-1 gives an overview on the SPI architecture. The main parts of the SPI are status, control and data registers, shifter logic, baud rate generator, master/slave control logic, and port control logic.

16.2.7 IOC1 — Input Capture and Output Compare Channel 1 Pin

This pin serves as input capture or output compare for channel 1.

16.2.8 IOC0 — Input Capture and Output Compare Channel 0 Pin

This pin serves as input capture or output compare for channel 0.

NOTE

For the description of interrupts see Section 16.6, "Interrupts".

16.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

16.3.1 Module Memory Map

The memory map for the TIM16B8CV2 module is given below in Figure 16-5. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B8CV2 module and the address offset for each register.

16.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R W	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
0x0001 CFORC	R W	0 FOC7	0 FOC6	0 FOC5	0 FOC4	0 FOC3	0 FOC2	0 FOC1	0 FOC0
0x0002 OC7M	R W	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
0x0003 OC7D	R W	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
0x0004 TCNTH	R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
0x0005 TCNTL	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0

= Unimplemented or Reserved

Figure 16-5. TIM16B8CV2 Register Summary (Sheet 1 of 3)

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256 KByte Flash Module (S12XFTMR256K1V1)

Register	Error Bit	Error Condition
	400500	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 18-26)
	ACCERK	Set if an invalid phrase index is supplied
FSTAT FPVIOL MGSTAT1 MGSTAT0		Set if the requested phrase has already been programmed ¹
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 18-40. Program Once Command Error Handling

18.4.2.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and D-Flash memory space.

Table 18-41. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Register	Error Bit	Error Condition
FSTAT FPVIOL MGSTAT1 MGSTAT0		Set if CCOBIX[2:0] != 000 at command launch
	ACCERK	Set if command not available in current mode (see Table 18-26)
	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 18-42. Erase All Blocks Command Error Handling

18.4.2.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or D-Flash block.

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19.2.1.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU or XGATE.



Figure 19-6. Flash Configuration Register (FCNFG)

CCIE, IGNSF, FDFD, and FSFD bits are readable and writable while remaining bits read 0 and are not writable.

Field	Description
7 CCIE	 Command Complete Interrupt Enable — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 19.2.1.7)
4 IGNSF	 Ignore Single Bit Fault — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 19.2.1.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
1 FDFD	 Force Double Bit Fault Detect — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. The FECCR registers will not be updated during the Flash array read operation with FDFD set unless an actual double bit fault is detected. 0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected 1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see Section 19.2.1.7) and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see Section 19.2.1.6)
0 FSFD	 Force Single Bit Fault Detect — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. The FECCR registers will not be updated during the Flash array read operation with FSFD set unless an actual single bit fault is detected. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see Section 19.2.1.7) and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see Section 19.2.1.6)

Table 19-10. FCNFG Field Descriptions

19.2.1.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

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DPS[4:0]	Global Address Range	Protected Size
1_0110	0x10_0000 - 0x10_16FF	5888 bytes
1_0111	0x10_0000 – 0x10_17FF	6144 bytes
1_1000	0x10_0000 – 0x10_18FF	6400 bytes
1_1001	0x10_0000 – 0x10_19FF	6656 bytes
1_1010	0x10_0000 – 0x10_1AFF	6912 bytes
1_1011	0x10_0000 – 0x10_1BFF	7168 bytes
1_1100	0x10_0000 - 0x10_1CFF	7424 bytes
1_1101	0x10_0000 – 0x10_1DFF	7680 bytes
1_1110	0x10_0000 - 0x10_1EFF	7936 bytes
1_1111	0x10_0000 – 0x10_1FFF	8192 bytes

Table 19-20. D-Flash Protection Address Range

19.2.1.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.



19.2.1.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes

Register	Error Bit	Error Condition
	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 19-25)
		Set if an invalid global address [22:0] is supplied
FSTAT		Set if a misaligned word address is supplied (global address [0] != 0)
FPVIOL MGSTAT1 MGSTAT0	FPVIOL	Set if the selected area of the D-Flash memory is protected
	Set if any errors have been encountered during the verify operation	
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 19-61. Erase D-Flash Sector Command Error Handling

19.3.3 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	l Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	l Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	l Bit

Table 19-62. Flash Interrupt Sources

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

19.3.3.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with the DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 19.2.1.5, "Flash Configuration Register (FCNFG)", Section 19.2.1.6, "Flash Error Configuration Register (FERCNFG)", Section 19.2.1.7, "Flash Status Register (FSTAT)", and Section 19.2.1.8, "Flash Error Status Register (FERSTAT)".

The logic used for generating the Flash module interrupts is shown in Figure 19-24.

Num	Rating	Symbol	Min	Мах	Unit
1	I/O, regulator and analog supply voltage	V _{DD35}	-0.3	6.0	V
2	Digital logic supply voltage ²	V _{DD}	-0.3	2.16	V
3	PLL supply voltage ²	V _{DDPLL}	-0.3	2.16	V
4	NVM supply voltage ²	V _{DDF}	-0.3	3.6	V
5	Voltage difference V _{DDX} to V _{DDA}	Δ_{VDDX}	-0.3	0.3	V
6	Voltage difference V _{SSX} to V _{SSA}	Δ_{VSSX}	-0.3	0.3	V
5	Voltage difference V _{DDM1,2} to V _{DDA}	$\Delta_{\rm VDDMA}$	-0.3	0.3	V
6	Voltage difference V _{SSM1,2} to V _{SSA}	$\Delta_{\rm VSSMA}$	-0.3	0.3	V
7	Digital I/O input voltage	V _{IN}	-0.3	6.0	V
8	Analog reference	V _{RH,} V _{RL}	-0.3	6.0	V
9	EXTAL, XTAL	V _{ILV}	-0.3	2.16	V
11	Instantaneous maximum current Single pin limit for all digital I/O pins ³	Ι _D	-25	+25	mA
12	Instantaneous maximum current Single pin limit for EXTAL, XTAL ⁴	I _{DL}	-25	+25	mA
14	Maximum current Single pin limit for power supply pins	I _{DV}	-100	+100	mA
15	Storage temperature range	T _{stg}	-65	155	°C

Table A-1. Absolute Maximum Ratings¹

Beyond absolute maximum ratings device might be damaged. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX} , or V_{SSA} and V_{DDA} . Those pins are internally clamped to V_{SSPLL} and V_{DDPLL} . 2

3

ESD Protection and Latch-up Immunity A.1.6

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

0x0010–0x0017 Module Mapping Control (S12XMMC) Map 2 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0,0012	Reserved	R	0	0	0	0	0	0	0	0
00012	Reserved	W								
0v0013		R	MGRAMO	0		PGMIFRO	0	0	0	0
00013	WINCCTLT ,	W	Ν			N				
0x0014	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0015	PPAGE	R	PIX7	PIX6	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
0,0010		0 11/102	W					1 0.00	1 0.02	
0x0016	RPAGE	R	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
0.0010		W						=		
0x0017	EPAGE	R	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
	LINGE	W	<i>.</i>	0			0	<u>_</u>		0

0x0018–0x0019 Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0018	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0019	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x001A-0x001B Device ID register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x001A	PARTIDH						PAR	TIDH			
		W									
0x001B	PARTIDL	R				PAR	TIDL				
		W									

0x001C-0x001F Port Integration Module (PIM) Map 3 of 4

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x001C	ECLKCTL	R W	NECLK	0	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0	
0x001D	Reserved	Reserved	R	0	0	0	0	0	0	0	0
			W								
0x001E	IRQCR	R				0	0	0	0	0	
		W									
0x001F	Reserved	R	0	0	0	0	0	0	0	0	
		W									