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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	88
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xhy256f0mlm

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0272 DDR0AD	R	0	0	0	0	DDR0AD3	DDR0AD2	DDR0AD1	DDR0AD0
	W								
0x0273 DDR1AD	R	DDR1AD7	DDR1AD6	DDR1AD5	DDR1AD4	DDR1AD3	DDR1AD2	DDR1AD1	DDR1AD0
	W								
0x0274 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0275 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0276 PER0AD	R	0	0	0	0	PER0AD3	PER0AD2	PER0AD1	PER0AD0
	W								
0x0277 PER1AD	R	PER1AD7	PER1AD6	PER1AD5	PER1AD4	PER1AD3	PER1AD2	PER1AD1	PER1AD0
	W								
0x0278 -0x027F Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0280 PTR	R	PTR7	PTR6	PTR5	PTR4	PTR3	PTR2	PTR1	PTR0
	W								
0x0281 PTIR	R	PTIR7	PTIR6	PTIR5	PTIR4	PTIR3	PTIR2	PTIR1	PTIR0
	W								
0x0282 DDRR	R	DDRR7	DDRR6	DDRR5	DDRR4	DDRR3	DDRR2	DDRR1	DDRR0
	W								
0x0283 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0284 PERR	R	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0
	W								
0x0285 PPSR	R	PPSR7	PPSR6	PPSR5	PPSR4	PPSR3	PPSR2	PPSR1	PPSR0
	W								
0x0286 WOMR	R	WOMR7	WOMR6	WOMR5	WOMR4	WOMR3	WOMR2	WOMR1	WOMR0
	W								
0x0287 Reserved	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Table 2-8. PUCR Register Field Descriptions

Field	Description
6 BKPUE	**BKGD pin pull-up Enable**—Enable pull-up device on pin This bit configures whether a pull-up device is activated, if the pin is used as input. If a pin is used as output this bit has no effect. 1 Pull-up device enabled 0 Pull-up device disabled
1 PUPBE	**Port B Pull-down Enable**—Enable pull-down devices on all port input pins This bit configures whether a pull-down device is activated on all associated port input pins. If a pin is used as output this bit has no effect. 1 pull-down device enabled 0 pull-down device disabled
0 PUPAE	**Port A Pull-down Enable**—Enable pull-down devices on all port input pins This bit configures whether a pull-down device is activated on all associated port input pins. If a pin is used as output this bit has no effect. 1 pull-down device enabled 0 pull-down device disabled

2.3.9 PIM Reserved Register

Address 0x000D (PRR) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-7. PIM Reserved Register

[1] Read: Anytime
Write: Anytime

Table 2-57. WOMR Register Field Descriptions

Field	Description
7-0 WOMR	**Port R wired-or mode**—Enable wired-or functionality This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven.This allows a multipoint connection of several serial modules. These bits have no influence on pins used as inputs. 1 Output buffers operate as open-drain outputs. 0 Output buffers operate as push-pull outputs.

2.3.72 PIM Reserved Registers

Address 0x0287 Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved u = Unaffected by reset

Figure 2-69. PIM Reserved Registers

1 Read: Always reads 0x00
Write: Unimplemented

2.3.73 Port T Interrupt Enable Register (PIET)

Read: Anytime.

Address 0x0288 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIET7	PIET6	PIET5	PIET4	PIET3	PIET2	PIET1	PIET0
Reset	0	0	0	0	0	0	0	0

Figure 2-70. Port TInterrupt Enable Register (PIET)

1 Read: Anytime.
Write: Anytime.

Table 2-58. PIET Register Field Descriptions

Field	Description
7-0 PIET	**Port T interrupt enable**— This register disables or enables on a per-pin basis the edge sensitive external interrupt associated with Port T. 1 Interrupt is enabled. 0 Interrupt is disabled (interrupt flag masked).

2.3.78 Port AD Interrupt Flag Register (PIF1AD)

Address 0x028D Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIF1AD7	PIF1AD6	PIF1AD5	PIF1AD4	PIF1AD3	PIF1AD2	PIF1AD1	PIF1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-75. Port F Interrupt Flag Register (PIF1AD)

1 Read: Anytime.
Write: Anytime.

Table 2-63. PIF1AD Register Field Descriptions

Field	Description
7-0 PIF1AD	**Port AD interrupt flag**— Each flag is set by an active edge on the associated input pin. To clear this flag, write logic level 1 to the corresponding bit in the PIF1AD register. Writing a 0 has no effect. [1] 1 Active falling edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). 0 No active edge pending.

1 In order to enable the Key Wakeup function, need to set the ATDIENL first.

2.3.79 Port R Interrupt Enable Register (PIER)

Address 0x028E Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	PIER4	PIER3	PIER2	PIER1	PIER0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-76. Port R Interrupt Enable Register (PIER)

1 Read: Anytime.
Write: Anytime.

Table 2-64. PIER Register Field Descriptions

Field	Description
4-0 PIER	**Port R interrupt enable**— This register disables or enables on a per-pin basis the edge sensitive external interrupt associated with Port R. 1 Interrupt is enabled. 0 Interrupt is disabled (interrupt flag masked).

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the XINT module.

4.3.1 Module Memory Map

Table 4-3 gives an overview over all XINT module registers.

Table 4-3. XINT Memory Map

Address	Use	Access
0x0120	RESERVED	—
0x0121	Interrupt Vector Base Register (IVBR)	R/W
0x0122–0x0125	RESERVED	—
0x0126	XGATE Interrupt Priority Configuration Register (INT_XGPRIO)	R/W
0x0127	Interrupt Request Configuration Address Register (INT_CFADDR)	R/W
0x0128	Interrupt Request Configuration Data Register 0 (INT_CFDATA0)	R/W
0x0129	Interrupt Request Configuration Data Register 1 (INT_CFDATA1)	R/W
0x012A	Interrupt Request Configuration Data Register 2 (INT_CFDATA2	R/W
0x012B	Interrupt Request Configuration Data Register 3 (INT_CFDATA3)	R/W
0x012C	Interrupt Request Configuration Data Register 4 (INT_CFDATA4)	R/W
0x012D	Interrupt Request Configuration Data Register 5 (INT_CFDATA5)	R/W
0x012E	Interrupt Request Configuration Data Register 6 (INT_CFDATA6)	R/W
0x012F	Interrupt Request Configuration Data Register 7 (INT_CFDATA7)	R/W

when the opcode is fetched from the memory. This precedes the instruction execution by an indefinite number of cycles due to instruction pipe lining. For a comparator match of an opcode at an odd address when TAG = 0, the corresponding even address must be contained in the comparator register. Thus for an opcode at odd address (n), the comparator register must contain address (n–1).

Once a successful comparator match has occurred, the condition that caused the original match is not verified again on subsequent matches. Thus if a particular data value is verified at a given address, this address may not still contain that data value when a subsequent match occurs.

Comparators C and D can also be used to select an address range to trace from. This is determined by the TRANGE bits in the DBGTCR register. The TRANGE encoding is shown in Table 6-9. If the TRANGE bits select a range definition using comparator D, then comparator D is configured for trace range definition and cannot be used for address bus comparisons. Similarly if the TRANGE bits select a range definition using comparator C, then comparator C is configured for trace range definition and cannot be used for address bus comparisons.

Match[0, 1, 2, 3] map directly to Comparators[A, B, C, D] respectively, except in range modes (see Section 6.3.2.4"). Comparator priority rules are described in the trigger priority section (Section 6.4.3.4").

6.4.2.1 Exact Address Comparator Match (Comparators A and C)

With range comparisons disabled, the match condition is an exact equivalence of address/data bus with the value stored in the comparator address/data registers. Further qualification of the type of access (R/W, word/byte) is possible.

Comparators A and C do not feature SZE or SZ control bits, thus the access size is not compared. Table 6-37 lists access considerations without data bus compare. Table 6-36 lists access considerations with data bus comparison. To compare byte accesses DBGxDH must be loaded with the data byte, the low byte must be masked out using the DBGxDLM mask register. On word accesses the data byte of the lower address is mapped to DBGxDH.

Table 6-36. Comparator A and C Data Bus Considerations

Access	Address	DBGxDH	DBGxDL	DBGxDHM	DBGxDLM	Example Valid Match	
Word	ADDR[n]	Data[n]	Data[n+1]	$FF	$FF	MOVW #$WORD ADDR[n]	config1
Byte	ADDR[n]	Data[n]	x	$FF	$00	MOVB #$BYTE ADDR[n]	config2
Word	ADDR[n]	Data[n]	x	$FF	$00	MOVW #$WORD ADDR[n]	config2
Word	ADDR[n]	x	Data[n+1]	$00	$FF	MOVW #$WORD ADDR[n]	config3

Code may contain various access forms of the same address, i.e. a word access of ADDR[n] or byte access of ADDR[n+1] both access n+1. At a word access of ADDR[n], address ADDR[n+1] does not appear on the address bus and so cannot cause a comparator match if the comparator contains ADDR[n]. Thus it is not possible to monitor all data accesses of ADDR[n+1] with one comparator.

To detect an access of ADDR[n+1] through a word access of ADDR[n] the comparator can be configured to ADDR[n], DBGxDL is loaded with the data pattern and DBGxDHM is cleared so only the data[n+1] is compared on accesses of ADDR[n].

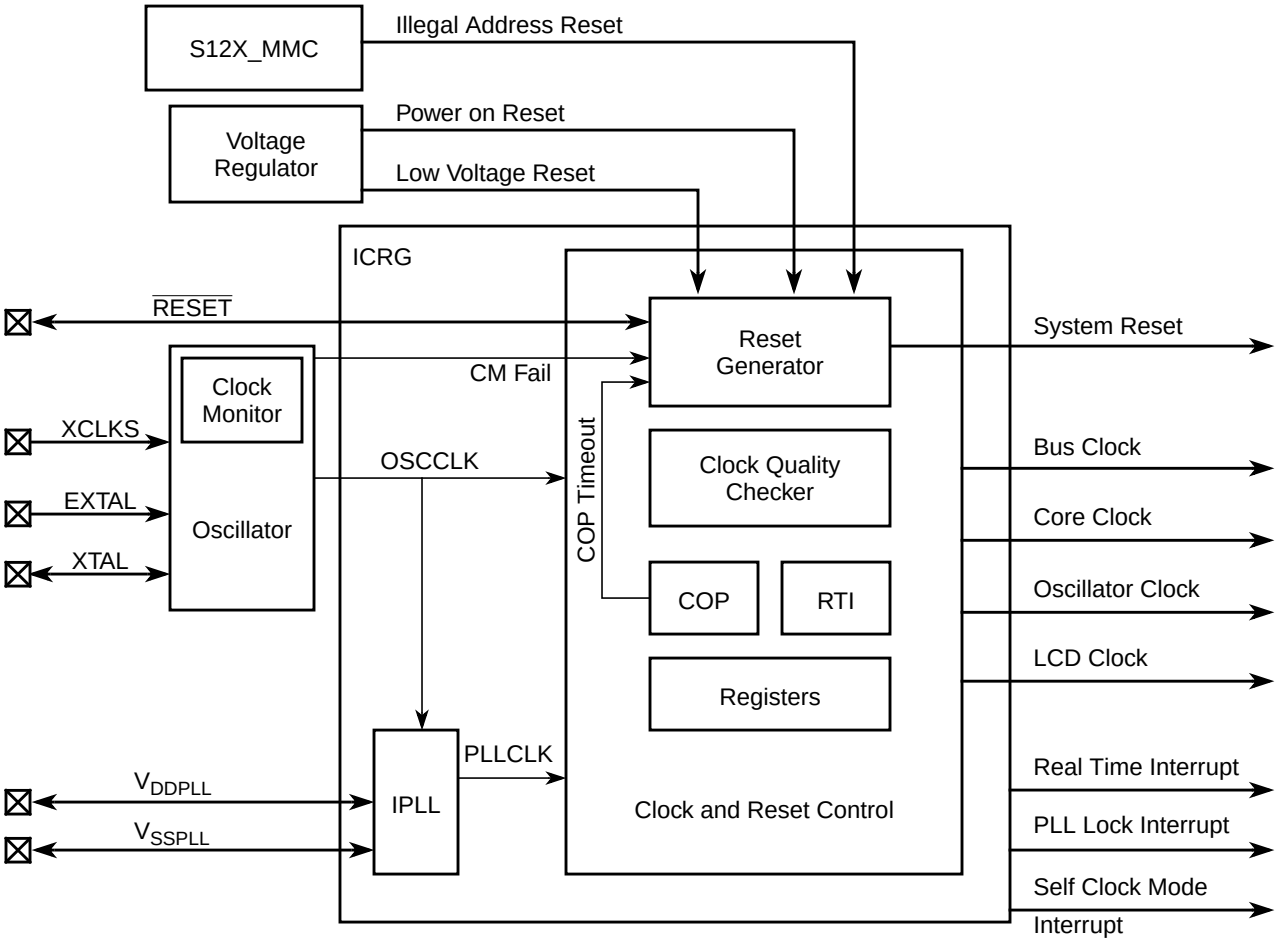


Figure 7-1. Block diagram of S12XECRG

7.2 Signal Description

This section lists and describes the signals that connect off chip.

7.2.1 V_{DDPLL}, V_{SSPLL}

These pins provides operating voltage (V_{DDPLL}) and ground (V_{SSPLL}) for the IPLL circuitry. This allows the supply voltage to the IPLL to be independently bypassed. Even if IPLL usage is not required V_{DDPLL} and V_{SSPLL} must be connected to properly.

7.2.2 $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is an active low bidirectional reset pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that an system reset (internal to MCU) has been triggered.

from the EXTAL input frequency. In full stop mode (PSTP = 0), the EXTAL pin is pulled down by an internal resistor of typical 200 kΩ.

NOTE

Freescale recommends an evaluation of the application board and chosen resonator or crystal by the resonator or crystal supplier.

Loop controlled circuit is not suited for overtone resonators and crystals.

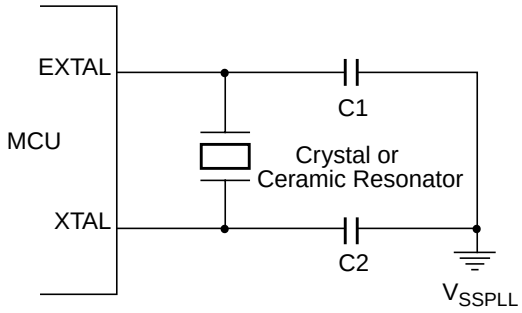
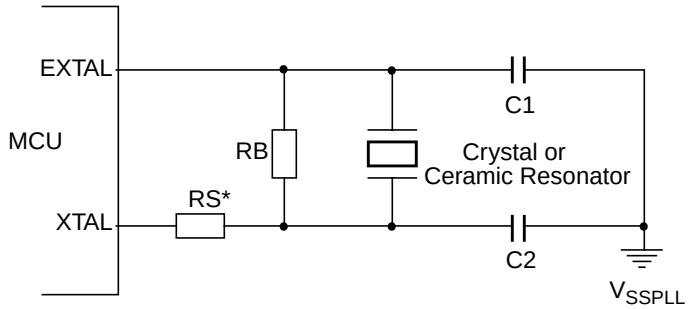


Figure 8-2. Loop Controlled Pierce Oscillator Connections (LCP mode selected)

NOTE

Full swing Pierce circuit is not suited for overtone resonators and crystals without a careful component selection.



* R_S can be zero (shorted) when use with higher frequency crystals. Refer to manufacturer's data.

Figure 8-3. Full Swing Pierce Oscillator Connections (FSP mode selected)

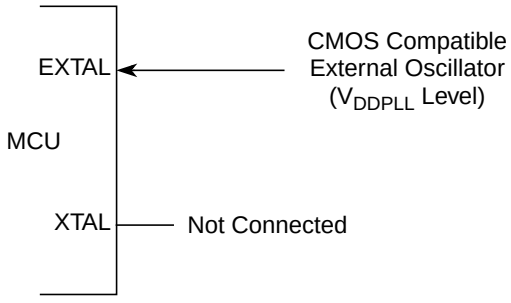


Figure 8-4. External Clock Connections (FSP mode selected)

Table 11-3. CANCTL0 Register Field Descriptions (continued)

Field	Description
1 SLPRQ[5]	**Sleep Mode Request** — This bit requests the MSCAN to enter sleep mode, which is an internal power saving mode (see Section 11.4.5.5, "MSCAN Sleep Mode"). The sleep mode request is serviced when the CAN bus is idle, i.e., the module is not receiving a message and all transmit buffers are empty. The module indicates entry to sleep mode by setting SLPAK = 1 (see Section 11.3.2.2, "MSCAN Control Register 1 (CANCTL1)"). SLPRQ cannot be set while the WUPIF flag is set (see Section 11.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)"). Sleep mode will be active until SLPRQ is cleared by the CPU or, depending on the setting of WUPE, the MSCAN detects activity on the CAN bus and clears SLPRQ itself. 0 Running — The MSCAN functions normally 1 Sleep mode request — The MSCAN enters sleep mode when CAN bus idle
0 INITRQ[6],[7]	**Initialization Mode Request** — When this bit is set by the CPU, the MSCAN skips to initialization mode (see Section 11.4.4.5, "MSCAN Initialization Mode"). Any ongoing transmission or reception is aborted and synchronization to the CAN bus is lost. The module indicates entry to initialization mode by setting INITAK = 1 (Section 11.3.2.2, "MSCAN Control Register 1 (CANCTL1)"). The following registers enter their hard reset state and restore their default values: CANCTL0[8], CANRFLG[9], CANRIER[10], CANTFLG, CANTIER, CANTARQ, CANTAAK, and CANTBSEL. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0-7, and CANIDMR0-7 can only be written by the CPU when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1). The values of the error counters are not affected by initialization mode. When this bit is cleared by the CPU, the MSCAN restarts and then tries to synchronize to the CAN bus. If the MSCAN is not in bus-off state, it synchronizes after 11 consecutive recessive bits on the CAN bus; if the MSCAN is in bus-off state, it continues to wait for 128 occurrences of 11 consecutive recessive bits. Writing to other bits in CANCTL0, CANRFLG, CANRIER, CANTFLG, or CANTIER must be done only after initialization mode is exited, which is INITRQ = 0 and INITAK = 0. 0 Normal operation 1 MSCAN in initialization mode

1. The MSCAN must be in normal mode for this bit to become set.
2. See the Bosch CAN 2.0A/B specification for a detailed definition of transmitter and receiver states.
3. In order to protect from accidentally violating the CAN protocol, TXCAN is immediately forced to a recessive state when the CPU enters wait (CSWAI = 1) or stop mode (see Section 11.4.5.2, "Operation in Wait Mode" and Section 11.4.5.3, "Operation in Stop Mode")**.**
4. The CPU has to make sure that the WUPE register and the WUPIE wake-up interrupt enable register (see Section 11.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)) is enabled, if the recovery mechanism from stop or wait is required.
5. The CPU cannot clear SLPRQ before the MSCAN has entered sleep mode (SLPRQ = 1 and SLPAK = 1).
6. The CPU cannot clear INITRQ before the MSCAN has entered initialization mode (INITRQ = 1 and INITAK = 1).
7. In order to protect from accidentally violating the CAN protocol, TXCAN is immediately forced to a recessive state when the initialization mode is requested by the CPU. Thus, the recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPAK = 1) before requesting initialization mode.
8. Not including WUPE, INITRQ, and SLPRQ.
9. TSTAT1 and TSTAT0 are not affected by initialization mode.
10. RSTAT1 and RSTAT0 are not affected by initialization mode.

11.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

For microcontrollers without a clock and reset generator (CRG), CANCLK is driven from the crystal oscillator (oscillator clock).

A programmable prescaler generates the time quanta (Tq) clock from CANCLK. A time quantum is the atomic unit of time handled by the MSCAN.

Eqn. 11-2

$$Tq = \frac{f_{CANCLK}}{(\text{Prescaler value})}$$

A bit time is subdivided into three segments as described in the Bosch CAN 2.0A/B specification. (see Figure 11-44):

- SYNC_SEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time Segment 1: This segment includes the PROP_SEG and the PHASE_SEG1 of the CAN standard. It can be programmed by setting the parameter TSEG1 to consist of 4 to 16 time quanta.
- Time Segment 2: This segment represents the PHASE_SEG2 of the CAN standard. It can be programmed by setting the TSEG2 parameter to be 2 to 8 time quanta long.

Eqn. 11-3

$$\text{Bit Rate} = \frac{f_{Tq}}{(\text{number of Time Quanta})}$$

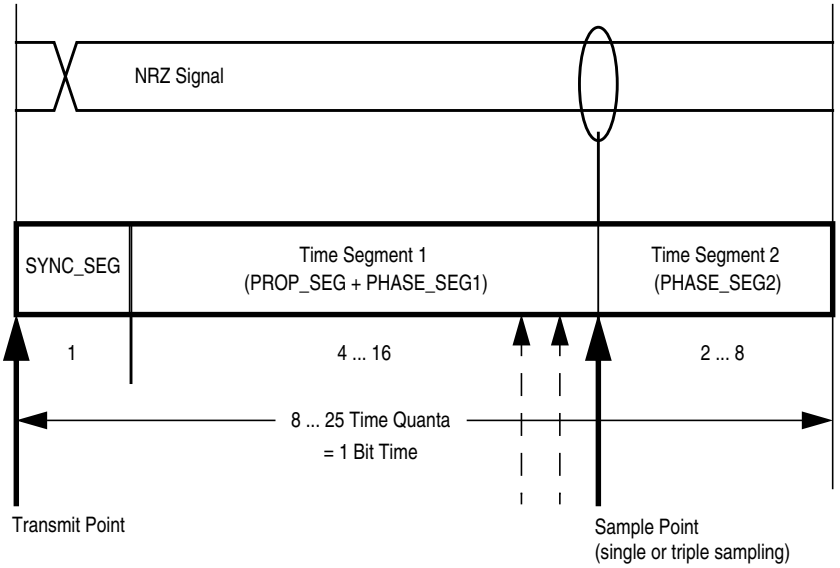


Figure 11-44. Segments within the Bit Time

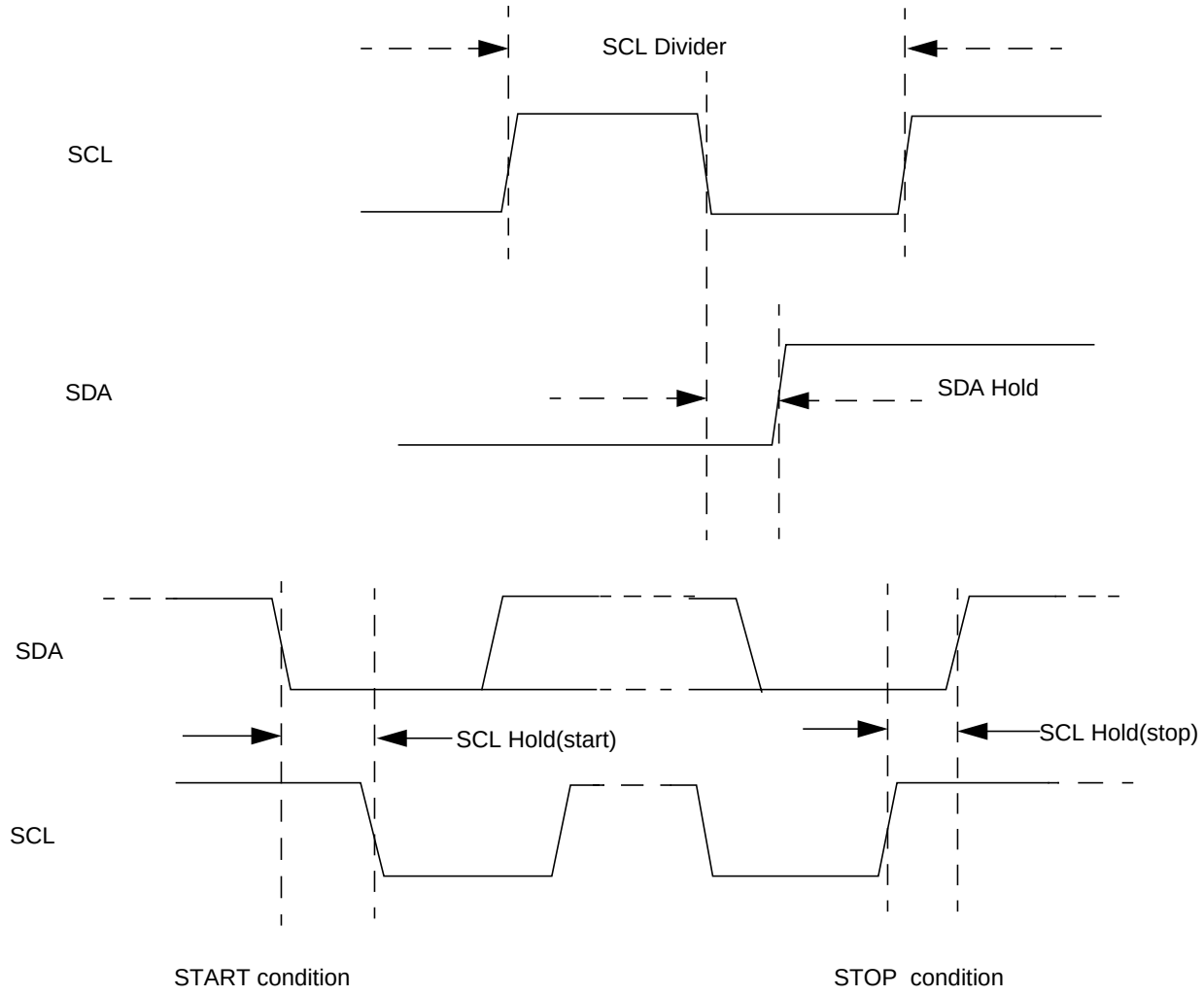


Figure 12-5. SCL Divider and SDA Hold

The equation used to generate the divider values from the IBFD bits is:

SCL Divider = MUL x {2 x (scl2tap + [(SCL_Tap -1) x tap2tap] + 2)}

The SDA hold delay is equal to the CPU clock period multiplied by the SDA Hold value shown in Table 12-7. The equation used to generate the SDA Hold value from the IBFD bits is:

SDA Hold = MUL x {scl2tap + [(SDA_Tap - 1) x tap2tap] + 3}

The equation for SCL Hold values to generate the start and stop conditions from the IBFD bits is:

SCL Hold(start) = MUL x [scl2start + (SCL_Tap - 1) x tap2tap]

SCL Hold(stop) = MUL x [scl2stop + (SCL_Tap - 1) x tap2tap]

Table 12-7. IIC Divider and Hold Values (Sheet 1 of 6)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
MUL=1				

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

14.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

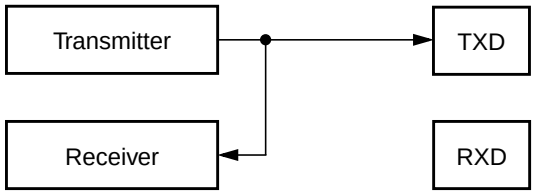


Figure 14-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

14.5 Initialization/Application Information

14.5.1 Reset Initialization

See Section 14.3.2, “Register Descriptions”.

14.5.2 Modes of Operation

14.5.2.1 Run Mode

Normal mode of operation.

To initialize a SCI transmission, see Section 14.4.5.2, “Character Transmission”.

Table 16-19. Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

NOTE

If the timer is not active (TEN = 0 in TSCR), there is no divide-by-64 because the ÷64 clock is generated by the timer prescaler.

Table 16-20. Timer Clock Selection

CLK1	CLK0	Timer Clock
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer Figure 16-30**.**

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

16.3.2.16 Pulse Accumulator Flag Register (PAFLG)

Module Base + 0x0021

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 16-25. Pulse Accumulator Flag Register (PAFLG)

Read: Anytime

Write: Anytime

When the TFFCA bit in the TSCR register is set, any access to the PACNT register will clear all the flags in the PAFLG register. Timer module or Pulse Accumulator must stay enabled (TEN=1 or PAEN=1) while clearing these bits.

Table 17-8. LCD Clock and Frame Frequency

Source clock Frequency in MHz	LCD Clock Prescaler			Divider	LCD Clock Frequency [Hz]	Frame Frequency [Hz]			
	LCLK2	LCLK1	LCLK0			1/1 Duty	1/2 Duty	1/3 Duty	1/4 Duty
IRCCLK = 16.0	1	1	0	65536	244	244	122	81	61
	1	1	1	131072	122	122	61	40	31

For other combinations of IRCCLK and divider not shown in Table 17-8, the following formula may be used to calculate the LCD frame frequency for each multiplex mode:

$$\text{LCD Frame Frequency (Hz)} = \left[\frac{(\text{IRCCLK (Hz)})}{\text{Divider}}\right] \cdot \text{Duty}$$

The possible divider values are shown in Table 17-8.

17.4.1.3 LCD RAM

For a segment on the LCD to be displayed, data must be written to the LCD RAM which is shown in Section 17.3, “Memory Map and Register Definition”. The 160 bits in the LCD RAM correspond to the 160 segments that are driven by the frontplane and backplane drivers. Writing a 1 to a given location will result in the corresponding display segment being driven with a differential RMS voltage necessary to turn the segment ON when the LCDEN bit is set and the corresponding FP[39:0]EN bit is set. Writing a 0 to a given location will result in the corresponding display segment being driven with a differential RMS voltage necessary to turn the segment OFF. The LCD RAM is a dual port RAM that interfaces with the internal address and data buses of the MCU. It is possible to read from LCD RAM locations for scrolling purposes. When LCDEN = 0, the LCD RAM can be used as on-chip RAM. Writing or reading of the LCDEN bit does not change the contents of the LCD RAM. After a reset, the LCD RAM contents will be indeterminate.

17.4.1.4 LCD Driver System Enable and Frontplane Enable Sequencing

If LCDEN = 0 (LCD40F4BV2 driver system disabled) and the frontplane enable bit, FP[39:0]EN, is set, the frontplane driver waveform will not appear on the output until LCDEN is set. If LCDEN = 1 (LCD40F4BV2 driver system enabled), the frontplane driver waveform will appear on the output as soon as the corresponding frontplane enable bit, FP[39:0]EN, in the registers FPENR0–FPENR4 is set.

17.4.1.5 LCD Bias and Modes of Operation

The LCD40F4BV2 driver has five modes of operation:

- 1/1 duty (1 backplane), 1/1 bias (2 voltage levels)
- 1/2 duty (2 backplanes), 1/2 bias (3 voltage levels)
- 1/2 duty (2 backplanes), 1/3 bias (4 voltage levels)
- 1/3 duty (3 backplanes), 1/3 bias (4 voltage levels)
- 1/4 duty (4 backplanes), 1/3 bias (4 voltage levels)

Table 18-46. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 18-26)
		Set if an invalid global address [22:16] is supplied
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.2.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and D-Flash memory space and, if the erase is successful, will release security.

Table 18-47. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and D-Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 18-48. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 18-26)
	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.2.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 18-7). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see

20.1.2.1.2 Dither Function

Dither function can be selected or deselected by setting or clearing the DITH bit. This bit influences all PWM channels. For details, please refer to Section 20.4.1.3.5, “Dither Bit (DITH)”.

20.1.2.2 PWM Channel Configuration Modes

The eight PWM channels can operate in three functional modes. Those modes are, with some restrictions, selectable for each channel independently.

20.1.2.2.1 Dual Full H-Bridge Mode

This mode is suitable to drive a stepper motor or a 360^{o} air gauge instrument. For details, please refer to Section 20.4.1.1.1, “Dual Full H-Bridge Mode (MCOM = 11)”. In this mode two adjacent PWM channels are combined, and two PWM channels drive four pins.

20.1.2.2.2 Full H-Bridge Mode

This mode is suitable to drive any load requiring a PWM signal in a H-bridge configuration using two pins. For details please refer to Section 20.4.1.1.2, “Full H-Bridge Mode (MCOM = 10)”.

20.1.2.2.3 Half H-Bridge Mode

This mode is suitable to drive a 90^{o} instrument driven by one pin. For details, please refer to Section 20.4.1.1.3, “Half H-Bridge Mode (MCOM = 00 or 01)”.

20.1.2.3 PWM Alignment Modes

Each PWM channel can operate independently in three different alignment modes. For details, please refer to Section 20.4.1.3.1, “PWM Alignment Modes”.

20.1.2.4 Low-Power Modes

The behavior of the motor controller in low-power modes is programmable. For details, please refer to Section 20.4.5, “Operation in Wait Mode” and Section 20.4.6, “Operation in Stop and Pseudo-Stop Modes”.

Table 20-4. Prescaler Values

MCPRE[1:0]	f_{TC}
00	f_{Bus}
01	$f_{Bus}/2$
10	$f_{Bus}/4$
11	$f_{Bus}/8$

20.3.2.2 Motor Controller Control Register 1

This register controls the behavior of the analog section of the motor controller as well as the interrupt enables.

Offset Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	RECIRC	0	0	0	0	0	0	MCTOIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-4. Motor Controller Control Register 1 (MCCTL1)

Table 20-5. MCCTL1 Field Descriptions

Field	Description
7 RECIRC	**Recirculation in (Dual) Full H-Bridge Mode** (refer to Section 20.4.1.3.3, “RECIRC Bit”)— RECIRC only affects the outputs in (dual) full H-bridge modes. In half H-bridge mode, the PWM output is always active low. RECIRC = 1 will also invert the effect of the S bits (refer to Section 20.4.1.3.2, “Sign Bit (S)”) in (dual) full H-bridge modes. RECIRC must be changed only while no PWM channel is operating in (dual) full H-bridge mode; otherwise, erroneous output pattern may occur. 0 Recirculation on the high side transistors. Active state for PWM output is logic low, the static channel will output logic high. 1 Recirculation on the low side transistors. Active state for PWM output is logic high, the static channel will output logic low.
0 MCTOIE	**Motor Controller Timer Counter Overflow Interrupt Enable** 0 Interrupt disabled. 1 Interrupt enabled. An interrupt will be generated when the motor controller timer counter overflow interrupt flag (MCTOIF) is set.

20.4.1.3.4 Relationship Between RECIRC Bit, S Bit, MCOM Bits, PWM State, and Output Transistors

Please refer to Figure 20-16 for the output transistor assignment.

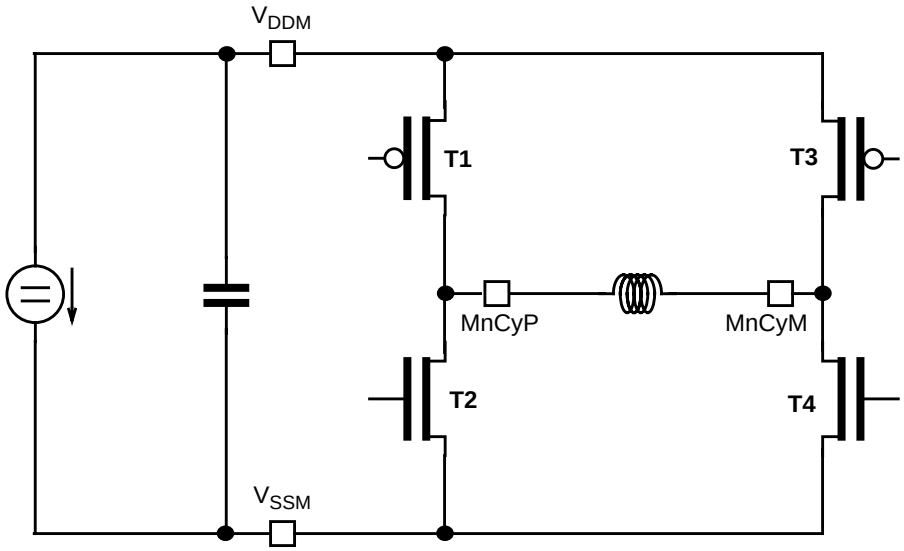


Figure 20-16. Output Transistor Assignment

Table 20-13 illustrates the state of the output transistors in different states of the PWM motor controller module. '—' means that the state of the output transistor is not controlled by the motor controller.

Table 20-13. State of Output Transistors in Various Modes

Mode	MCOM[1:0]	PWM Duty	RECIRC	S	T1	T2	T3	T4
Off	Don't care	—	Don't care	Don't care	—	—	—	—
Half H-Bridge	00	Active	Don't care	Don't care	—	—	OFF	ON
Half H-Bridge	00	Passive	Don't care	Don't care	—	—	ON	OFF
Half H-Bridge	01	Active	Don't care	Don't care	OFF	ON	—	—
Half H-Bridge	01	Passive	Don't care	Don't care	ON	OFF	—	—
(Dual) Full	10 or 11	Active	0	0	ON	OFF	OFF	ON
(Dual) Full	10 or 11	Passive	0	0	ON	OFF	ON	OFF
(Dual) Full	10 or 11	Active	0	1	OFF	ON	ON	OFF
(Dual) Full	10 or 11	Passive	0	1	ON	OFF	ON	OFF
(Dual) Full	10 or 11	Active	1	0	ON	OFF	OFF	ON
(Dual) Full	10 or 11	Passive	1	0	OFF	ON	OFF	ON
(Dual) Full	10 or 11	Active	1	1	OFF	ON	ON	OFF
(Dual) Full	10 or 11	Passive	1	1	OFF	ON	OFF	ON

C.1.1 112-Pin LQFP Recommended PCB Layout

Figure C-1. 112-Pin LQFP Recommended PCB Layout (Loop Controlled Pierce Oscillator)

0x00130–0x013F Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0130-0x013F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0140–0x017F MSCAN (CAN0) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	CAN0CTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0141	CAN0CTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		W								
0x0142	CAN0BTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0143	CAN0BTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0144	CAN0RFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x0145	CAN0RIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x0146	CAN0TFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x0147	CAN0TIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								
0x0148	CAN0TARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		W								
0x0149	CAN0TAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		W								
0x014A	CAN0TBSEL	R	0	0	0	0	0	TX2	TX1	TX0
		W								
0x014B	CAN0IDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		W								
0x014C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x014D	CAN0MISC	R	0	0	0	0	0	0	0	BOHOLD
		W								
0x014E	CAN0RXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		W								
0x014F	CAN0TXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		W								
0x0150-0x0153	CAN0IDAR0-CAN0IDAR3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0154-0x0157	CAN0IDMR0-CAN0IDMR3	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0158-0x015B	CAN0IDAR4-CAN0IDAR7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								