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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	76
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xhy256f0vll

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1.11.3.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

1.11.3.3 I/O Pins

Refer to the PIM section for reset configurations of all peripheral module ports.

1.11.3.4 Memory

The RAM arrays are not initialized out of reset.

1.12 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the COPCTL registerare loaded from the Flash register FOPT. See Table 1-12 and Table 1-13 for coding. The FOPT register is loaded from the Flash configuration field byte at global address 0x7_FF0E during the reset sequence.

If the MCU is secured the COP time-out rate is always set to the longest period (CR[2:0] = 111) after any reset into Special Single Chip mode.{mcu_9s12xhy256_cop_resetval.s}

Table 1-12. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in COPCTL Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-13. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.13 ATD External Trigger Input Connection

Table 2-2. Block Memory Map (continued)

Port	Offset or Address	Register	Access	Reset Value	Section/Page
Key Wak eup	0x0288	PIET—Port T Interrupt Enable Register	R/W	0x00	2.3.73/2-133
	0x0289	PIFT—Port T Interrupt Flag Register	R/W	0x00	2.3.74/2-134
	0x028A	PIES—Port S Interrupt Enable Register	R/W	0x00	2.3.75/2-134
	0x028B	PIFS—Port S Interrupt Flag Register	R/W	0x00	2.3.76/2-135
	0x028C	PIE1AD—Port AD Interrupt Enable Register	R/W	0x00	2.3.77/2-135
	0x028D	PIF1AD—Port AD Interrupt Flag Register	R/W	0x00	2.3.78/2-136
	0x028E	PIER—Port R Interrupt Enable Register	R/W	0x00	2.3.79/2-136
	0x028F	PIFR—Port R Interrupt Flag Register	R/W	0x00	2.3.80/2-137
U	0x0290	PTU—Port U Data Register	R/W	0x00	2.3.81/2-137
	0x0291	PTIU—Port U input Register	R	[3]	2.3.82/2-138
	0x0292	DDRU—Port U Data Direction Register	R/W	0x00	2.3.83/2-139
	0x0293	PIM Reserved	R	0x00	2.3.84/2-139
	0x0294	PERU—Port U Pull Device Enable Register	R/W	0x00	2.3.85/2-140
	0x0295	PPSU—Port U Polarity Select Register	R/W	0x00	2.3.86/2-140
	0x0296	SRRU—Port U Slew Rate Register	R/W	0x00	2.3.87/2-141
	0x0297	PTURR— Port S Routing Register PIM Reserved	R	0x00	2.3.88/2-141
V	0x0298	PTV—Port V Data Register	R/W	0x00	2.3.89/2-143
	0x0299	PTIV—Port V Input Register	R	[3]	2.3.90/2-145
	0x029A	DDRV—Port V Data Direction Register	R/W	0x00	2.3.91/2-146
	0x029B	PIM Reserved	R	0x00	2.3.92/2-148
	0x029C	PERV—Port V Pull Device Enable Register	R/W	0x00	2.3.93/2-148
	0x029D	PPSV—Port V Polarity Select Register	R/W	0x00	2.3.94/2-148
	0x029E	SRRV—Port V Slew Rate Register	R/W	0x00	2.3.95/2-149
	0x029F	PTVRR— Port S Routing Register	R	0x00	2.3.96/2-150

[1] Refer to memory map in SoC Guide to determine related module

[2] Write access not applicable for one or more register bits. Refer to register description

[3] Read always returns logic level on pins.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PORTA	R W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

= Unimplemented or Reserved

2.3.89 Port V Data Register (PTV)

Address 0x0298 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
	—	—	—	—	$\overline{SS}$	—	—	MISO[2]
	—	—	—	—	PWM7	PWM6	PWM5	PWM4
	—	—	—	—	SDA	SCK	MOSI	SCL
	—	IOC1_3	—	IOC1_2	—	IOC1_1	—	IOC1_0
		IOC0_7		IOC0_6		IOC0_5		IOC0_4
Altern. Function	M3C1P	M3C1M	M3C0P	M3C0M	M2C1P	M2C1M	M2C0P	M2C0M
	M3SINP	M3SINM	M3COSP	M3COSM	M2SINP	M2SINM	M2COSP	M2COSM
Reset	0	0	0	0	0	0	0	0

Figure 2-86. Port V Data Register (PTV)

[1] Read: Anytime.
Write: Anytime

[2] Special SPI/PWM&IIC priority

Table 2-73. PTV register Field Descriptions

Field	Description
7,5 PTV	**Port V general purpose input/output data**—Data Register, Motor driver PWM output Port V pins are associated with the Motor PWM output. When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The SSD takes precedence over the Motor Driver and general purpose I/O function • The Motor driver PWM takes precedence over the general purpose I/O function.
6, 4 PTV	**Port V general purpose input/output data**—Data Register, Motor driver PWM output, TIM1 channel 3,2 Port V pins are associated with the Motor PWM output and TIM1 channels 3-2 When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The SSD takes precedence over the Motor Driver and TIM0,TIM1 and general purpose I/O function • The Motor driver PWM takes precedence over the TIM0, TIM1 and the general purpose I/O function. • The TIM0 output compare function takes precedence over the TIM1 and the general purpose I/O function. • The TIM1 output compare function takes precedence over the general purpose I/O function if the related channels is enabled[1]

The two fixed 4KB pages (0xFE, 0xFF) contain unimplemented area in the range not occupied by RAM if RAMSIZE is less than 8KB (Refer to Section 3.4.2.3, “Implemented Memory Map).

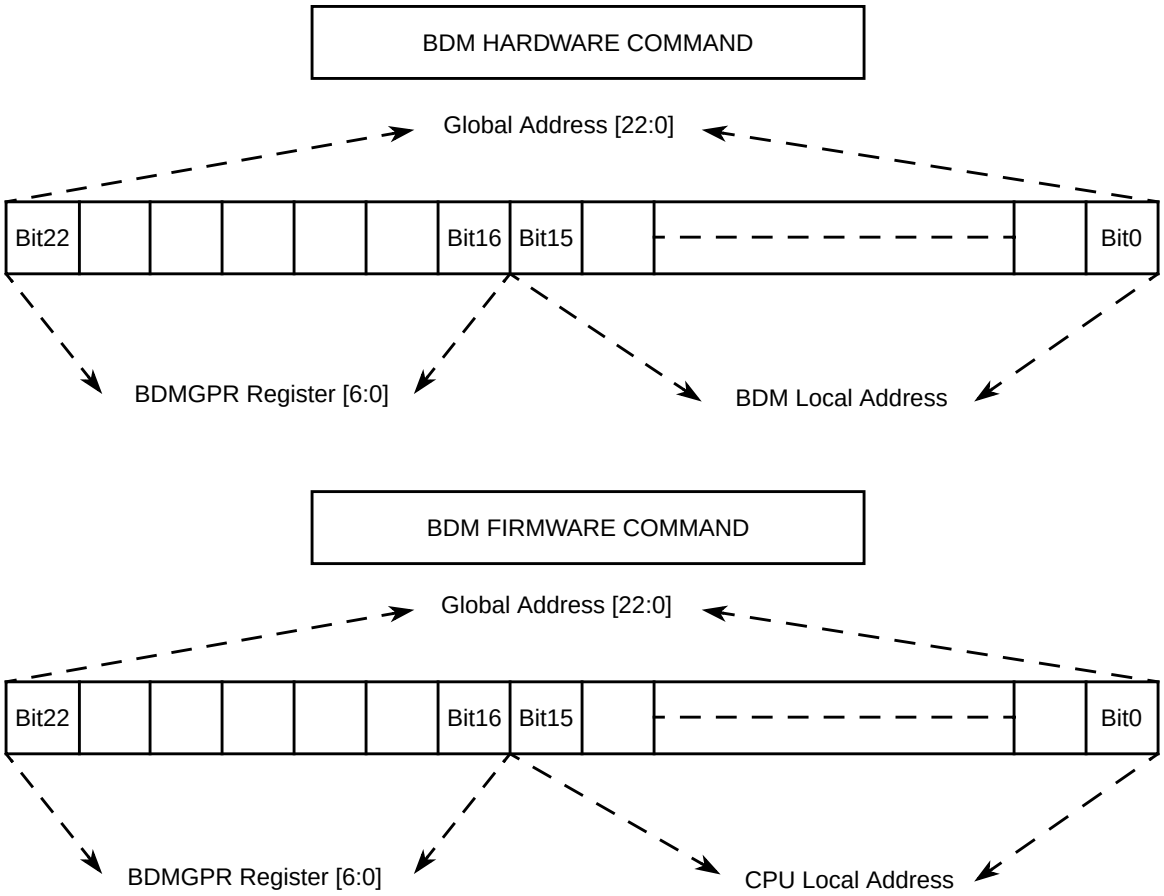


Figure 3-18. BDMGPR Address Mapping

3.4.2.3 Implemented Memory Map

The global memory spaces reserved for the internal resources (RAM, Data FLASH, and FLASH) are not determined by the MMC module. Size of the individual internal resources are however fixed in the design of the device cannot be changed by the user. Please refer to the SoC Guide for further details. Figure 3-19 and Table 3-10 show the memory spaces occupied by the on-chip resources. Please note that the memory spaces have fixed top addresses.

Table 3-10. Global Implemented Memory Space

Internal Resource	$Address
RAM	RAM_LOW = 0x10_0000 minus RAMSIZE[1]
Data FLASH	DF_HIGH = 0x10_0000 plus DFLASHSIZE[2]
FLASH	FLASH_LOW = 0x80_0000 minus FLASHSIZE[3]

1 RAMSIZE is the hexadecimal value of RAM SIZE in Bytes
2 DFLASHSIZE is the hexadecimal value of DFLASH SIZE in Bytes
3 FLASHSIZE is the hexadecimal value of FLASH SIZE in Bytes

9.3.2.6 Reserved 06

The Reserved 06 is reserved for test purposes.

0x02F6

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-7. Reserved 06

9.3.2.7 High Temperature Trimming Register (VREGHTTR)

The VREGHTTR register allows to trim the VREG temperature sense.

0x02F7

	7	6	5	4	3	2	1	0
R	HTOEN	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	0[1]	0[1]	0[1]	0[1]

1. Reset value is either 0 or preset by factory. See Section 1 (Device Overview) for details.

= Unimplemented or Reserved

Figure 9-8. VREGHTTR

Table 9-11. VREGHTTR field descriptions

Field	Description
7 HTOEN	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled 0 The temperature sense offset is disabled 1 The temperature sense offset is enabled
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 23-16 for trimming effects.

Table 9-12. Trimming Effect

Bit	Trimming Effect
HTTR[3]	Increases V_{HT} twice of HTTR[2]
HTTR[2]	Increases V_{HT} twice of HTTR[1]
HTTR[1]	Increases V_{HT} twice of HTTR[0]
HTTR[0]	Increases V_{HT} (to compensate Temperature Offset)

IIC Interrupt	—	—	—	IBAL, TCF, IAAS bits in IBSR register	When either of IBAL, TCF or IAAS bits is set may cause an interrupt based on arbitration lost, transfer complete or address detect conditions

Internally there are three types of interrupts in IIC. The interrupt service routine can determine the interrupt type by reading the status register.

IIC Interrupt can be generated on

1. Arbitration lost condition (IBAL bit set)
2. Byte transfer condition (TCF bit set)
3. Address detect condition (IAAS bit set)

The IIC interrupt is enabled by the IBIE bit in the IIC control register. It must be cleared by writing 0 to the IBF bit in the interrupt service routine.

12.7 Application Information

12.7.1 IIC Programming Examples

12.7.1.1 Initialization Sequence

Reset will put the IIC bus control register to its default status. Before the interface can be used to transfer serial data, an initialization procedure must be carried out, as follows:

1. Update the frequency divider register (IBFD) and select the required division ratio to obtain SCL frequency from system clock.
2. Update the ADTYPE of IBCR2 to define the address length, 7 bits or 10 bits.
3. Update the IIC bus address register (IBAD) to define its slave address. If 10-bit address is applied IBCR2 should be updated to define the rest bits of address.
4. Set the IBEN bit of the IIC bus control register (IBCR) to enable the IIC interface system.
5. Modify the bits of the IIC bus control register (IBCR) to select master/slave mode, transmit/receive mode and interrupt enable or not.
6. If supported general call, the GCEN in IBCR2 should be asserted.

12.7.1.2 Generation of START

After completion of the initialization procedure, serial data can be transmitted by selecting the 'master transmitter' mode. If the device is connected to a multi-master bus system, the state of the IIC bus busy bit (IBB) must be tested to check whether the serial bus is free.

If the bus is free (IBB=0), the start condition and the first byte (the slave address) can be sent. The data written to the data register comprises the slave calling address and the LSB set to indicate the direction of transfer required from the slave.

The bus free time (i.e., the time between a STOP condition and the following START condition) is built into the hardware that generates the START cycle. Depending on the relative frequencies of the system

Caution:When IIC is configured as 10-bit address,the point of the data array in interrupt routine must be reset after it’s addressed.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000B PWMSCNTB[1]	R	0	0	0	0	0	0	0	0
	W								
0x000C PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000D PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000E PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000F PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0010 PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0011 PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0012 PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0013 PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0014 PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0015 PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0016 PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0017 PWMPER3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0018 PWMPER4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0019 PWMPER5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								

= Unimplemented or Reserved

Figure 13-2. PWM Register Summary (Sheet 2 of 3)

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

14.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

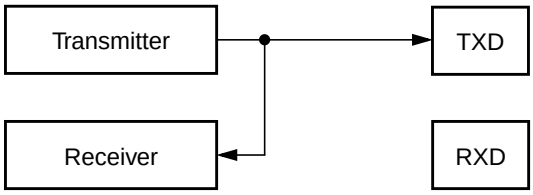


Figure 14-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

14.5 Initialization/Application Information

14.5.1 Reset Initialization

See Section 14.3.2, “Register Descriptions”.

14.5.2 Modes of Operation

14.5.2.1 Run Mode

Normal mode of operation.

To initialize a SCI transmission, see Section 14.4.5.2, “Character Transmission”.

15.4.3.1 Clock Phase and Polarity Controls

Using two bits in the SPI control register 1, software selects one of four combinations of serial clock phase and polarity.

The CPOL clock polarity control bit specifies an active high or low clock and has no significant effect on the transmission format.

The CPHA clock phase control bit selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

15.4.3.2 CPHA = 0 Transfer Format

The first edge on the SCK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. In some peripherals, the first bit of the slave's data is available at the slave's data out pin as soon as the slave is selected. In this format, the first SCK edge is issued a half cycle after $\overline{SS}$ has become low.

A half SCK cycle later, the second edge appears on the SCK line. When this second edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the shift register, depending on LSBFE bit.

After this second edge, the next bit of the SPI master data is transmitted out of the serial data output pin of the master to the serial input pin on the slave. This process continues for a total of 16 edges on the SCK line, with data being latched on odd numbered edges and shifted on even numbered edges.

Data reception is double buffered. Data is shifted serially into the SPI shift register during the transfer and is transferred to the parallel SPI data register after the last bit is shifted in.

After 2n[4] (last) SCK edges:

- Data that was previously in the master SPI data register should now be in the slave data register and the data that was in the slave data register should be in the master.
- The SPIF flag in the SPI status register is set, indicating that the transfer is complete.

Figure 15-12 is a timing diagram of an SPI transfer where CPHA = 0. SCK waveforms are shown for CPOL = 0 and CPOL = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave and the MOSI signal is the output from the master. The $\overline{SS}$ pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

4. n depends on the selected transfer width, please refer to Section 15.3.2.2, "SPI Control Register 2 (SPICR2)

Upon clearing CCIF to launch the Erase Verify All Blocks command, the Memory Controller will verify that the entire Flash memory space is erased. The CCIF flag will set after the Erase Verify All Blocks operation has completed.

Table 18-30. Erase Verify All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

18.4.2.2 Erase Verify Block Command

The Erase Verify Block command allows the user to verify that an entire P-Flash or D-Flash block has been erased. The FCCOB upper global address bits determine which block must be verified.

Table 18-31. Erase Verify Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x02	Global address [22:16] of the Flash block to be verified.

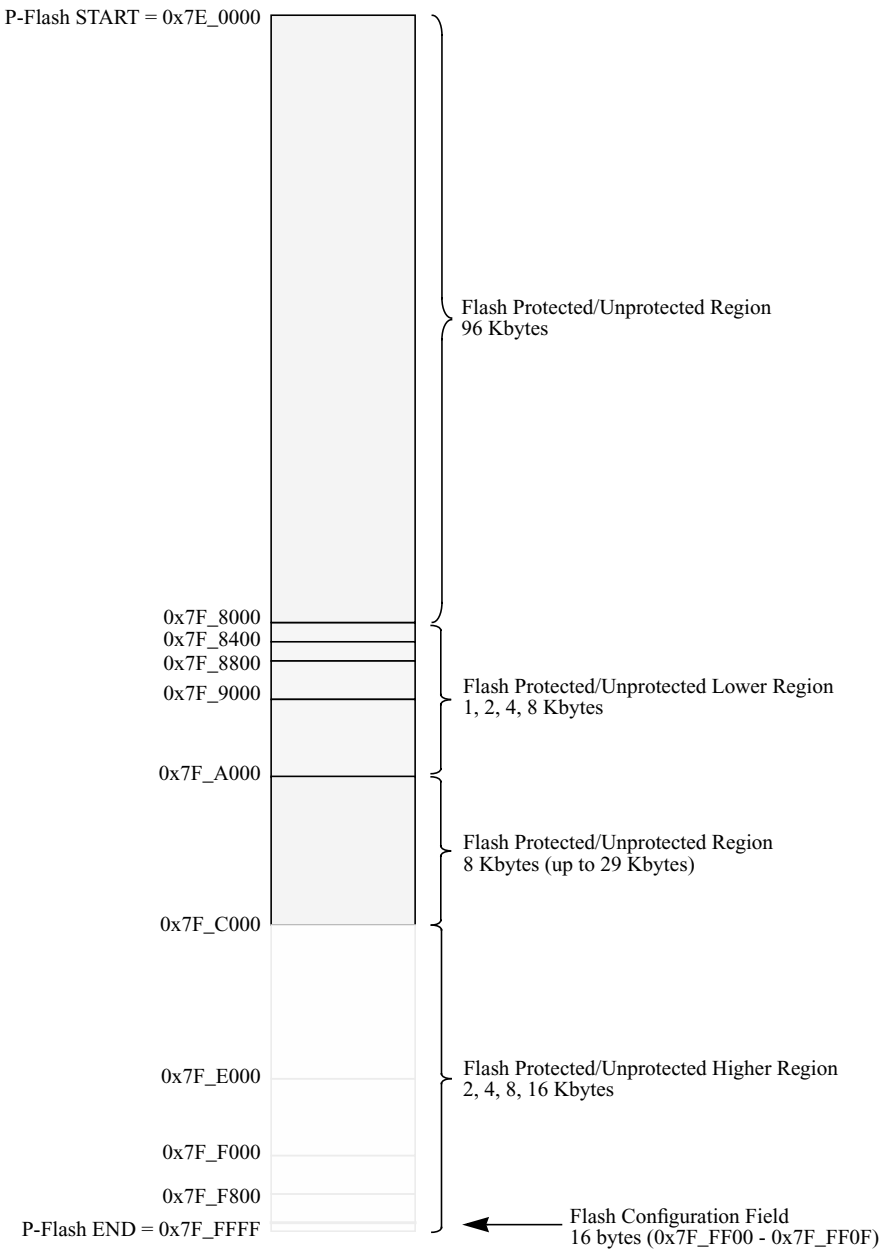
Upon clearing CCIF to launch the Erase Verify Block command, the Memory Controller will verify that the selected P-Flash or D-Flash block is erased. The CCIF flag will set after the Erase Verify Block operation has completed.

Table 18-32. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid global address [22:16] is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

18.4.2.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases. The section to be verified cannot cross a 256 Kbyte boundary in the P-Flash memory space.


P-Flash START = 0x7E_0000
Flash Protected/Unprotected Region
96 Kbytes
0x7F_8000
0x7F_8400
0x7F_8800
0x7F_9000
Flash Protected/Unprotected Lower Region
1, 2, 4, 8 Kbytes
0x7F_A000
Flash Protected/Unprotected Region
8 Kbytes (up to 29 Kbytes)
0x7F_C000
0x7F_E000
Flash Protected/Unprotected Higher Region
2, 4, 8, 16 Kbytes
0x7F_F000
0x7F_F800
P-Flash END = 0x7F_FFFF
Flash Configuration Field
16 bytes (0x7F_FF00 - 0x7F_FF0F)

19.3.1.3 Valid Flash Module Commands

Table 19-25. Flash Commands by Mode

FCMD	Command	Unsecured				Secured			
		NS[1]	NX[2]	SS[3]	ST[4]	NS[5]	NX[6]	SS[7]	ST[8]
0x01	Erase Verify All Blocks	*	*	*	*	*	*	*	*
0x02	Erase Verify Block	*	*	*	*	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	*	*			
0x04	Read Once	*	*	*	*	*			
0x06	Program P-Flash	*	*	*	*	*			
0x07	Program Once	*	*	*	*	*			
0x08	Erase All Blocks			*	*			*	*
0x09	Erase Flash Block	*	*	*	*	*			
0x0A	Erase P-Flash Sector	*	*	*	*	*			
0x0B	Unsecure Flash			*	*			*	*
0x0C	Verify Backdoor Access Key	*				*			
0x0D	Set User Margin Level	*	*	*	*	*			
0x0E	Set Field Margin Level			*	*				
0x10	Erase Verify D-Flash Section	*	*	*	*	*			
0x11	Program D-Flash	*	*	*	*	*			
0x12	Erase D-Flash Sector	*	*	*	*	*			

1 Unsecured Normal Single Chip mode.
2 Unsecured Normal Expanded mode.
3 Unsecured Special Single Chip mode.
4 Unsecured Special Mode.
5 Secured Normal Single Chip mode.
6 Secured Normal Expanded mode.
7 Secured Special Single Chip mode.
8 Secured Special Mode.

19.3.1.4 P-Flash Commands

Table 19-26 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

20.3.2.4 Motor Controller Channel Control Registers

Each PWM channel has one associated control register to control output delay, PWM alignment, and output mode. The registers are named MCCC0... MCCC7. In the following, MCCC0 is described as a reference for all eight registers.

Offset Module Base + 0x0010 . . . 0x0017

	7	6	5	4	3	2	1	0
R	MCOM1	MCOM0	MCAM1	MCAM0	0	0	CD1	CD0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-7. Motor Controller Control Register Channel 0–7 (MCCC0–MCCC7)

Table 20-6. MCCC0–MCCC7 Field Descriptions

Field	Description
7:6 MCOM[1:0]	**Output Mode** — MCOM1, MCOM0 control the PWM channel's output mode. See Table 20-7.
5:4 MCAM[1:0]	**PWM Channel Alignment Mode** — MCAM1, MCAM0 control the PWM channel's PWM alignment mode and operation. See Table 20-8. MCAM[1:0] and MCOM[1:0] are double buffered. The values used for the generation of the output waveform will be copied to the working registers either at once (if all PWM channels are disabled or MCPER is set to 0) or if a timer counter overflow occurs. Reads of the register return the most recent written value, which are not necessarily the currently active values.
1:0 CD[1:0]	**PWM Channel Delay** — Each PWM channel can be individually delayed by a programmable number of PWM timer counter clocks. The delay will be n/f_{TC}. See Table 20-9.

Table 20-7. Output Mode

MCOM[1:0]	Output Mode
00	Half H-bridge mode, PWM on MnCxM, MnCxP is released
01	Half H-bridge mode, PWM on MnCxP, MnCxM is released
10	Full H-bridge mode
11	Dual full H-bridge mode

Table 20-8. PWM Alignment Mode

MCAM[1:0]	PWM Alignment Mode
00	Channel disabled
01	Left aligned
10	Right aligned
11	Center aligned

21.3.2.4 Stepper Stall Detector Flag Register (SSDFLG)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	MCZIF	0	0	0	0	0	0	AOVIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-5. Stepper Stall Detector Flag Register (SSDFLG)

Read: anytime

Write: anytime.

Table 21-10. SSDFLG Field Descriptions

Field	Description
7 MCZIF	**Modulus Counter Underflow Interrupt Flag** — This flag is set when the modulus down-counter reaches 0x0000. If not masked (MCZIE = 1), a modulus counter underflow interrupt is pending while this flag is set. This flag is cleared by writing a ‘1’ to the bit. A write of ‘0’ has no effect.
0 AOVIF	**Accumulator Overflow Interrupt Flag** — This flag is set when the Integration Accumulator has a positive or negative overflow. If not masked (AOVIE = 1), an accumulator overflow interrupt is pending while this flag is set. This flag is cleared by writing a ‘1’ to the bit. A write of ‘0’ has no effect.

21.3.2.5 Modulus Down-Counter Count Register (MDCCNT)

Module Base + 0x0004

	15	14	13	12	11	10	9	8
R	MDCCNT							
W								
Reset	1	1	1	1	1	1	1	1

Figure 21-6. Modulus Down-Counter Count Register High (MDCCNT)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	MDCCNT							
W								
Reset	1	1	1	1	1	1	1	1

Figure 21-7. Modulus Down-Counter Count Register Low (MDCCNT)

Read: anytime

Write: anytime.

C.1.2 100-Pin QFP Recommended PCB Layout

Figure C-2. 100-Pin QFP Recommended PCB Layout (Loop Controlled Pierce Oscillator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01F0–0x01FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0200-0x021F Liquid Crystal Display 40x4(LCD) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0200	LCDCR0	R	LCDEN	0	LCLK2	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
		W								
0x0201	LCDCR1	R	0	0	0	0	0	0	LCDSWAI	LCDRPSTP
		W								
0x0202	FPENR0	R	FP7EN	FP6EN	FP5EN	FP4EN	FP3EN	FP2EN	FP1EN	FP0EN
		W								
0x0203	FPENR1	R	FP15EN	FP14EN	FP13EN	FP12EN	FP11EN	FP10EN	FP9EN	FP8EN
		W								
0x0204	FPENR2	R	FP23EN	FP22EN	FP21EN	FP20EN	FP19EN	FP18EN	FP17EN	FP16EN
		W								
0x0205	FPENR3	R	FP31EN	FP30EN	FP29EN	FP28EN	FP27EN	FP26EN	FP25EN	FP24EN
		W								
0x0206	FPENR4	R	FP39EN	FP38EN	FP37EN	FP36EN	FP35EN	FP34EN	FP33EN	FP32EN
		W								
0x0207	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0208	LCDRAM0	R	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
		W								
0x0209	LCDRAM1	R	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
		W								
0x020A	LCDRAM2	R	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
		W								
0x020B	LCDRAM3	R	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
		W								
0x020C	LCDRAM4	R	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
		W								
0x020D	LCDRAM5	R	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
		W								
0x020E	LCDRAM6	R	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
		W								
0x020F	LCDRAM7	R	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0
		W								
0x0210	LCDRAM8	R	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
		W								