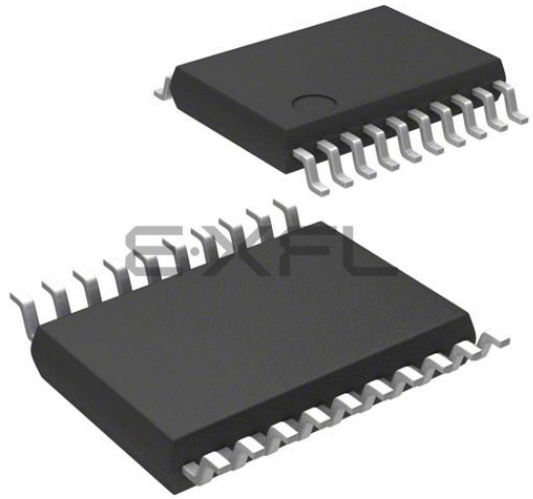

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	15
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f030f4p6

List of tables

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F030x4/x6/x8/xC microcontrollers.

This document should be read in conjunction with the STM32F0x0xx reference manual (RM0360). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = 2.4 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMA manages memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
22	16	12	12	PA6	I/O	TTa	-	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT USART3_CTS(5)	ADC_IN6
23	17	13	13	PA7	I/O	TTa	-	SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
24	-	-	-	PC4	I/O	TTa	-	EVENTOUT, USART3_TX(5)	ADC_IN14
25	-	-	-	PC5	I/O	TTa	-	USART3_RX(5)	ADC_IN15, WKPU5(5)
26	18	14	-	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, EVENTOUT, USART3_CK(5)	ADC_IN8
27	19	15	14	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, USART3_RTS(5)	ADC_IN9
28	20	-	-	PB2	I/O	FT	(6)	-	-
29	21	-	-	PB10	I/O	FT	-	SPI2_SCK(5), I2C1_SCL(2), I2C2_SCL(3)(5), USART3_TX(5)	-
30	22	-	-	PB11	I/O	FT	-	I2C1_SDA(2), I2C2_SDA(3)(5), EVENTOUT, USART3_RX(5)	-
31	23	16	-	VSS	S	-	-	Ground	
32	24	17	16	VDD	S	-	-	Digital power supply	
33	25	-	-	PB12	I/O	FT	-	SPI1_NSS(2), SPI2_NSS(3)(5), TIM1_BKIN, EVENTOUT, USART3_CK(5)	-

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
34	26	-	-	PB13	I/O	FT	-	SPI1_SCK(2), SPI2_SCK(3)(5), I2C2_SCL(5), TIM1_CH1N, USART3_CTS(5)	-
35	27	-	-	PB14	I/O	FT	-	SPI1_MISO(2), SPI2_MISO(3)(5), I2C2_SDA(5), TIM1_CH2N, TIM15_CH1(3)(5), USART3_RTS(5)	-
36	28	-	-	PB15	I/O	FT	-	SPI1_MOSI(2), SPI2_MOSI(3)(5), TIM1_CH3N, TIM15_CH1N(3)(5), TIM15_CH2(3)(5)	RTC_REFIN, WKPU7(5)
37	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	29	18	-	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	30	19	17	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN(3)(5) I2C1_SCL(2)(5)	-
43	31	20	18	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA(2)(5)	-
44	32	21	-	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL(5)	-
45	33	22	-	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA(5)	-

Table 12. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART1_CTS(2)	-	-	USART4_TX(1)	-	-
		USART2_CTS(1)(3)					
PA1	EVENTOUT	USART1_RTS(2)	-	-	USART4_RX(1)	TIM15_CH1N(1)	-
		USART2_RTS(1)(3)					
PA2	TIM15_CH1(1)(3)	USART1_TX(2)	-	-	-	-	-
		USART2_TX(1)(3)					
PA3	TIM15_CH2(1)(3)	USART1_RX(2)	-	-	-	-	-
		USART2_RX(1)(3)					
PA4	SPI1_NSS	USART1_CK(2)	-	-	TIM14_CH1	USART6_TX(1)	-
		USART2_CK(1)(3)					
PA5	SPI1_SCK	-	-	-	-	USART6_RX(1)	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	USART3_CTS(1)	TIM16_CH1	EVENTOUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-
PA9	TIM15_BKIN(1)(3)	USART1_TX	TIM1_CH2	-	I2C1_SCL(1)(2)	MCO(1)	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA(1)(2)	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	SCL	-

Table 17. STM32F030x4/x6/x8/xC peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
-	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 43FF	4 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
-	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15(1)
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 1800 - 0x4001 23FF	3 KB	Reserved
	0x4001 1400 - 0x4001 17FF	1 KB	USART6(2)
	0x4001 0800 - 0x4001 13FF	3 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

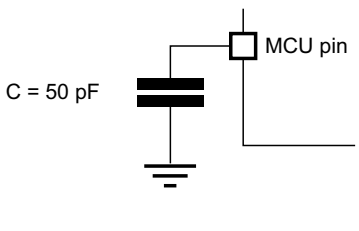
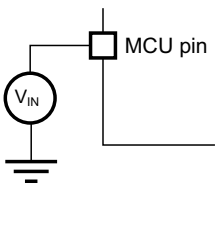


Figure 11. Pin input voltage



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress *ratings* only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	-0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	V
	BOOT0	0	V_{DDIOx} + 4.0 (3)	V
	Input voltage on any other pin	V_{SS} –0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. V_{DDIOx} is internally connected with VDD pin.

Table 21. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	Analog operating voltage	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3(2)	
		FT and FTf I/O	-0.3	5.5(2)	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 (1)	LQFP64	-	455	mW
		LQFP48	-	364	
		LQFP32	-	357	
		TSSOP20	-	263	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge(2)	1.80	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V

Table 27. Typical and maximum consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
				3.6 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		19	48	µA
		Regulator in low-power mode, all oscillators OFF		5	32	
	Supply current in Standby mode	LSI ON and IWDG ON		2	-	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run or low-power mode, all oscillators OFF	2.9	3.5	
	Supply current in Standby mode		LSI ON and IWDG ON	3.3	-	
			LSI OFF and IWDG OFF	2.8	3.5	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run or low-power mode, all oscillators OFF	1.7	-	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	-	
			LSI OFF and IWDG OFF	1.4	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 30. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	2.8	5	µs
$t_{WUSTANDBY}$	Wakeup from Standby mode	-	51	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4 SYSCLK cycles	-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 14: High-speed external clock source AC timing diagram*.

Table 31. High-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

1. Guaranteed by design, not tested in production.

Figure 14. High-speed external clock source AC timing diagram

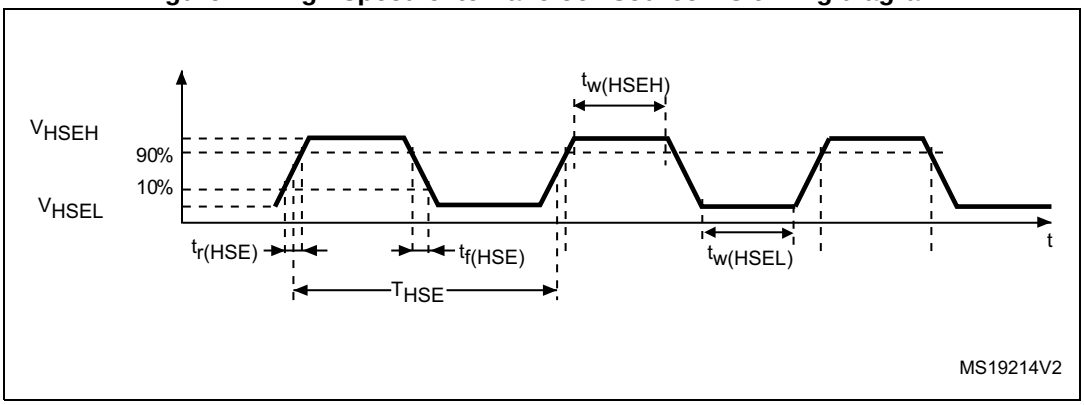


Table 33. HSE oscillator characteristics

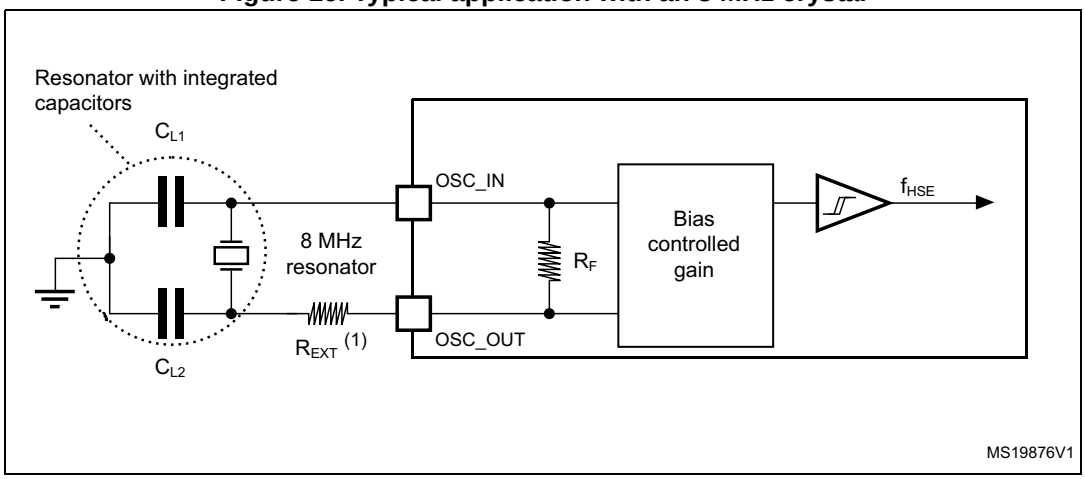
Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
I_{DD}	HSE current consumption	During startup[3]	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results

6.3.8 Internal clock source characteristics

The parameters given in *Table 35* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 35. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{HSI}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = -40 to 85°C	-	±5	-	%
		T_A = 25°C	-	±1(3)	-	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. With user calibration.

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 36. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 85 °C	-	±5	-	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 37. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C4(2) C3(3)	500(2) 250(3)	V

1. Data based on characterization results, not tested in production.
2. Applicable to STM32F030xC
3. Applicable to STM32F030x4, STM32F030x6, and STM32F030x8

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 45*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Figure 18. TC and TTa I/O input characteristics

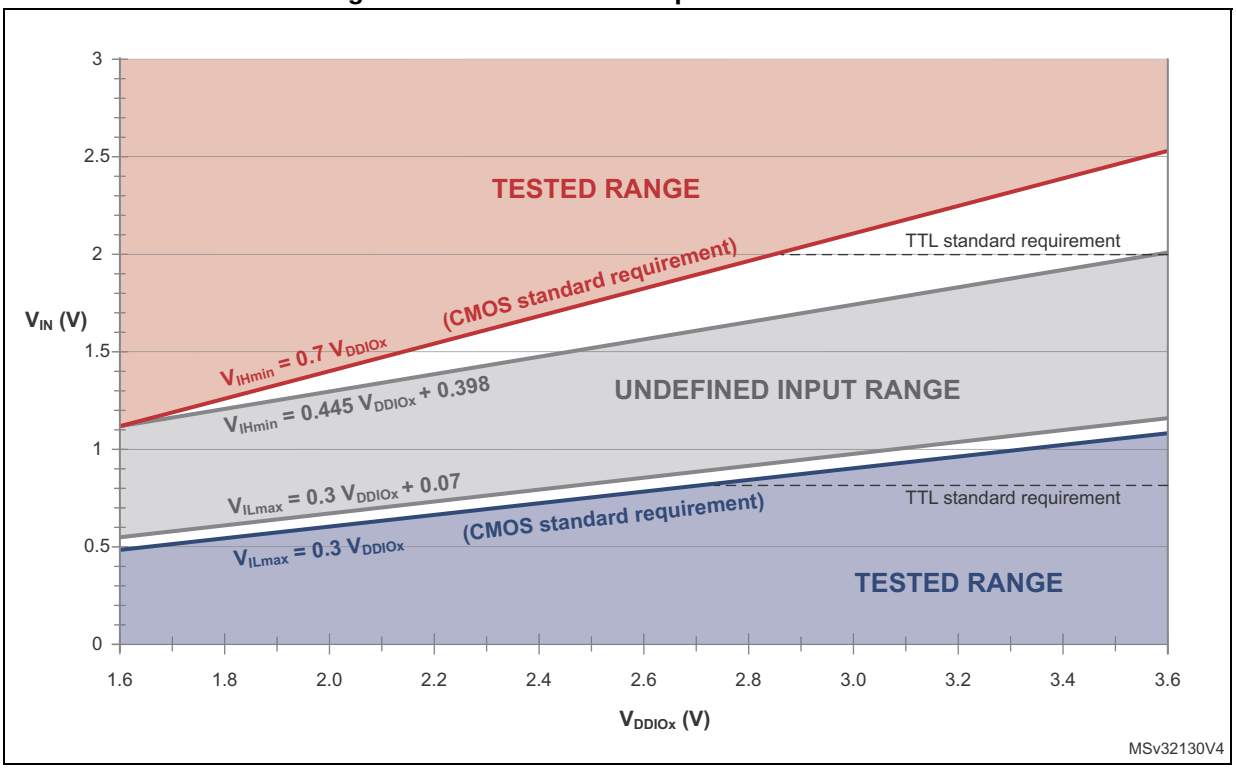


Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics

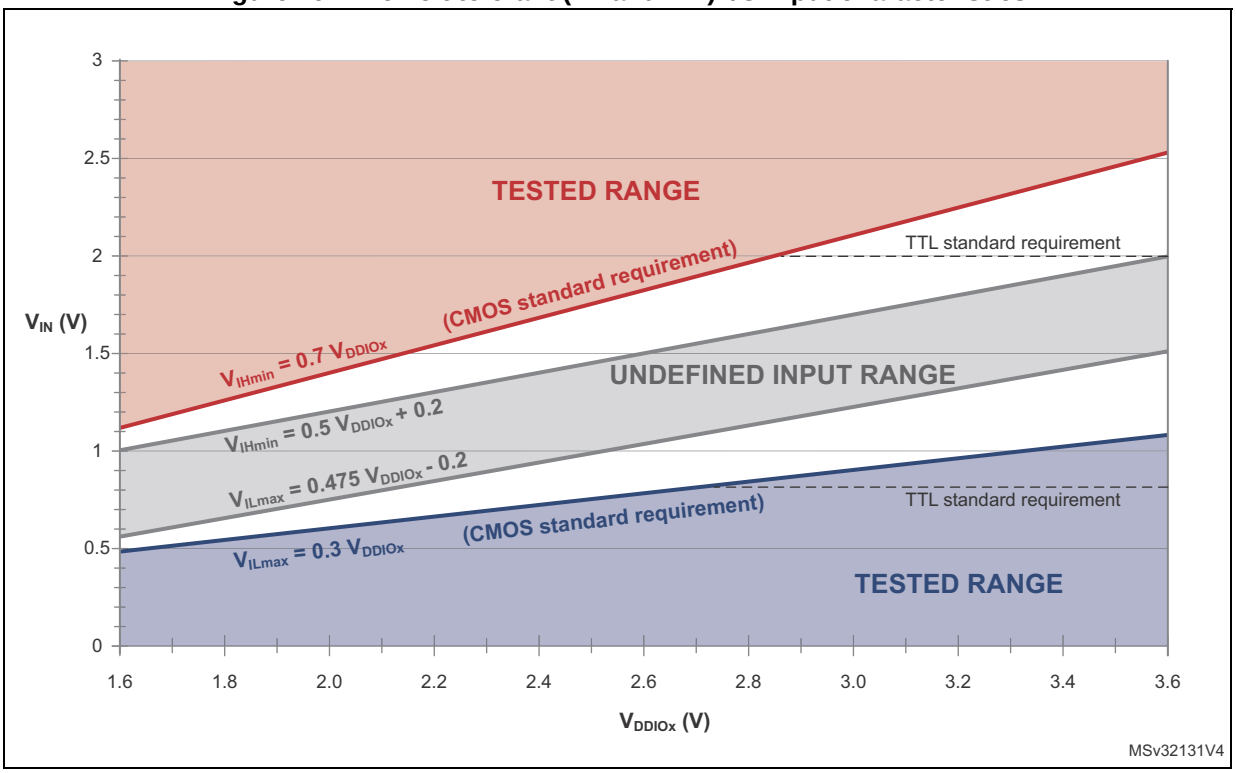
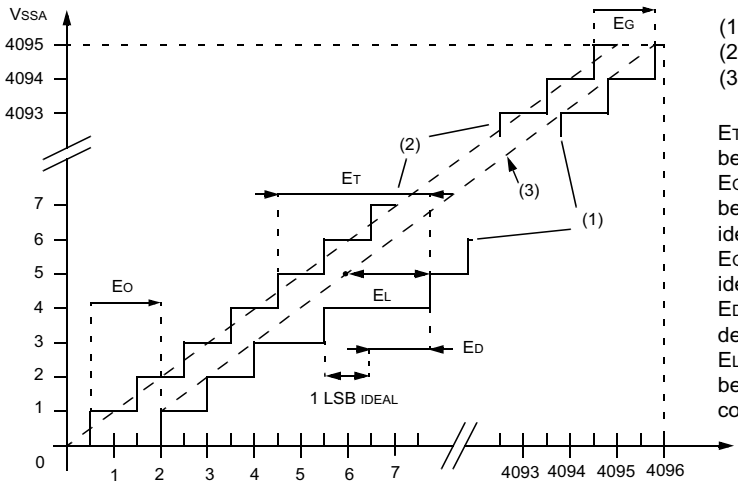


Figure 22. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

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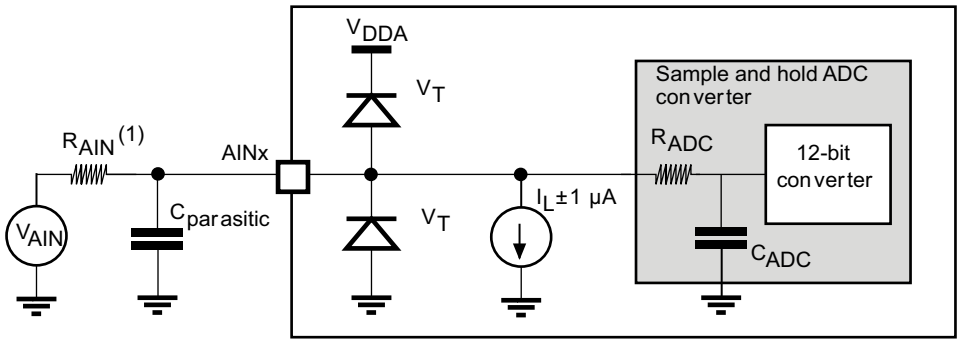
Figure 23. Typical connection diagram using the ADC



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1. Refer to *Table 50: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

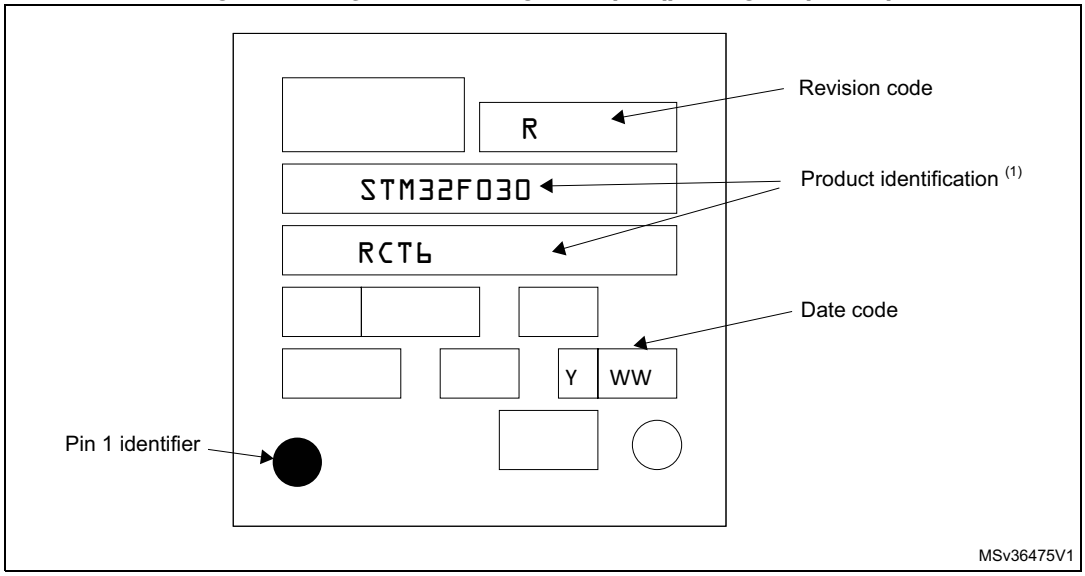
Power supply decoupling should be performed as shown in *Figure 12: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 29. LQFP64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 65. Document revision history (continued)

Date	Revision	Changes
23-Jan-2017	3	– *Section 3.11.2: General-purpose timers (TIM3, TIM14..17)* - number of timers – *Table 5: Timer feature comparison* - footnotes added – *Table 7: STM32F030x4/x6/x8/xC I^2C implementation* - FM+ and footnote – *Figure 3* through *Figure 6* - darker highlight on pins – *Table 11: STM32F030x4/6/8/C pin definitions* - corrections – *Table 12: Alternate functions selected through GPIOA_AFR registers for port A* - note order – *Table 14* through *Table 16* - corrected footnotes – *Figure 9: STM32F030x4/x6/x8/xC memory map* footnote – *Figure 12: Power supply scheme* – *Table 24: Embedded internal reference voltage*: added t_{START}, changed V_{REFINT} and $t_{S\_vrefint}$ values and notes – *Table 25: Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V* footnotes – *Table 26: Typical and maximum current consumption from the V_{DDA} supply* values for STM32F030xC and footnotes – *Table 34: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* LSEDRV[1:0] values removed (see ref. manual) – *Table 50: ADC characteristics* - t_{STAB} defined relative to clock frequency; notes *3.* and *4.* added – *Section 3.14: Universal synchronous/asynchronous receiver/transmitter (USART)* - introduction and *Table 8: STM32F0x0 USART implementation* – *Figure 9: STM32F030x4/x6/x8/xC memory map* footnote – *Table 43: ESD absolute maximum ratings* - C4 or C3 class, depending on device variant; CDM values updated to match the referenced standard. (CDM standard was updated in the previous release, without duly modifying the related values.) – *Table 53: TS characteristics*: removed the min. value for t_{START} and parameter name change – *Figure 18* and *Figure 19* improved – *Section 7: Package information* name and structure *change* – *Section 8: Ordering information* renamed from Part numbering