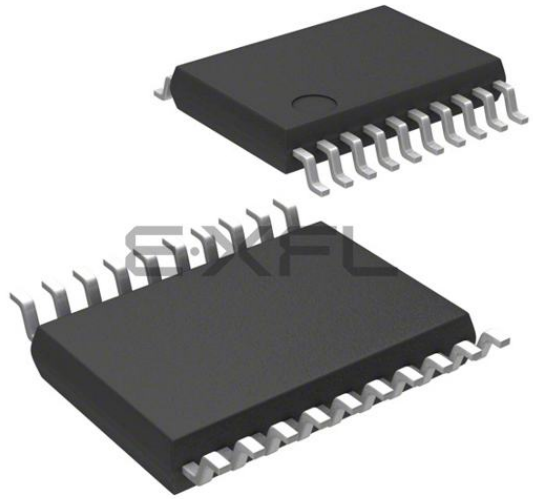

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	15
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f030f4p6tr

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F030x4/x6/x8/xC microcontrollers.

This document should be read in conjunction with the STM32F0x0xx reference manual (RM0360). The reference manual is available from the STMicroelectronics website *www.st.com*.

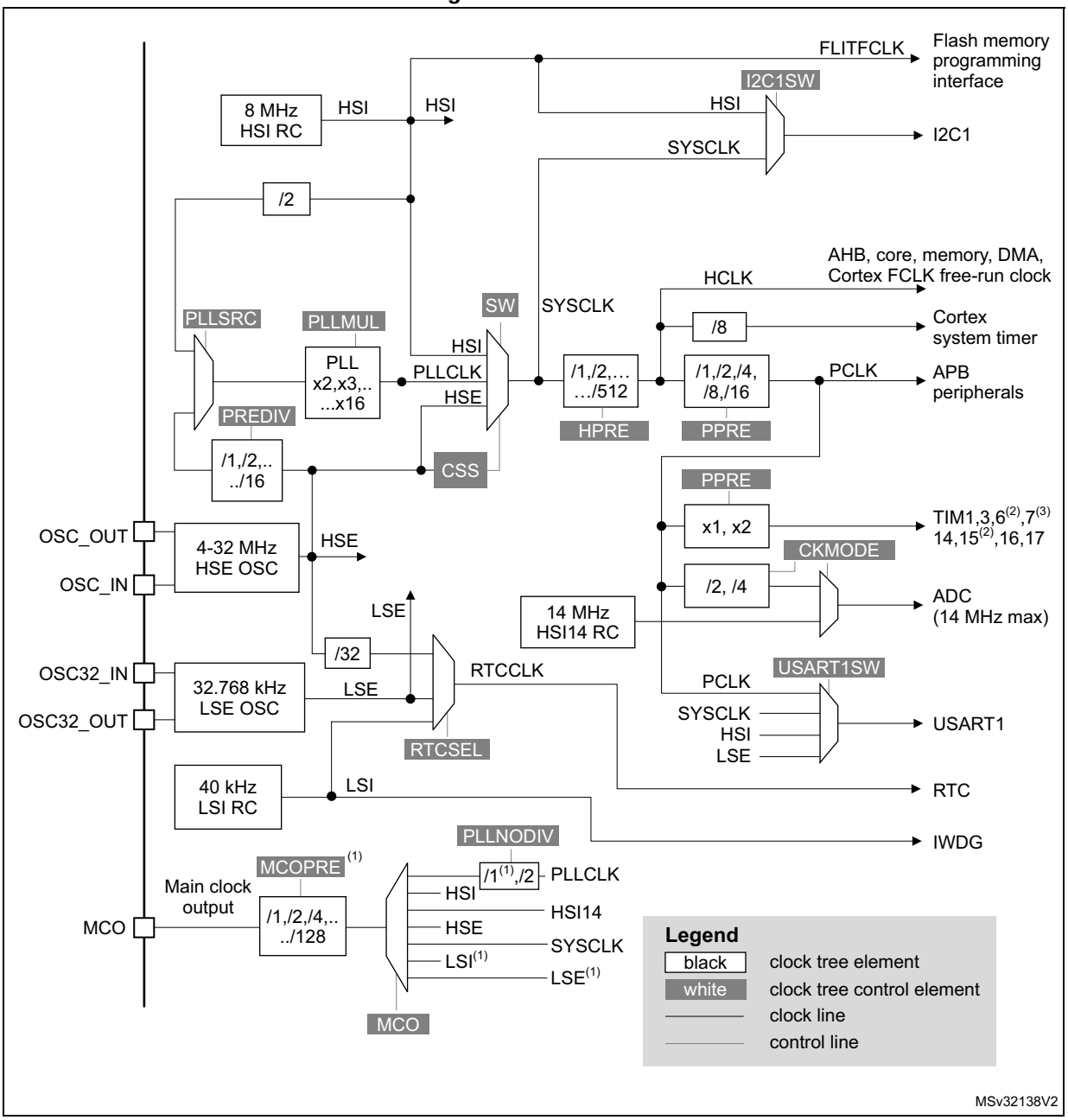
For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

Table 2. STM32F030x4/x6/x8/xC family device features and peripheral counts

Peripheral		STM32 F030F4	STM32 F030K6	STM32 F030C6	STM32 F030C8	STM32 F030CC	STM32 F030R8	STM32 F030RC
Flash (Kbytes)		16	32	32	64	256	64	256
SRAM (Kbytes)		4			8	32	8	32
Timers	Advanced control	1 (16-bit)						
	General purpose	4 (16-bit)(1)			5 (16-bit)			
	Basic	-			1 (16-bit)(2)	2 (16-bit)	1 (16-bit)(2)	2 (16-bit)
Comm. interfaces	SPI	1(3)			2			
	I^2C	1(4)			2			
	USART	1(5)			2(6)	6	2(6)	6
12-bit ADC (number of channels)		1 (9 ext. +2 int.)	1 (10 ext. +2 int.)	1 (10 ext. +2 int.)	1 (10 ext. +2 int.)	1 (10 ext. +2 int.)	1 (16 ext. +2 int.)	1 (16 ext. +2 int.)
GPIOs		15	26	39	39	37	55	51
Max. CPU frequency		48 MHz						
Operating voltage		2.4 to 3.6 V						
Operating temperature		Ambient operating temperature: -40°C to 85°C Junction temperature: -40°C to 105°C						
Packages		TSSOP20	LQFP32	LQFP48			LQFP64	

1. TIM15 is not present.
2. TIM7 is not present.
3. SPI2 is not present.
4. I2C2 is not present.
5. USART2 to USART6 are not present.
6. USART3 to USART6 are not present

Figure 2. Clock tree



1. Applies to STM32F030x4/x6/xC devices.
2. Applies to STM32F030x8/xC devices.
3. Applies to STM32F030xC devices.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

3.11 Timers and watchdogs

The STM32F030x4/x6/x8/xC devices include up to five general-purpose timers, two basic timers and one advanced control timer.

Table 5 compares the features of the different timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	-
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	-
	TIM15(1)	16-bit	Up	Any integer between 1 and 65536	Yes	2	-
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6,(1) TIM7(2)	16-bit	Up	Any integer between 1 and 65536	Yes	0	-

1. Available on STM32F030x8 and STM32F030xC devices only.
2. Available on STM32F030xC devices only

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

Table 9. STM32F030x4/x6/x8/xC SPI implementation(1)

SPI features	SPI1	SPI2(2)
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
TI mode	X	X

1. X = supported.
2. Not available on STM32F030x4/6.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
46	34	23	19	PA13 (SWDIO)	I/O	FT	(7)	IR_OUT, SWDIO	-
47(4)	35(4)	-	-	PF6	I/O	FT	(4)	I2C1_SCL(2), I2C2_SCL(3)	-
47(5)	35(5)	-	-	VSS	S	-	(5)	Ground	
48(4)	36(4)	-	-	PF7	I/O	FT	(4)	I2C1_SDA(2), I2C2_SDA(3)	-
48(5)	36(5)	-	-	VDD	S	-	(5)	Complementary power supply	
49	37	24	20	PA14 (SWCLK)	I/O	FT	(7)	USART1_TX(2), USART2_TX(3)(5), SWCLK	-
50	38	25	-	PA15	I/O	FT	-	SPI1_NSS, USART1_RX(2), USART2_RX(3)(5), USART4_RTS(5), EVENTOUT	-
51	-	-	-	PC10	I/O	FT	-	USART3_TX(5), USART4_TX(5)	-
52	-	-	-	PC11	I/O	FT	-	USART3_RX(5), USART4_RX(5)	-
53	-	-	-	PC12	I/O	FT	-	USART3_CK(5), USART4_CK(5), USART5_TX(5)	-
54	-	-	-	PD2	I/O	FT	-	TIM3_ETR, USART3_RTS(5), USART5_RX(5)	-
55	39	26	-	PB3	I/O	FT	-	SPI1_SCK, EVENTOUT, USART5_TX(5)	-
56	40	27	-	PB4	I/O	FT	-	SPI1_MISO, TIM3_CH1, EVENTOUT, TIM17_BKIN(5), USART5_RX(5)	-
57	41	28	-	PB5	I/O	FT	-	SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS(5)	WKPU6(5)

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

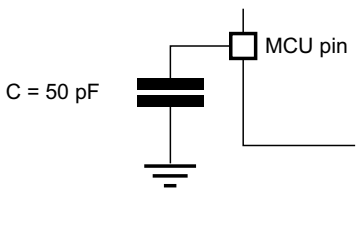


Figure 11. Pin input voltage

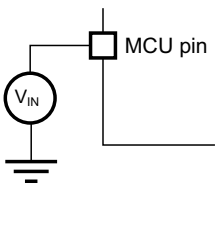


Table 19. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$(3)	Injected current on FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 18: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 52: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.4	3.6	V

Table 27. Typical and maximum consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
				3.6 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		19	48	µA
		Regulator in low-power mode, all oscillators OFF		5	32	
	Supply current in Standby mode	LSI ON and IWDG ON		2	-	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run or low-power mode, all oscillators OFF	2.9	3.5	
	Supply current in Standby mode		LSI ON and IWDG ON	3.3	-	
			LSI OFF and IWDG OFF	2.8	3.5	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run or low-power mode, all oscillators OFF	1.7	-	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	-	
			LSI OFF and IWDG OFF	1.4	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

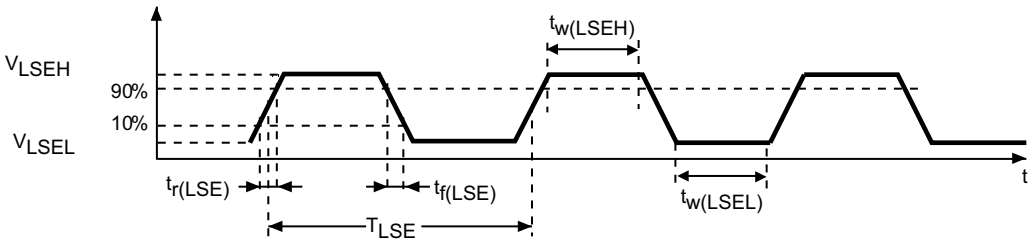
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 32. Low-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 33*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 33. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

obtained with typical external components specified in *Table 34*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

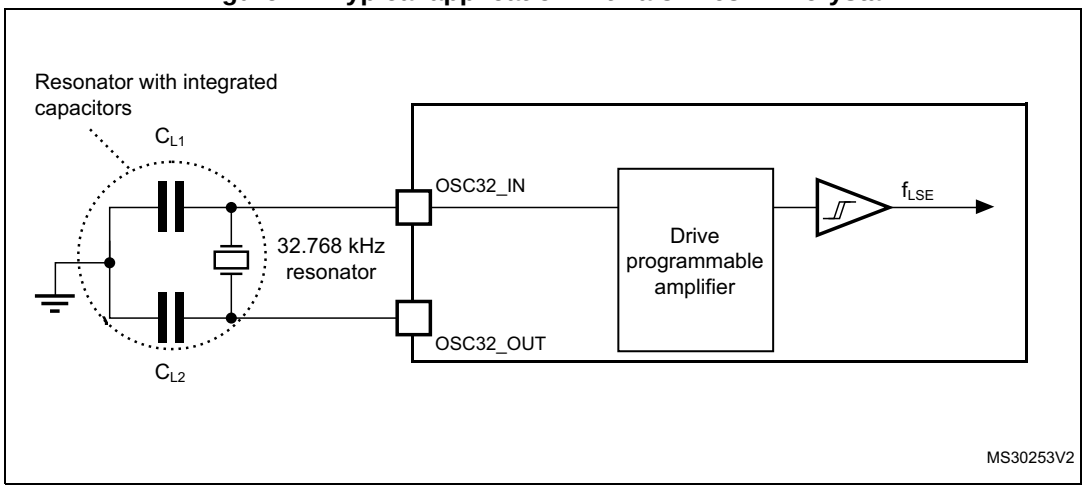
Table 34. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	µA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	µA/V
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 17. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 47. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6 mA	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
$V_{OLFm+}^{(2)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\|$ = 10 mA	-	0.4	V

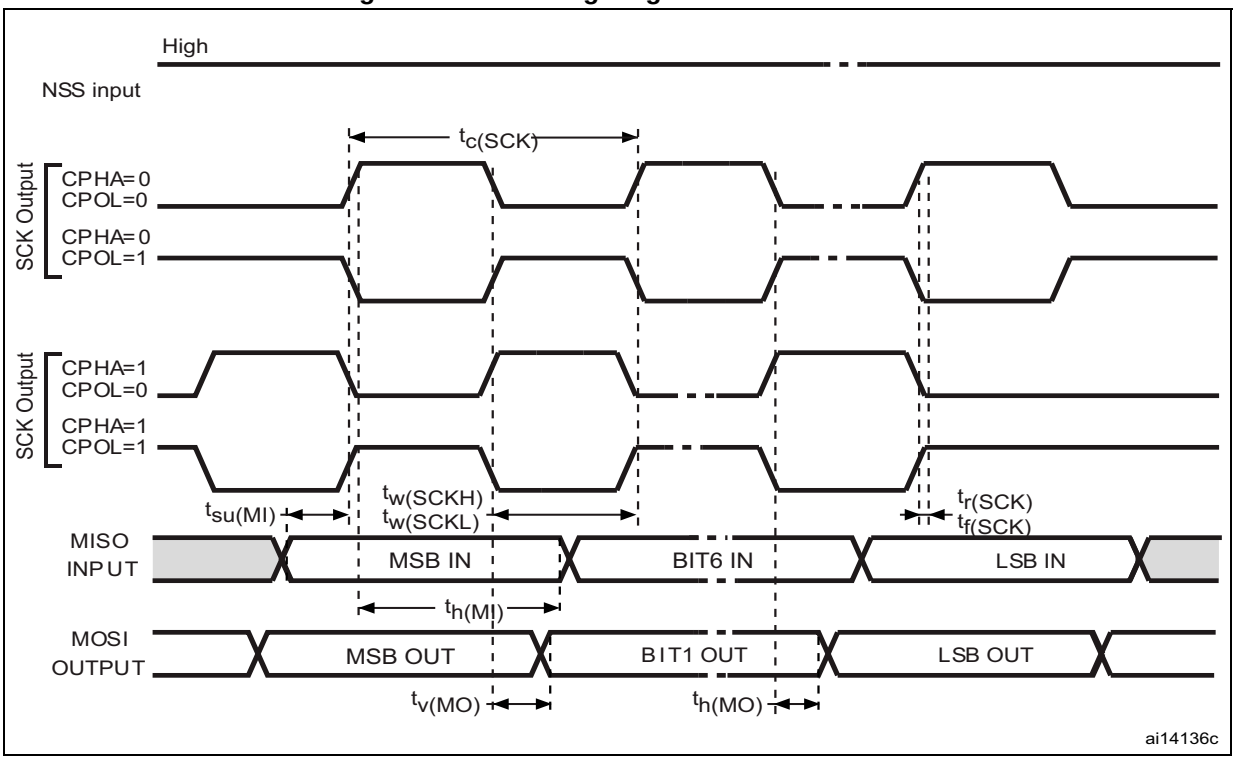
1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 48*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Figure 26. SPI timing diagram - master mode



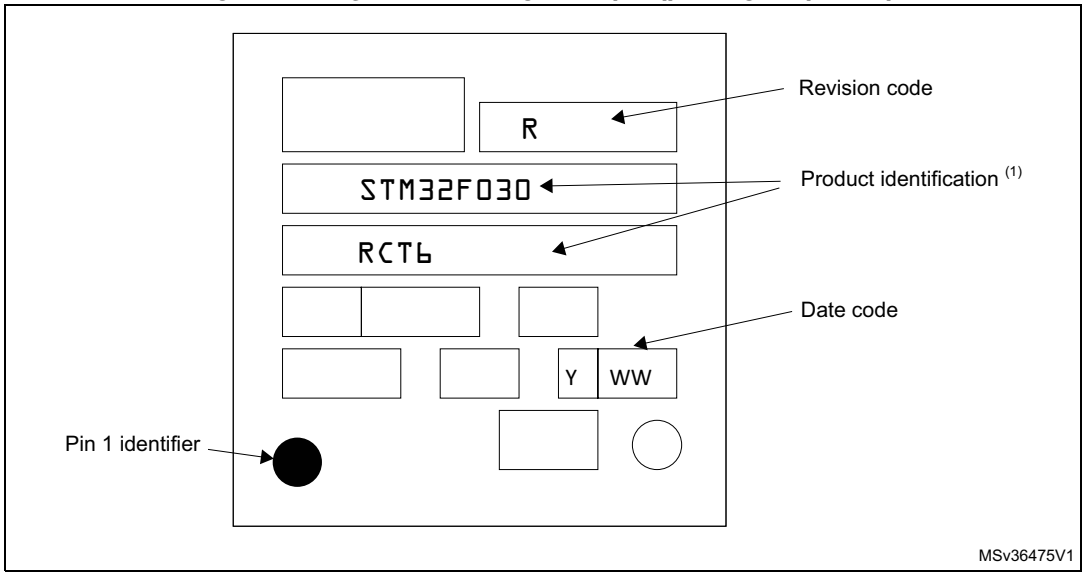
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 29. LQFP64 marking example (package top view)



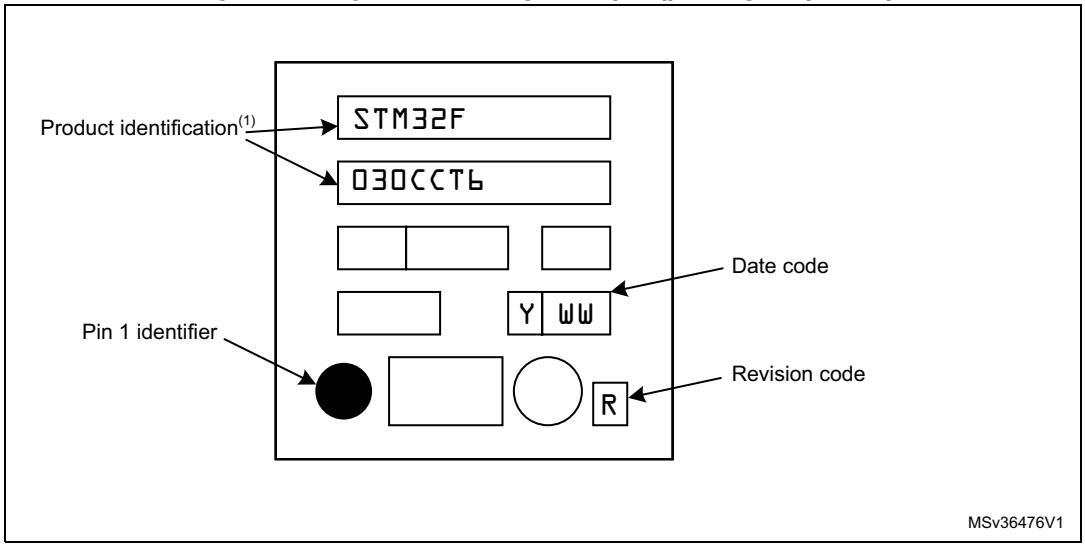
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 32. LQFP48 marking example (package top view)



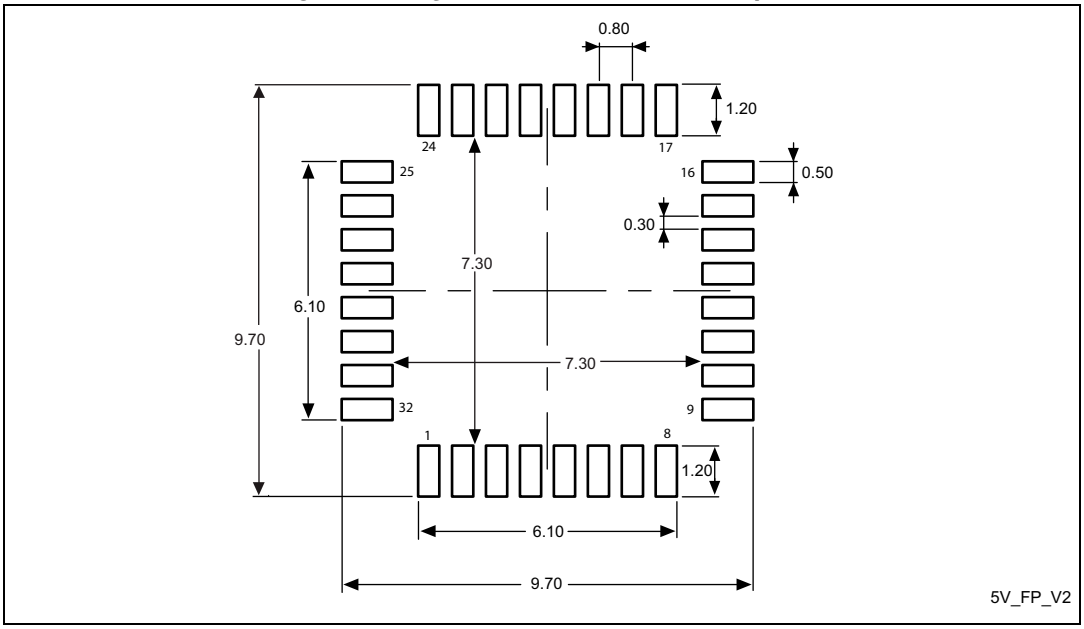
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 61. LQFP32 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. LQFP32 recommended footprint



1. Dimensions are expressed in millimeters.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 21: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 63. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_J	**Thermal resistance junction-ambient** LQFP64 - 10 mm x 10 mm	44	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 mm x 7 mm	55	
	Thermal resistance junction-ambient LQFP32 - 7 mm x 7 mm	56	
	Thermal resistance junction-ambient TSSOP20 - 6.5 mm x 6.4 mm	76	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

Table 65. Document revision history (continued)

Date	Revision	Changes
23-Jan-2017	3	– *Section 3.11.2: General-purpose timers (TIM3, TIM14..17)* - number of timers – *Table 5: Timer feature comparison* - footnotes added – *Table 7: STM32F030x4/x6/x8/xC I^2C implementation* - FM+ and footnote – *Figure 3* through *Figure 6* - darker highlight on pins – *Table 11: STM32F030x4/6/8/C pin definitions* - corrections – *Table 12: Alternate functions selected through GPIOA_AFR registers for port A* - note order – *Table 14* through *Table 16* - corrected footnotes – *Figure 9: STM32F030x4/x6/x8/xC memory map* footnote – *Figure 12: Power supply scheme* – *Table 24: Embedded internal reference voltage*: added t_{START}, changed V_{REFINT} and $t_{S\_vrefint}$ values and notes – *Table 25: Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V* footnotes – *Table 26: Typical and maximum current consumption from the V_{DDA} supply* values for STM32F030xC and footnotes – *Table 34: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* LSEDRV[1:0] values removed (see ref. manual) – *Table 50: ADC characteristics* - t_{STAB} defined relative to clock frequency; notes *3.* and *4.* added – *Section 3.14: Universal synchronous/asynchronous receiver/transmitter (USART)* - introduction and *Table 8: STM32F0x0 USART implementation* – *Figure 9: STM32F030x4/x6/x8/xC memory map* footnote – *Table 43: ESD absolute maximum ratings* - C4 or C3 class, depending on device variant; CDM values updated to match the referenced standard. (CDM standard was updated in the previous release, without duly modifying the related values.) – *Table 53: TS characteristics*: removed the min. value for t_{START} and parameter name change – *Figure 18* and *Figure 19* improved – *Section 7: Package information* name and structure *change* – *Section 8: Ordering information* renamed from Part numbering