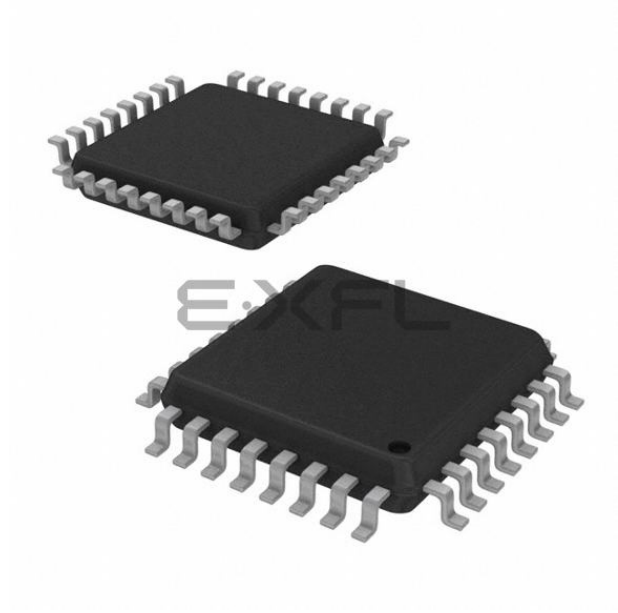

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f030k6t6 |

# 2 Description

The STM32F030x4/x6/x8/xC microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 256 Kbytes of Flash memory and up to 32 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two $I^2C$s, up to two SPIs and up to six USARTs), one 12-bit ADC, seven general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F030x4/x6/x8/xC microcontrollers operate in the -40 to +85 °C temperature range from a 2.4 to 3.6V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F030x4/x6/x8/xC microcontrollers include devices in four different packages ranging from 20 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F030x4/x6/x8/xC peripherals proposed.

These features make the STM32F030x4/x6/x8/xC microcontrollers suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

## 3.11 Timers and watchdogs

The STM32F030x4/x6/x8/xC devices include up to five general-purpose timers, two basic timers and one advanced control timer.

*Table 5* compares the features of the different timers.

**Table 5. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | 3 |
| General purpose | TIM3 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | - |
| | TIM15(1) | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | - |
| | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6,(1) TIM7(2) | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | - |

1. Available on STM32F030x8 and STM32F030xC devices only.
2. Available on STM32F030xC devices only

### 3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

### 3.11.2 General-purpose timers (TIM3, TIM14..17)

There are four or five synchronizable general-purpose timers embedded in the STM32F030x4/x6/x8/xC devices (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

#### TIM3

STM32F030x4/x6/x8/xC devices feature one synchronizable 4-channel general-purpose timer. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM3 general-purpose timer can work with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM3 has an independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

The counter can be frozen in debug mode.

#### TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

#### TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

### 3.11.3 Basic timers TIM6 and TIM7

These timers can be used as a generic 16-bit time base.

### 3.11.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It

**Figure 7. LQFP32 32-pin package pinout (top view)**

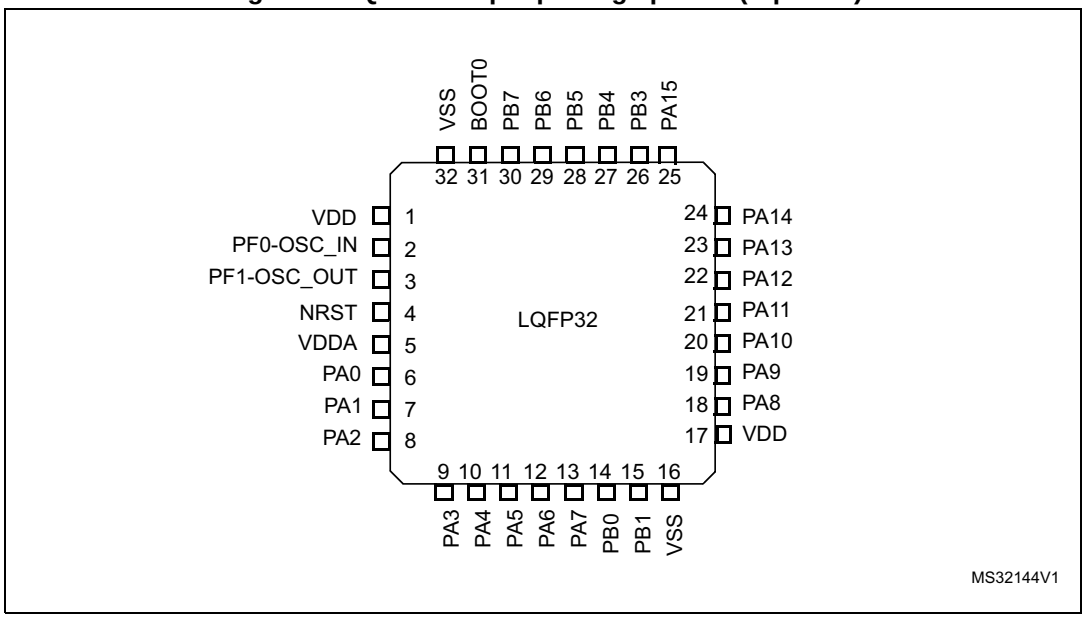



**Figure 8. TSSOP20 20-pin package pinout (top view)**

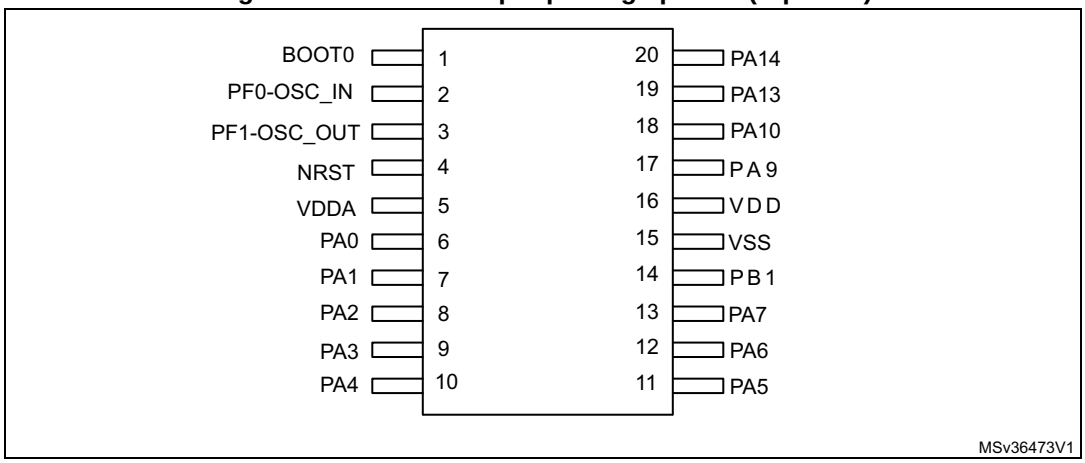


Table 11. STM32F030x4/6/8/C pin definitions (continued)

| Pin number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP48 | LQFP32 | TSSOP20 | | | | | Alternate functions | Additional functions |
| 22 | 16 | 12 | 12 | PA6 | I/O | TTa | - | SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT USART3_CTS(5) | ADC_IN6 |
| 23 | 17 | 13 | 13 | PA7 | I/O | TTa | - | SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT | ADC_IN7 |
| 24 | - | - | - | PC4 | I/O | TTa | - | EVENTOUT, USART3_TX(5) | ADC_IN14 |
| 25 | - | - | - | PC5 | I/O | TTa | - | USART3_RX(5) | ADC_IN15, WKPU5(5) |
| 26 | 18 | 14 | - | PB0 | I/O | TTa | - | TIM3_CH3, TIM1_CH2N, EVENTOUT, USART3_CK(5) | ADC_IN8 |
| 27 | 19 | 15 | 14 | PB1 | I/O | TTa | - | TIM3_CH4, TIM14_CH1, TIM1_CH3N, USART3_RTS(5) | ADC_IN9 |
| 28 | 20 | - | - | PB2 | I/O | FT | (6) | - | - |
| 29 | 21 | - | - | PB10 | I/O | FT | - | SPI2_SCK(5), I2C1_SCL(2), I2C2_SCL(3)(5), USART3_TX(5) | - |
| 30 | 22 | - | - | PB11 | I/O | FT | - | I2C1_SDA(2), I2C2_SDA(3)(5), EVENTOUT, USART3_RX(5) | - |
| 31 | 23 | 16 | - | VSS | S | - | - | Ground | |
| 32 | 24 | 17 | 16 | VDD | S | - | - | Digital power supply | |
| 33 | 25 | - | - | PB12 | I/O | FT | - | SPI1_NSS(2), SPI2_NSS(3)(5), TIM1_BKIN, EVENTOUT, USART3_CK(5) | - |

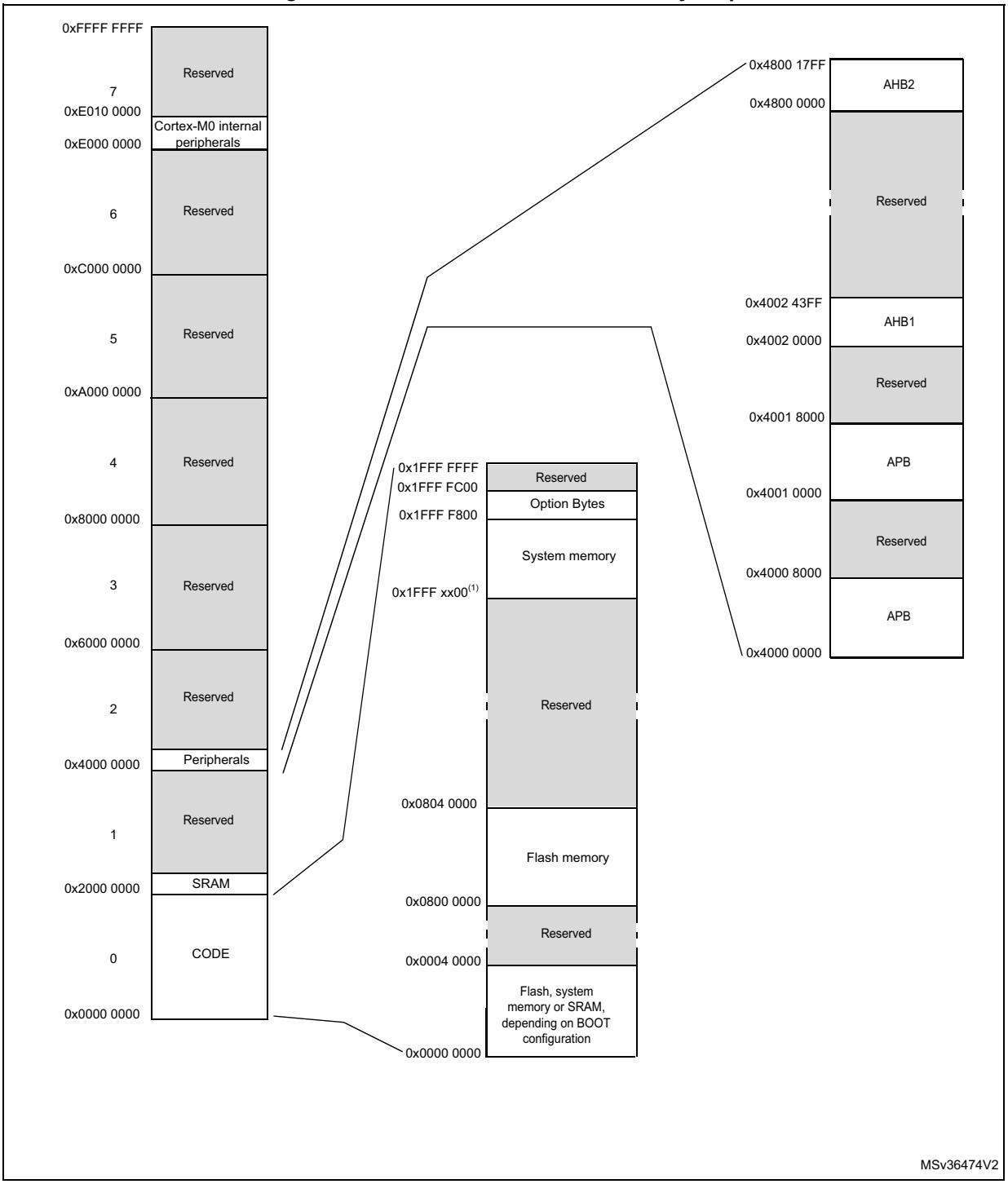
**Table 13. Alternate functions selected through GPIOB_AFR registers for port B (continued)**

| Pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 |
|---|---|---|---|---|---|---|
| PB8 | - | I2C1_SCL | TIM16_CH1 | - | - | - |
| PB9 | IR_OUT | I2C1_SDA | TIM17_CH1 | EVENTOUT | - | SPI2_NSS(1) |
| PB10 | - | I2C1_SCL(2) | - | - | USART3_TX(1) | SPI2_SCK(1) |
| | | I2C2_SCL(1)(3) | | | USART3_RX(1) | - |
| PB11 | EVENTOUT | I2C1_SDA(2) | - | - | USART3_RX(1) | - |
| | | I2C2_SDA(1)(3) | | | | |
| PB12 | SPI1_NSS(2) | EVENTOUT | TIM1_BKIN | - | USART3_RTS(1) | TIM15(1) |
| | SPI2_NSS(1)(3) | | | | | |
| PB13 | SPI1_SCK(2) | - | TIM1_CH1N | - | USART3_CTS((1) | I2C2_SCL(1) |
| | SPI2_SCK(1)(3) | | | | | |
| PB14 | SPI1_MISO(2) | TIM15_CH1(1)(3) | TIM1_CH2N | - | USART3_RTS(1) | I2C2_SDA(1) |
| | SPI2_MISO(1)(3) | | | | | |
| PB15 | SPI1_MOSI(2) | TIM15_CH2(1)(3) | TIM1_CH3N | TIM15_CH1N(1)(3) | - | - |
| | SPI2_MOSI(1)(3) | | | | | |

1. This feature is available on STM32F030xC devices.
2. This feature is available on STM32F030x4 and STM32F030x6 devices.
3. This feature is available on STM32F030x8 devices.

# 5 Memory mapping

**Figure 9. STM32F030x4/x6/x8/xC memory map**




1. The start address of the system memory is 0x1FFF EC00 for STM32F030x4, STM32F030x6 and STM32F030x8 devices, and 0x1FFF D800 for STM32F030xC devices.

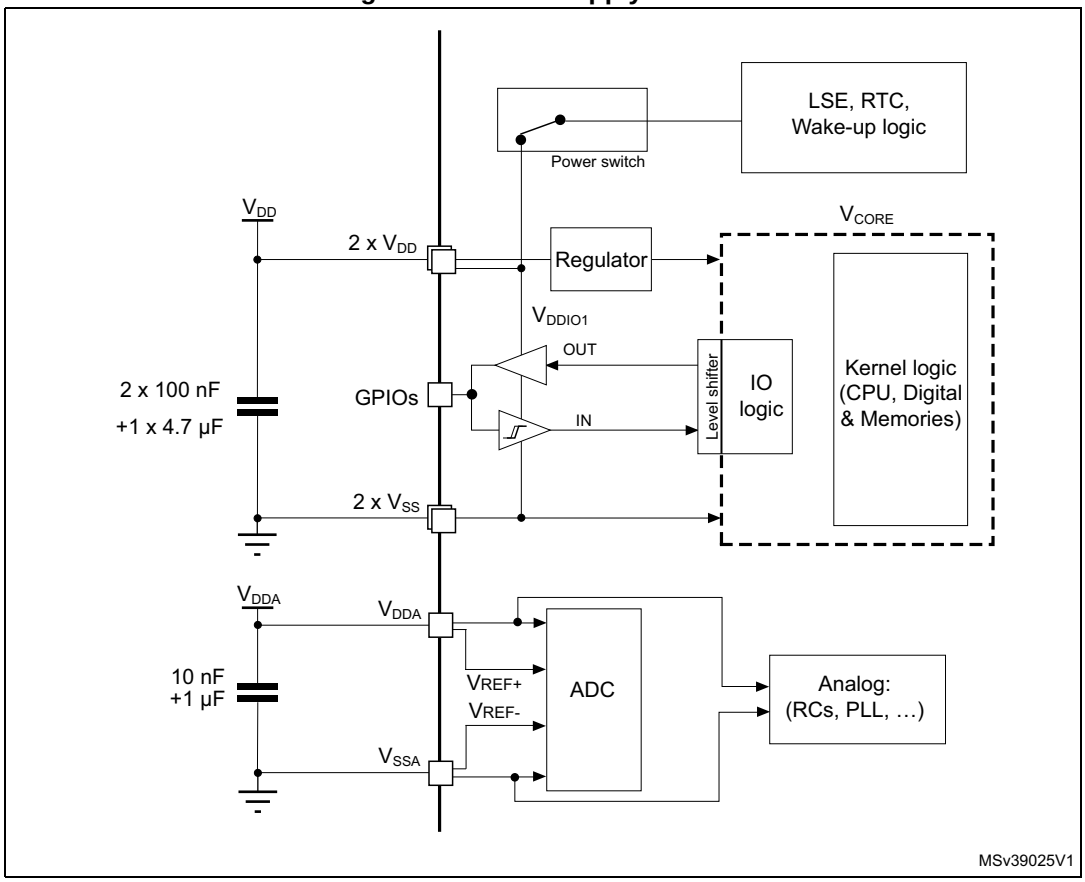
**Table 17. STM32F030x4/x6/x8/xC peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| - | 0x4000 8000 - 0x4000 FFFF | 32 KB | Reserved |
| APB | 0x4000 7400 - 0x4000 7FFF | 3 KB | Reserved |
| | 0x4000 7000 - 0x4000 73FF | 1 KB | PWR |
| | 0x4000 5C00 - 0x4000 6FFF | 5 KB | Reserved |
| | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2(1) |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | 1 KB | USART5(2) |
| | 0x4000 4C00 - 0x4000 4FFF | 1 KB | USART4(2) |
| | 0x4000 4800 - 0x4000 4BFF | 1 KB | USART3(2) |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2(1) |
| | 0x4000 3C00 - 0x4000 43FF | 2 KB | Reserved |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2(1) |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 2400 - 0x4000 27FF | 1 KB | Reserved |
| | 0x4000 2000 - 0x4000 23FF | 1 KB | TIM14 |
| | 0x4000 1800 - 0x4000 1FFF | 2 KB | Reserved |
| | 0x4000 1400 - 0x4000 17FF | 1 KB | TIM7(2) |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6(1) |
| | 0x4000 0800 - 0x4000 0FFF | 2 KB | Reserved |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | Reserved |

1. This feature is available on STM32F030x8 and STM32F030xC devices only. For STM32F030x6 and STM32F060x4, the area is Reserved.
2. This feature is available on STM32F030xC devices only. This area is reserved for STM32F030x4/6/8 devices.

### 6.1.6 Power supply scheme

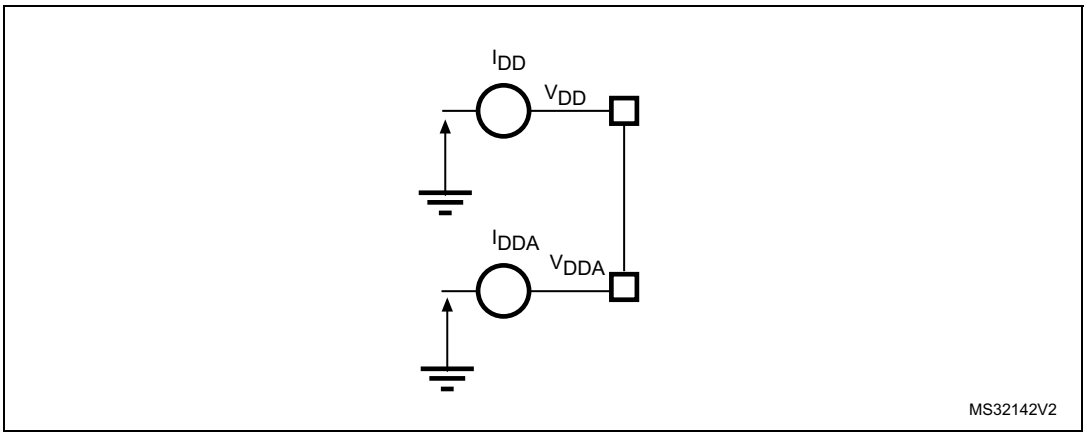
**Figure 12. Power supply scheme**




**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### 6.1.7 Current consumption measurement

**Figure 13. Current consumption measurement scheme**



### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 25* to *Table 27* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

**Table 25. Typical and maximum current consumption from $V_{DD}$ supply at $V_{DD}$ = 3.6 V(1)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | All peripherals enabled | | Unit |
|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$(2) 85 °C | |
| $I_{DD}$ | Supply current in Run mode, code executing from Flash | HSI or HSE clock, PLL on | 48 MHz | 22.0 | 22.8 | mA |
| | | | 48 MHz | 26.8 | 30.2 | |
| | | | 24 MHz | 12.2 | 13.2 | |
| | | | 24 MHz | 14.1 | 16.2 | |
| | | HSI or HSE clock, PLL off | 8 MHz | 4.4 | 5.2 | |
| | | | 8 MHz | 4.9 | 5.6 | |
| $I_{DD}$ | Supply current in Run mode, code executing from RAM | HSI or HSE clock, PLL on | 48 MHz | 22.2 | 23.2 | mA |
| | | | 48 MHz | 26.1 | 29.3 | |
| | | | 24 MHz | 11.2 | 12.2 | |
| | | | 24 MHz | 13.3 | 15.7 | |
| | | HSI or HSE clock, PLL off | 8 MHz | 4.0 | 4.5 | |
| | | | 8 MHz | 4.6 | 5.2 | |
| $I_{DD}$ | Supply current in Sleep mode, code executing from Flash or RAM | HSI or HSE clock, PLL on | 48 MHz | 14 | 15.3 | mA |
| | | | 48 MHz | 17.0 | 19.0 | |
| | | | 24 MHz | 7.3 | 7.8 | |
| | | | 24 MHz | 8.7 | 10.1 | |
| | | HSI or HSE clock, PLL off | 8 MHz | 2.6 | 2.9 | |
| | | | 8 MHz | 3.0 | 3.5 | |

1. The gray shading is used to distinguish the values for STM32F030xC devices.
2. Data based on characterization results, not tested in production unless otherwise specified.

**Table 27. Typical and maximum consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | | Typ @$V_{DD}$ ($V_{DD}$ = $V_{DDA}$) | Max(1) | Unit |
|---|---|---|---|---|---|---|
| | | | | 3.6 V | $T_A$ = 85 °C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in run mode, all oscillators OFF | | 19 | 48 | µA |
| | | Regulator in low-power mode, all oscillators OFF | | 5 | 32 | |
| | Supply current in Standby mode | LSI ON and IWDG ON | | 2 | - | |
| $I_{DDA}$ | Supply current in Stop mode | $V_{DDA}$ monitoring ON | Regulator in run or low-power mode, all oscillators OFF | 2.9 | 3.5 | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 3.3 | - | |
| | | | LSI OFF and IWDG OFF | 2.8 | 3.5 | |
| | Supply current in Stop mode | $V_{DDA}$ monitoring OFF | Regulator in run or low-power mode, all oscillators OFF | 1.7 | - | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 2.3 | - | |
| | | | LSI OFF and IWDG OFF | 1.4 | - | |

1. Data based on characterization results, not tested in production unless otherwise specified.

### Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD}$ = $V_{DDA}$ = 3.3 V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to $f_{HCLK}$ frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK}$ = $f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 42. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/48 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | -3 | dBµV |
| | | | 30 to 130 MHz | 23 | |
| | | | 130 MHz to 1 GHz | 17 | |
| | | | EMI Level | 4 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 43. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Packages | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | All | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1 | All | C4(2)<br>C3(3) | 500(2)<br>250(3) | V |

1. Data based on characterization results, not tested in production.
2. Applicable to STM32F030xC
3. Applicable to STM32F030x4, STM32F030x6, and STM32F030x8

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 44. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DDIOx}$ (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 45*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

**Table 45. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 and PF1 pins | -0 | NA | mA |
| | Injected current on PA9, PB3, PB13, PF11 pins with induced leakage current on adjacent pins less than 50 µA | -5 | NA | |
| | Injected current on PA11 and PA12 pins with induced leakage current on adjacent pins less than -1 mA | -5 | NA | |
| | Injected current on all other FT and FTf pins | -5 | NA | |
| | Injected current on PB0 and PB1 pins | -5 | NA | |
| | Injected current on PC0 pin | -0 | +5 | |
| | Injected current on all other TTa, TC and RST pins | -5 | +5 | |

## 6.3.14 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

**Table 46. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low level input voltage | TC and TTa I/O | - | - | $0.3\ V_{DDIOx}+0.07$(1) | V |
| | | FT and FTf I/O | - | - | $0.475\ V_{DDIOx}-0.2$(1) | |
| | | BOOT0 | - | - | $0.3\ V_{DDIOx}-0.3$(1) | |
| | | All I/Os except BOOT0 pin | - | - | $0.3\ V_{DDIOx}$ | |
| $V_{IH}$ | High level input voltage | TC and TTa I/O | $0.445\ V_{DDIOx}+0.398$(1) | - | - | V |
| | | FT and FTf I/O | $0.5\ V_{DDIOx}+0.2$(1) | - | - | |
| | | BOOT0 | $0.2\ V_{DDIOx}+0.95$(1) | - | - | |
| | | All I/Os except BOOT0 pin | $0.7\ V_{DDIOx}$ | - | - | |
| $V_{hys}$ | Schmitt trigger hysteresis | TC and TTa I/O | - | 200(1) | - | mV |
| | | FT and FTf I/O | - | 100(1) | - | |
| | | BOOT0 | - | 300(1) | - | |

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$, plus the maximum consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 18: Voltage characteristics*).

### Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

**Table 47. Output voltage characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 8 mA<br>$V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | |
| $V_{OL}^{(2)}$ | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 20 mA<br>$V_{DDIOx} \geq 2.7$ V | - | 1.3 | V |
| $V_{OH}^{(2)}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$–1.3 | - | |
| $V_{OL}^{(2)}$ | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 6 mA | - | 0.4 | V |
| $V_{OH}^{(2)}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | |
| $V_{OLFm+}^{(2)}$ | Output low level voltage for an FTf I/O pin in Fm+ mode | $\|I_{IO}\|$ = 20 mA<br>$V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| | | $\|I_{IO}\|$ = 10 mA | - | 0.4 | V |

1. The $I_{IO}$ current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{IO}$.
2. Data based on characterization results. Not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 48*, respectively.

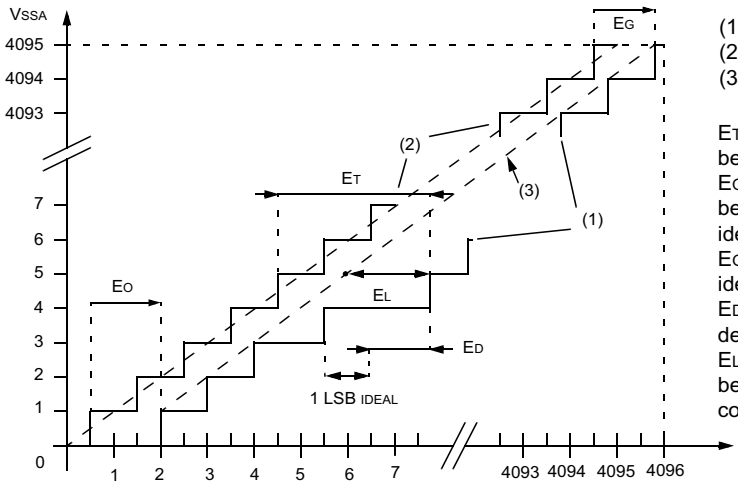
Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

**Table 48. I/O AC characteristics(1)(2)**

| OSPEEDRy [1:0] value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| x0 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx} \geq$ 2.4 V | - | 2 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 125 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 125 | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx} \geq$ 2.4 V | - | 10 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 25 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 25 | |
| 11 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DDIOx} \geq$ 2.7 V | - | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DDIOx} \geq$ 2.7 V | - | 30 | |
| | | | $C_L$ = 50 pF, 2.4 V $\leq V_{DDIOx} <$ 2.7 V | - | 20 | |
| | $t_{f(IO)out}$ | Output fall time | $C_L$ = 30 pF, $V_{DDIOx} \geq$ 2.7 V | - | 5 | ns |
| | | | $C_L$ = 50 pF, $V_{DDIOx} \geq$ 2.7 V | - | 8 | |
| | | | $C_L$ = 50 pF, 2.4 V $\leq V_{DDIOx} <$ 2.7 V | - | 12 | |
| | $t_{r(IO)out}$ | Output rise time | $C_L$ = 30 pF, $V_{DDIOx} \geq$ 2.7 V | - | 5 | |
| | | | $C_L$ = 50 pF, $V_{DDIOx} \geq$ 2.7 V | - | 8 | |
| | | | $C_L$ = 50 pF, 2.4 V $\leq V_{DDIOx} <$ 2.7 V | - | 12 | |
| Fm+ configuration (4) | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx} \geq$ 2.4 V | - | 2 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 12 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 34 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0360 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 20*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0360 for a detailed description of Fm+ I/O configuration.

**Figure 22. ADC accuracy characteristics**




(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$ = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
$E_O$ = Offset Error: maximum deviation between the first actual transition and the first ideal one.
$E_G$ = Gain Error: deviation between the last ideal transition and the last actual one.
$E_D$ = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
$E_L$ = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

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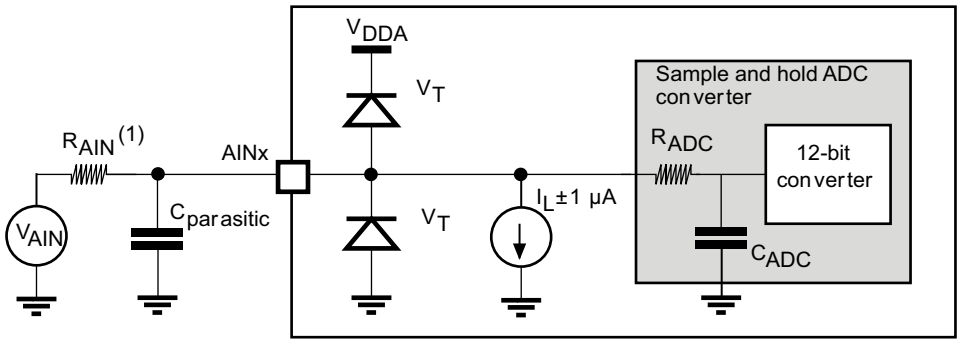
**Figure 23. Typical connection diagram using the ADC**

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1. Refer to *Table 50: ADC characteristics* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 12: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

**Figure 24. SPI timing diagram - slave mode and CPHA = 0**

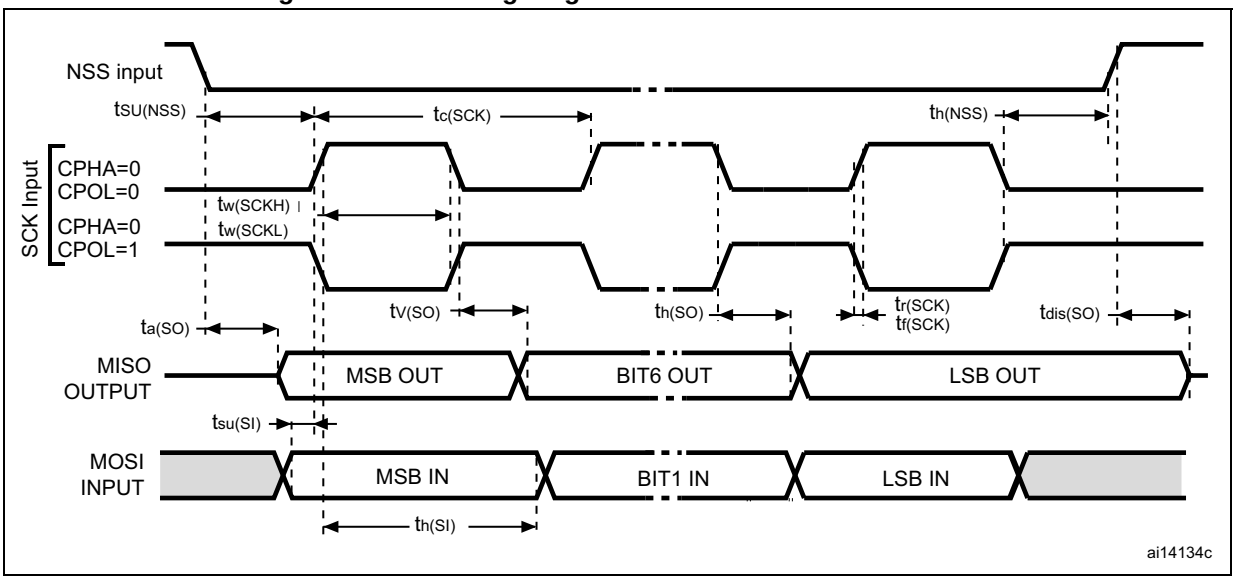
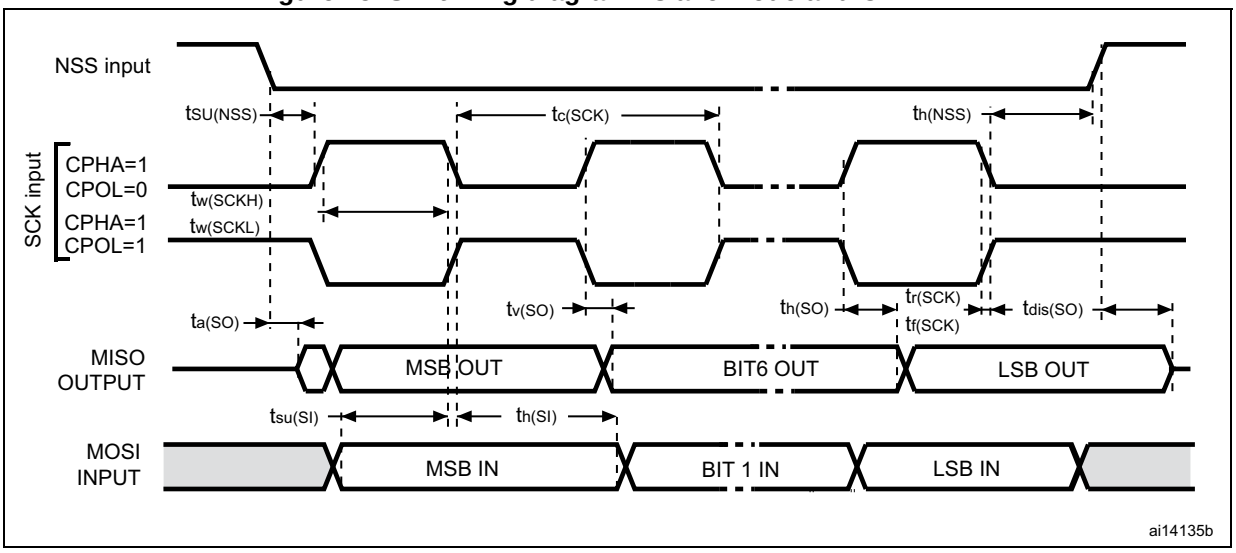



**Figure 25. SPI timing diagram - slave mode and CPHA = 1**




1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.