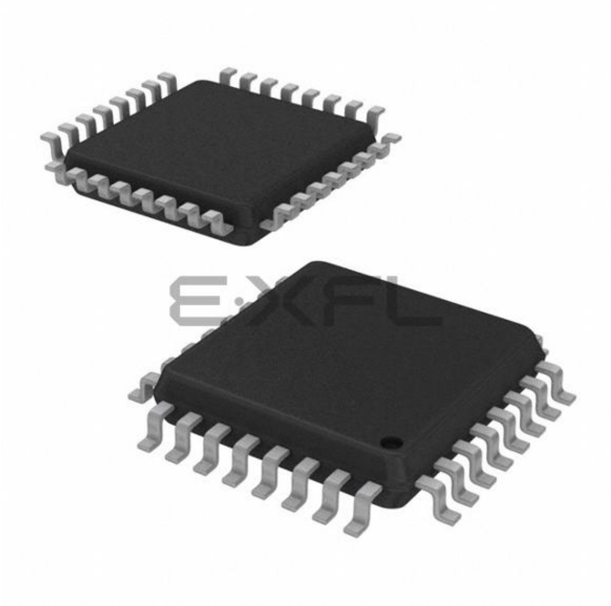
STMicroelectronics - STM32F030K6T6TR Datasheet



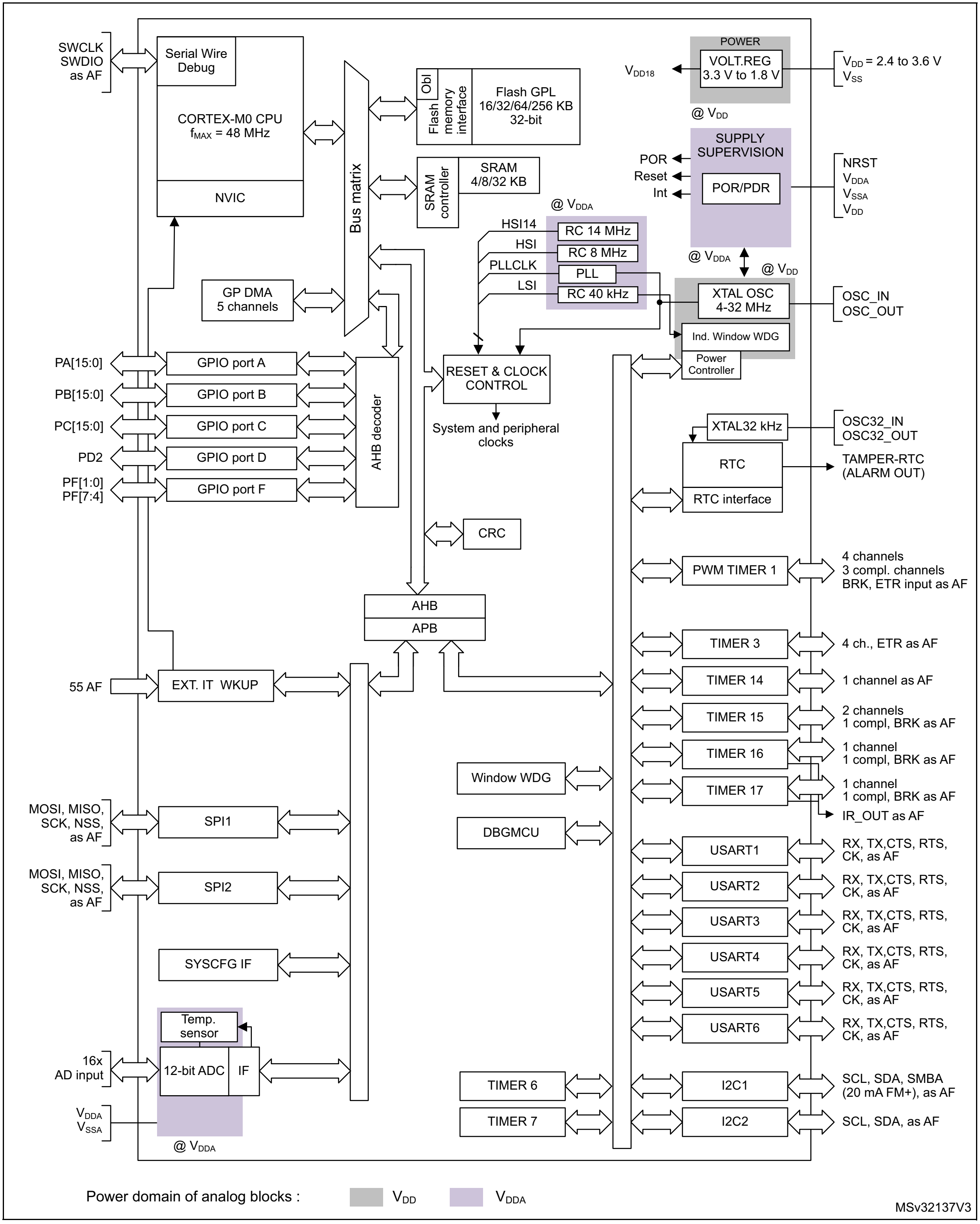
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

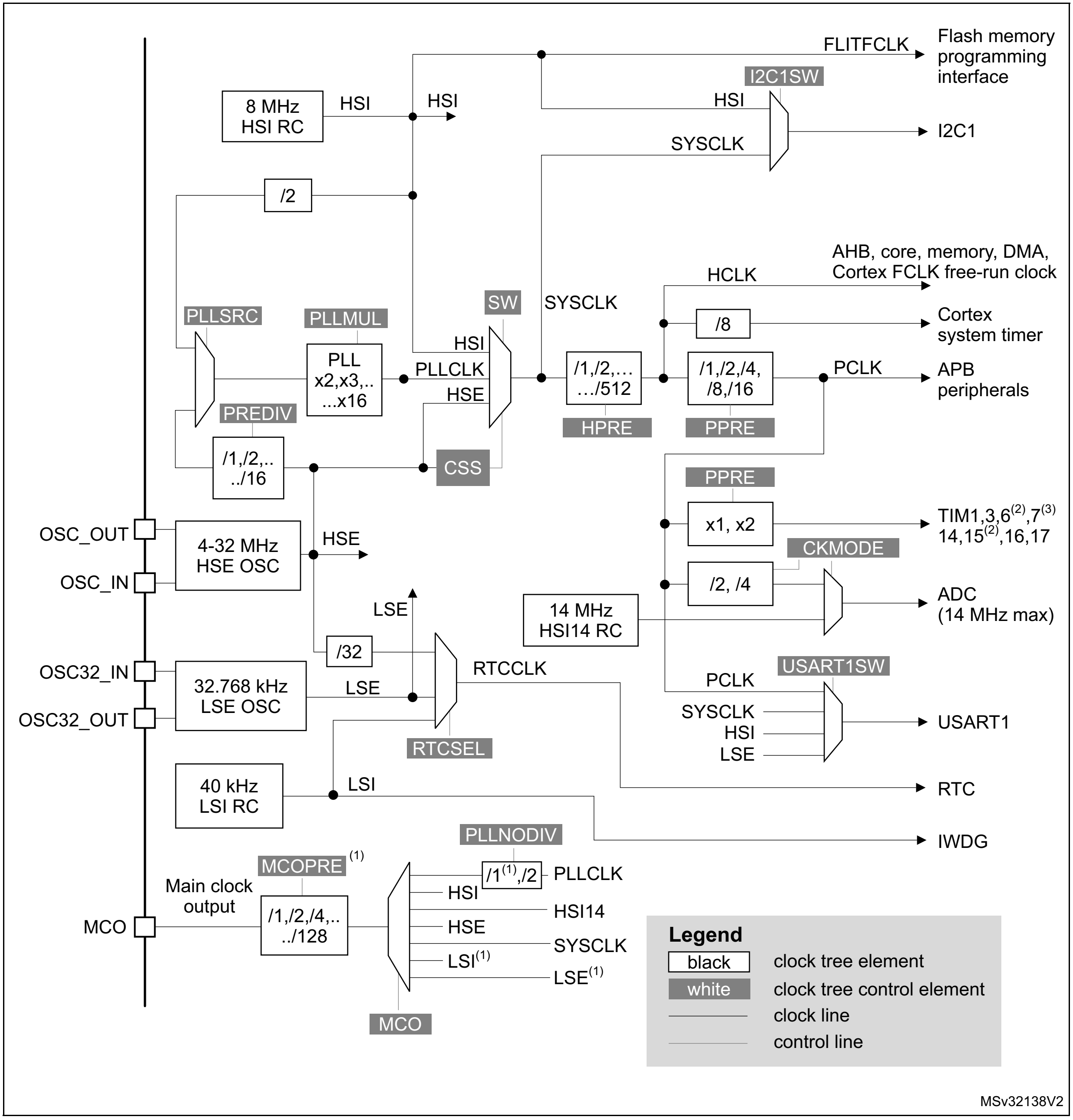
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f030k6t6tr

Figure 1. Block diagram



1. TIMER6, TIMER15, SPI, USART2 and I2C2 are available on STM32F030x8/C devices only.
2. USART3, USART4, USART5, USART6 and TIMER7 are available on STM32F030xC devices only.

Figure 2. Clock tree



1. Applies to STM32F030x4/x6/xC devices.
2. Applies to STM32F030x8/xC devices.
3. Applies to STM32F030xC devices.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

3.13 Inter-integrated circuit interfaces (I^2C)

Up to two I2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) or Fast mode (up to 400 kbit/s). I2C1 also supports Fast Mode Plus (up to 1 Mbit/s), with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	-

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management

The I2C interfaces can be served by the DMA controller.

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F030x4/x6/x8/xC I^2C implementation(1)

I2C features	I2C1	I2C2(2)
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s), with 20mA output drive I/Os	X	-
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	-	-

1. X = supported.
2. Only available on STM32F030x8/C devices.

3.14 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to six universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 6 Mbit/s.

Table 21. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	Analog operating voltage	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3(2)	
		FT and FTf I/O	-0.3	5.5(2)	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 (1)	LQFP64	-	455	mW
		LQFP48	-	364	
		LQFP32	-	357	
		TSSOP20	-	263	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge(2)	1.80	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V

Table 23. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(4)	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 24. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40°C < T_A < +85°C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 (1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	-100(1)	-	100(1)	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 26. Typical and maximum current consumption from the V_{DDA} supply(1)

Symbol	Parameter	Conditions(2)	f_{HCLK}	V_{DDA} = 3.6 V		Unit
				Typ	Max @ T_A(3)	
					85 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	175	215	µA
			48 MHz	160	192	
		HSE bypass, PLL off	8 MHz	3.9	4.9	
			8 MHz	3.7	4.6	
			1 MHz	3.9	4.1	
			1 MHz	3.3	4.4	
		HSI clock, PLL on	48 MHz	244	275	
			48 MHz	235	275	
		HSI clock, PLL off	8 MHz	85	105	
			8 MHz	77	92	

1. The gray shading is used to distinguish the values for STM32F030xC devices.
2. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash or RAM. Furthermore, when the PLL is off, I_{DDA} is independent of the frequency.
3. Data based on characterization results, not tested in production.

Table 37. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 38. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 85 °C unless otherwise specified.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = -40 to +85 °C	-	53.5	-	µs
t_{ERASE}	Page erase time(2)	T_A = -40 to +85 °C	-	30	-	ms
t_{ME}	Mass erase time	T_A = -40 to +85 °C	-	30	-	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA
V_{prog}	Programming voltage	-	2.4	-	3.6	V

1. Guaranteed by design, not tested in production.
2. Page size is 1KB for STM32F030x4/6/8 devices and 2KB for STM32F030xC devices

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 42. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-3	dBµV
			30 to 130 MHz	23	
			130 MHz to 1 GHz	17	
			EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C4(2) C3(3)	500(2) 250(3)	V

1. Data based on characterization results, not tested in production.
2. Applicable to STM32F030xC
3. Applicable to STM32F030x4, STM32F030x6, and STM32F030x8

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 45*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Figure 18. TC and TTa I/O input characteristics

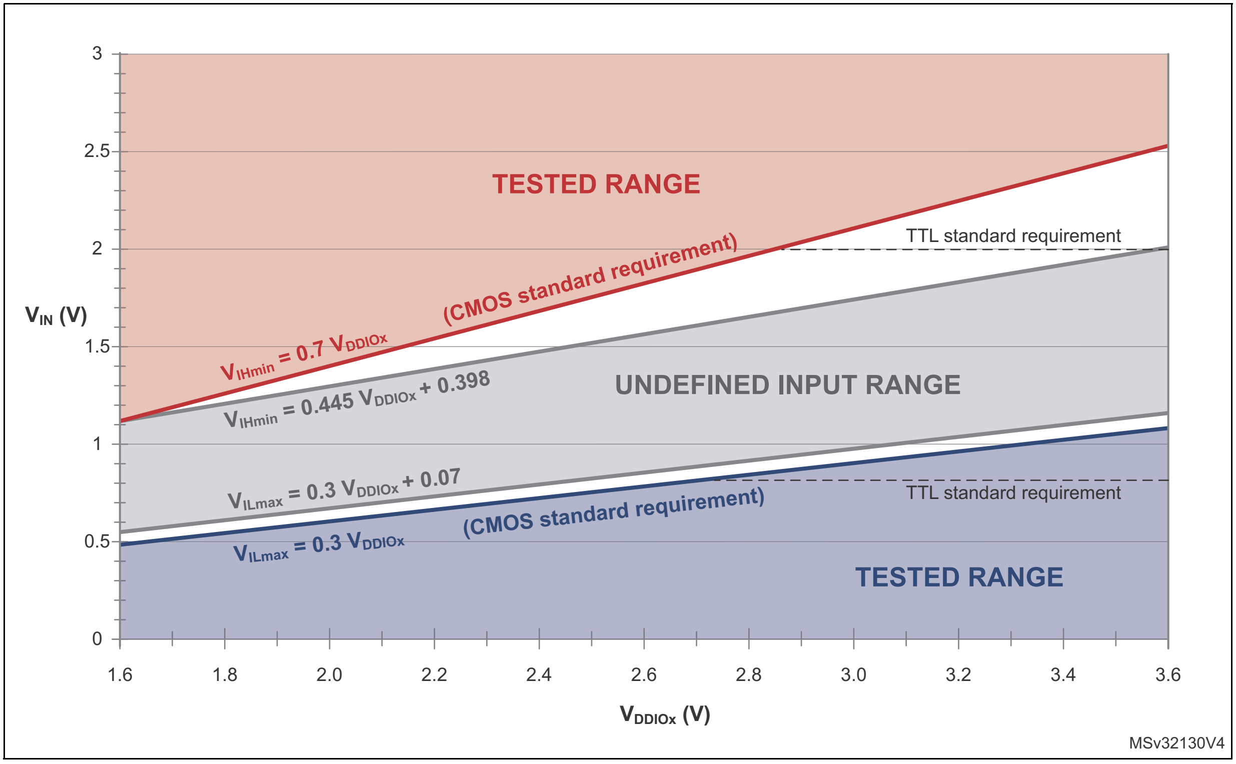


Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics

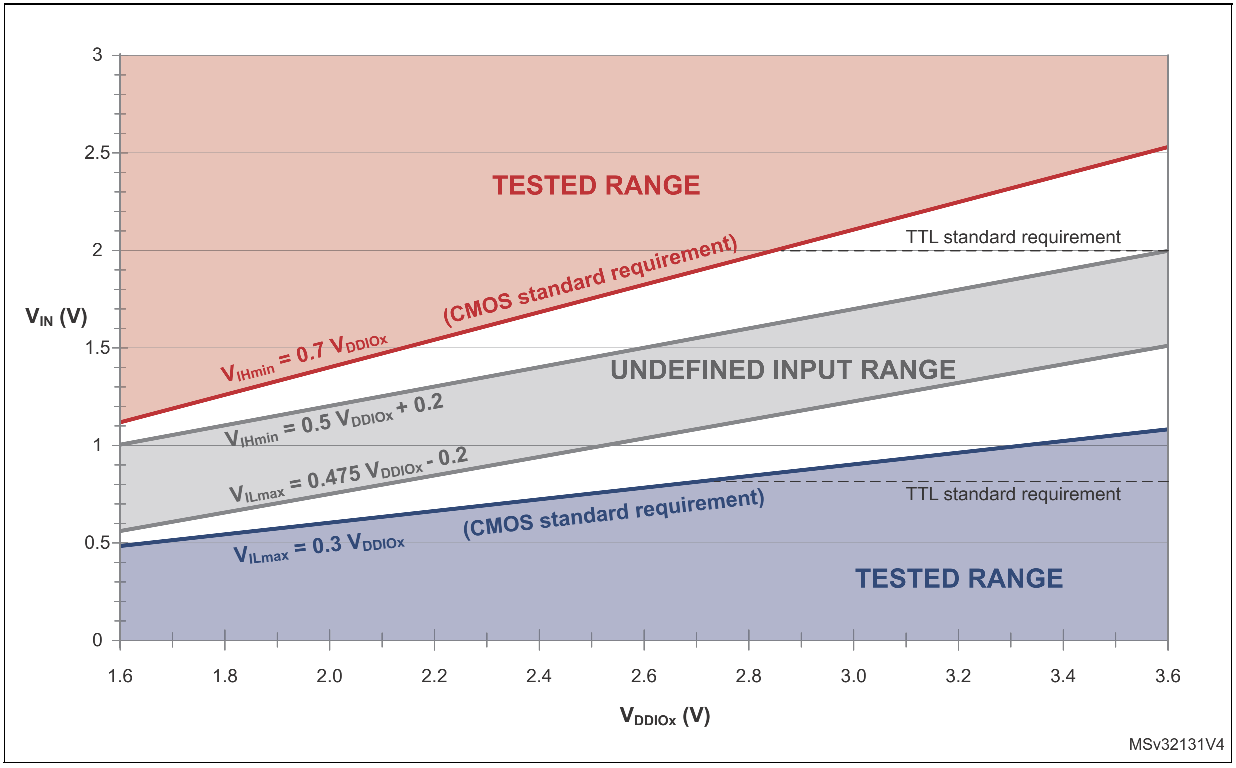
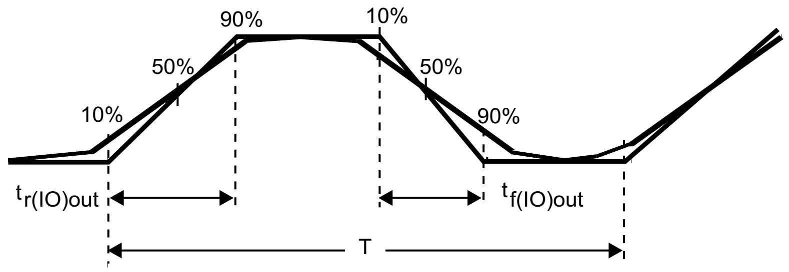


Table 48. I/O AC characteristics[(1)][(2)]

OSPEEDRy [1:0] value[(1)]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency[(3)]	C_L = 50 pF, $V_{DDIOx} \geq 2.4$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency[(3)]	C_L = 50 pF, $V_{DDIOx} \geq 2.4$ V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
11	$f_{max(IO)out}$	Maximum frequency[(3)]	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	50	MHz
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	30	
			C_L = 50 pF, 2.4 V $\leq V_{DDIOx} < 2.7$ V	-	20	
	$t_{f(IO)out}$	Output fall time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	ns
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2.4 V $\leq V_{DDIOx} < 2.7$ V	-	12	
	$t_{r(IO)out}$	Output rise time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2.4 V $\leq V_{DDIOx} < 2.7$ V	-	12	
Fm+ configuration[(4)]	$f_{max(IO)out}$	Maximum frequency[(3)]	C_L = 50 pF, $V_{DDIOx} \geq 2.4$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	12	ns
	$t_{r(IO)out}$	Output rise time		-	34	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0360 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 20*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0360 for a detailed description of Fm+ I/O configuration.

Figure 20. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq \frac{2}{3}T$ and if the duty cycle is (45-55%)
when loaded by C_L (see the table *I/O AC characteristics definition*)

MS32132V3

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

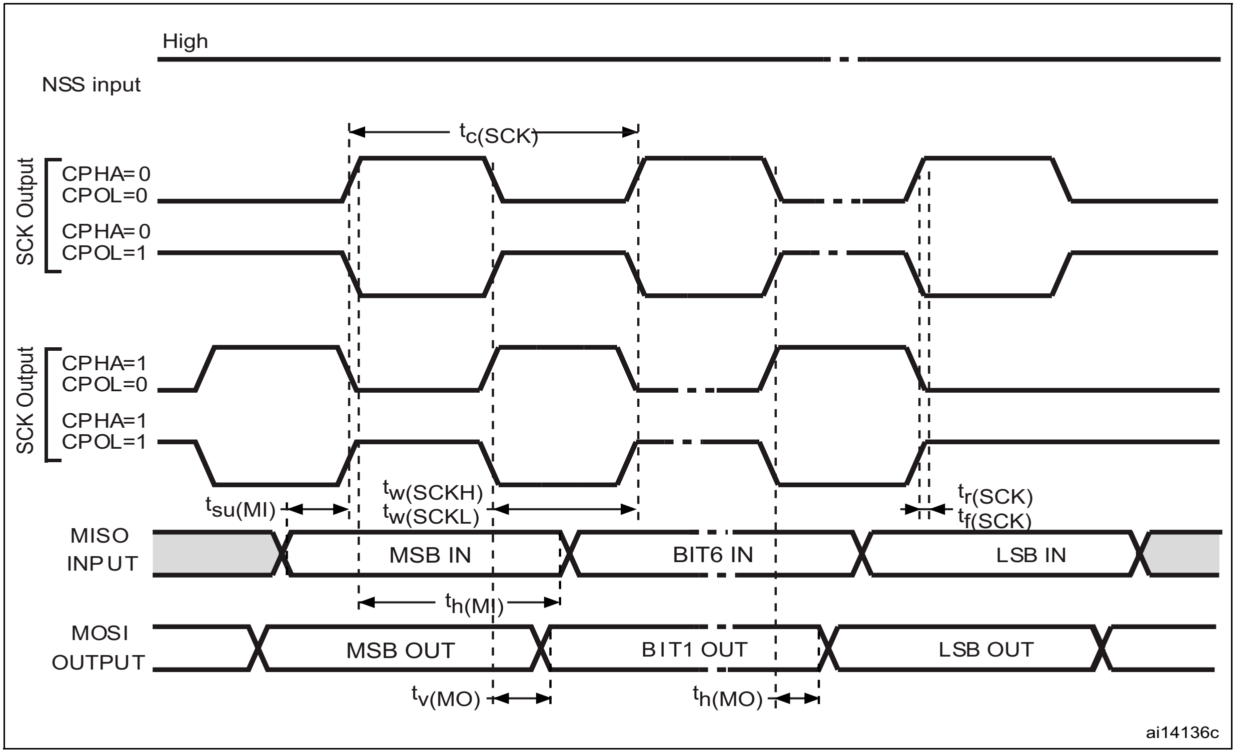
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 V_{DD}+0.07[1]	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445 V_{DD}+0.398[1]	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100[1]	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	300[3]	-	-	ns
		$2.4 < V_{DD} < 3.6$	500[3]	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 26. SPI timing diagram - master mode



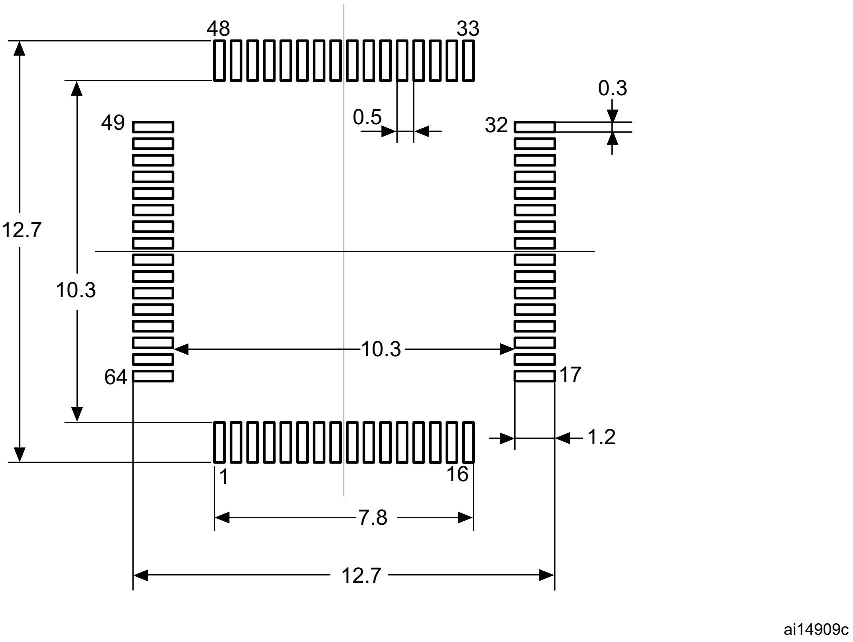
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 59. LQFP64 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 28. LQFP64 recommended footprint



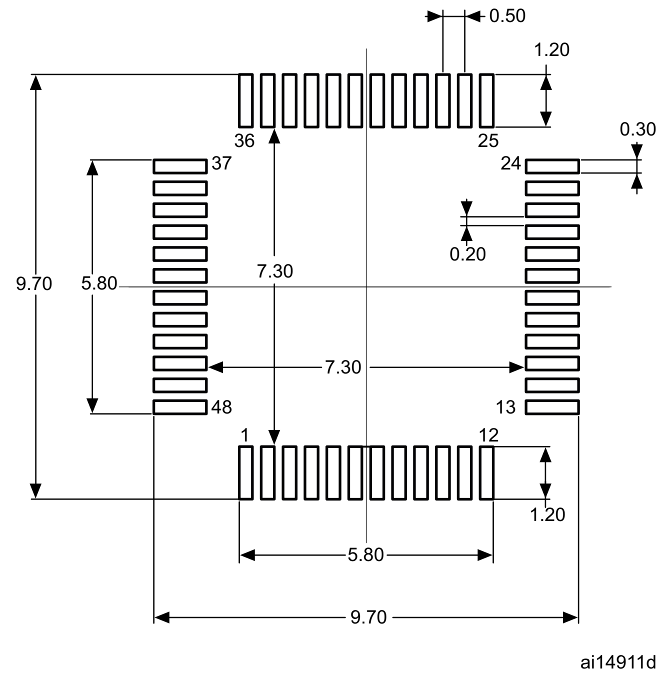
1. Dimensions are expressed in millimeters.

Table 60. LQFP48 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 31. LQFP48 recommended footprint

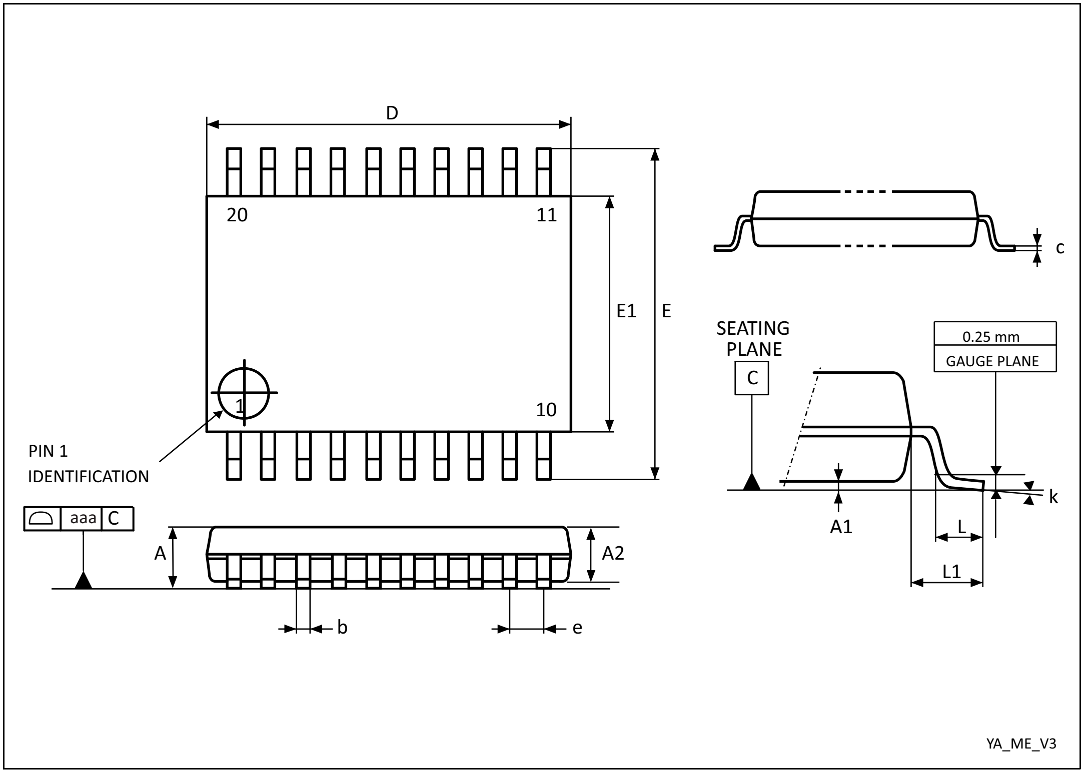


1. Dimensions are expressed in millimeters.

7.4 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch package.

Figure 36.TSSOP20 outline



1. Drawing is not to scale.

Table 62. TSSOP20 mechanical data

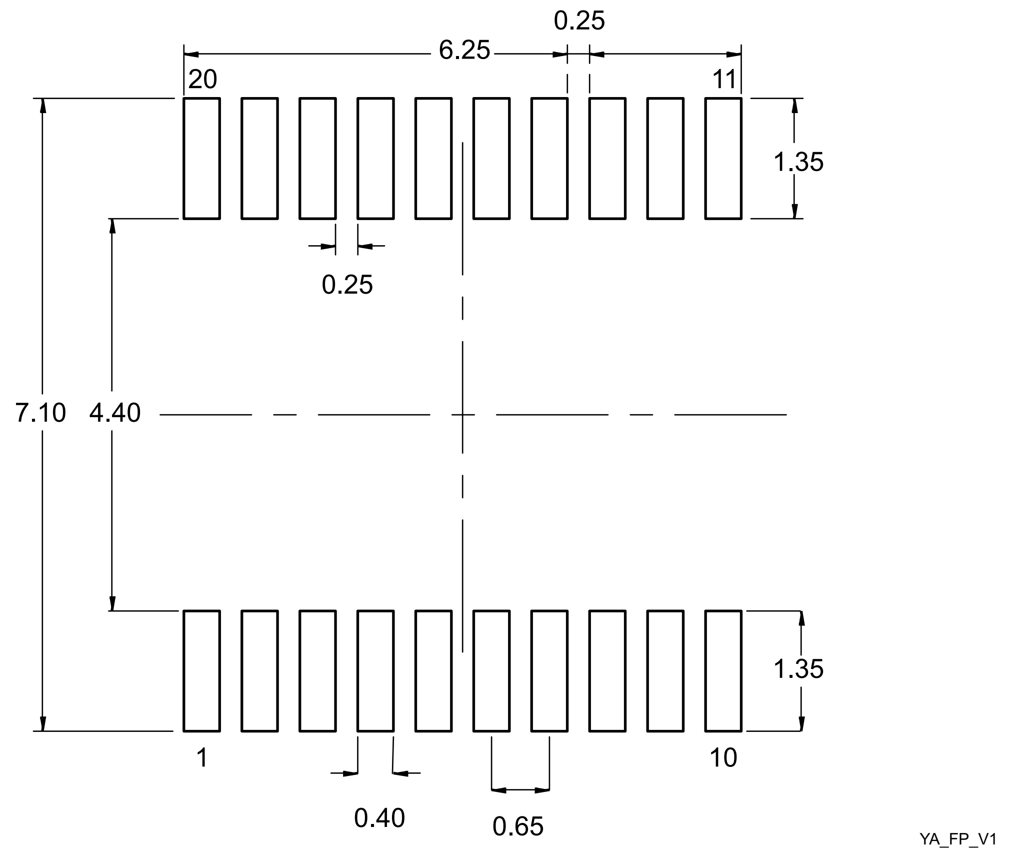
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 62. TSSOP20 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 37. TSSOP20 footprint



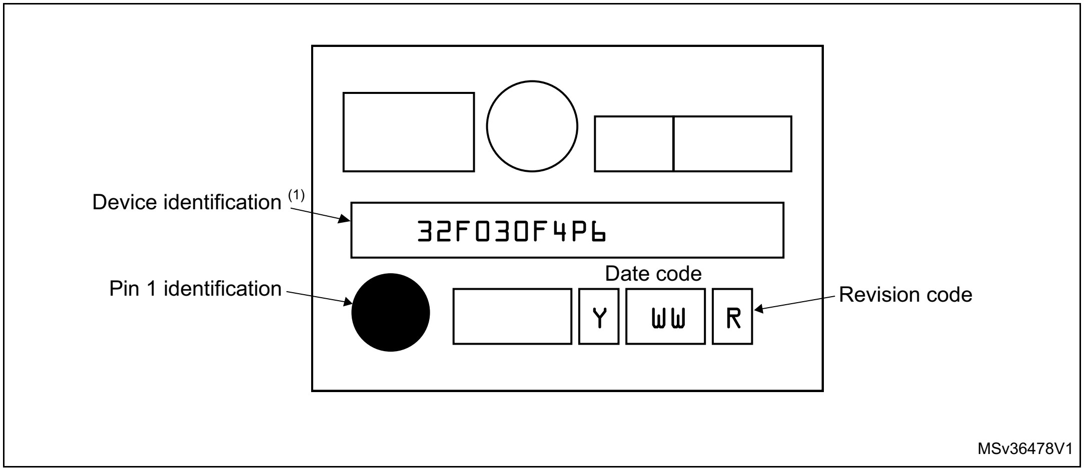
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 38. TSSOP20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 64. Ordering information scheme

Example: STM32 F 030 C 6 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

030 = STM32F030xx

Pin count

F = 20 pins
K = 32 pins
C = 48 pins
R = 64 pins

Code size

4 = 16 Kbyte of Flash memory
6 = 32 Kbyte of Flash memory
8 = 64 Kbyte of Flash memory
C = 256 Kbyte of Flash memory

Package

P = TSSOP
T = LQFP

Temperature range

6 = –40 to 85 °C

Options

xxx = programmed parts
TR = tape and reel

Table 65. Document revision history (continued)

Date	Revision	Changes
23-Jan-2017	3	– *Section 3.11.2: General-purpose timers (TIM3, TIM14..17)* - number of timers – *Table 5: Timer feature comparison* - footnotes added – *Table 7: STM32F030x4/x6/x8/xC I^2C implementation* - FM+ and footnote – *Figure 3* through *Figure 6* - darker highlight on pins – *Table 11: STM32F030x4/6/8/C pin definitions* - corrections – *Table 12: Alternate functions selected through GPIOA_AFR registers for port A* - note order – *Table 14* through *Table 16* - corrected footnotes – *Figure 9: STM32F030x4/x6/x8/xC memory map* footnote – *Figure 12: Power supply scheme* – *Table 24: Embedded internal reference voltage*: added t_{START}, changed V_{REFINT} and $t_{S\_vrefint}$ values and notes – *Table 25: Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V* footnotes – *Table 26: Typical and maximum current consumption from the V_{DDA} supply* values for STM32F030xC and footnotes – *Table 34: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* LSEDRV[1:0] values removed (see ref. manual) – *Table 50: ADC characteristics* - t_{STAB} defined relative to clock frequency; notes *3.* and *4.* added – *Section 3.14: Universal synchronous/asynchronous receiver/transmitter (USART)* - introduction and *Table 8: STM32F0x0 USART implementation* – *Figure 9: STM32F030x4/x6/x8/xC memory map* footnote – *Table 43: ESD absolute maximum ratings* - C4 or C3 class, depending on device variant; CDM values updated to match the referenced standard. (CDM standard was updated in the previous release, without duly modifying the related values.) – *Table 53: TS characteristics*: removed the min. value for t_{START} and parameter name change – *Figure 18* and *Figure 19* improved – *Section 7: Package information* name and structure *change* – *Section 8: Ordering information* renamed from Part numbering