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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f030rct6tr

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2 Description

The STM32F030x4/x6/x8/xC microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 256 Kbytes of Flash memory and up to 32 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, up to two SPIs and up to six USARTs), one 12-bit ADC, seven general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F030x4/x6/x8/xC microcontrollers operate in the -40 to +85 °C temperature range from a 2.4 to 3.6V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F030x4/x6/x8/xC microcontrollers include devices in four different packages ranging from 20 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F030x4/x6/x8/xC peripherals proposed.

These features make the STM32F030x4/x6/x8/xC microcontrollers suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

3 Functional overview

3.1 ARM®-Cortex®-M0 core with embedded Flash and SRAM

The ARM® Cortex®-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 3 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 4 to 32 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 256 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and two internal (temperature sensor, voltage reference measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

Table 12. Alternate functions selected through GPIOA_AFR registers for port A (continued)

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	SDA	-
PA13	SWDIO	IR_OUT	-	-	-	-	-
PA14	SWCLK	USART1_TX[2] USART2_TX[1][3]	-	-	-	-	-
PA15	SPI1_NSS	USART1_RX[2] USART2_RX[1][3]	-	EVENTOUT	USART4_RTS[1]	-	-

1. This feature is available on STM32F030xC devices.
2. This feature is available on STM32F030x4 and STM32F030x6 devices.
3. This feature is available on STM32F030x8 devices.

Table 13. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	USART3_CK[1]	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS[1]	-
PB2	-	-	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-	USART5_TX[1]	-
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT	-	USART5_RX[1]	TIM17_BKIN[1]
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	USART5_CK_RTS[1]	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-	USART4_CTS[1]	-

Table 19. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)[1]	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)[1]	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)[1]	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)[1]	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins[2]	80	
	Total output current sourced by sum of all I/Os and control pins[2]	-80	
$I_{INJ(PIN)}$[3]	Injected current on FT and FTf pins	-5/+0[4]	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins[5]	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)[6]	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 18: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note [2] below *Table 52: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.4	3.6	V

Table 27. Typical and maximum consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} ($V_{DD} = V_{DDA}$)	Max(1)	Unit
				3.6 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		19	48	µA
		Regulator in low-power mode, all oscillators OFF		5	32	
	Supply current in Standby mode	LSI ON and IWDG ON		2	-	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run or low-power mode, all oscillators OFF	2.9	3.5	
	Supply current in Standby mode		LSI ON and IWDG ON	3.3	-	
			LSI OFF and IWDG OFF	2.8	3.5	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run or low-power mode, all oscillators OFF	1.7	-	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	-	
			LSI OFF and IWDG OFF	1.4	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 28. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	23.3	11.5	mA
			8 MHz	4.5	3.0	
I_{DDA}	Supply current in Run mode from V_{DDA} supply		48 MHz	158	158	µA
			8 MHz	2.43	2.43	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 46: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

Table 33. HSE oscillator characteristics

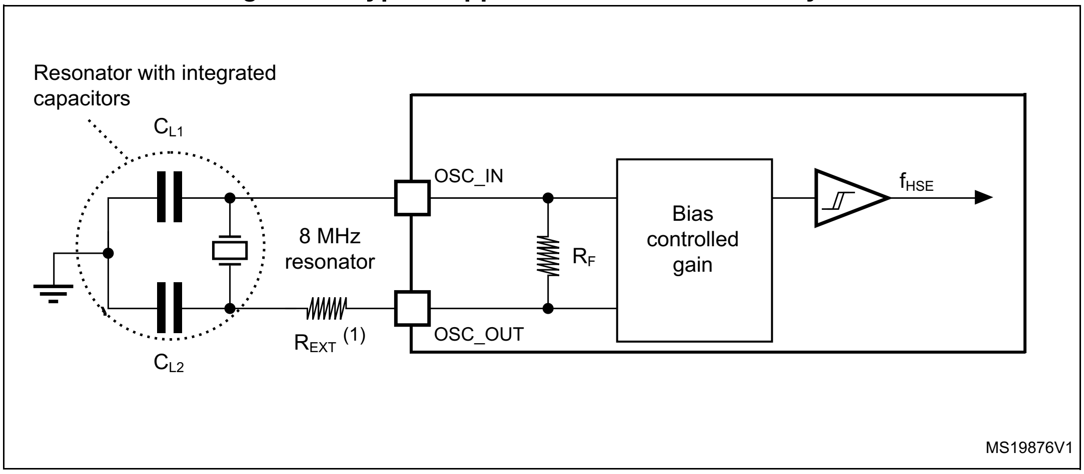
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results

6.3.8 Internal clock source characteristics

The parameters given in *Table 35* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 35. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1[2]	%
$DuCy_{HSI}$	Duty cycle	-	45[2]	-	55[2]	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = -40 to 85°C	-	±5	-	%
		T_A = 25°C	-	±1[3]	-	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	1[2]	-	2[2]	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. With user calibration.

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 36. HSI14 oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1[2]	%
$DuCy_{(HSI14)}$	Duty cycle	-	45[2]	-	55[2]	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 85 °C	-	±5	-	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1[2]	-	2[2]	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 37. LSI oscillator characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz

Table 45. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 and PF1 pins	-0	NA	mA
	Injected current on PA9, PB3, PB13, PF11 pins with induced leakage current on adjacent pins less than 50 µA	-5	NA	
	Injected current on PA11 and PA12 pins with induced leakage current on adjacent pins less than -1 mA	-5	NA	
	Injected current on all other FT and FTf pins	-5	NA	
	Injected current on PB0 and PB1 pins	-5	NA	
	Injected current on PC0 pin	-0	+5	
	Injected current on all other TTa, TC and RST pins	-5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DDIOx}+0.07$(1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DDIOx}-0.2$(1)	
		BOOT0	-	-	$0.3\ V_{DDIOx}-0.3$(1)	
		All I/Os except BOOT0 pin	-	-	$0.3\ V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DDIOx}+0.398$(1)	-	-	V
		FT and FTf I/O	$0.5\ V_{DDIOx}+0.2$(1)	-	-	
		BOOT0	$0.2\ V_{DDIOx}+0.95$(1)	-	-	
		All I/Os except BOOT0 pin	$0.7\ V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	

Table 46. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current[2]	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	±0.1	µA
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	±0.2	
		FT and FTf I/O [3] $V_{DDIOx} \leq V_{IN} \leq 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor [4]	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor[4]	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 45: I/O current injection susceptibility*.
3. To sustain a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* for standard I/Os, and in *Figure 19* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 47. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 6 mA	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OLFm+}(2)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\lvert I_{IO}\rvert$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\lvert I_{IO}\rvert$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 48*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Figure 24. SPI timing diagram - slave mode and CPHA = 0

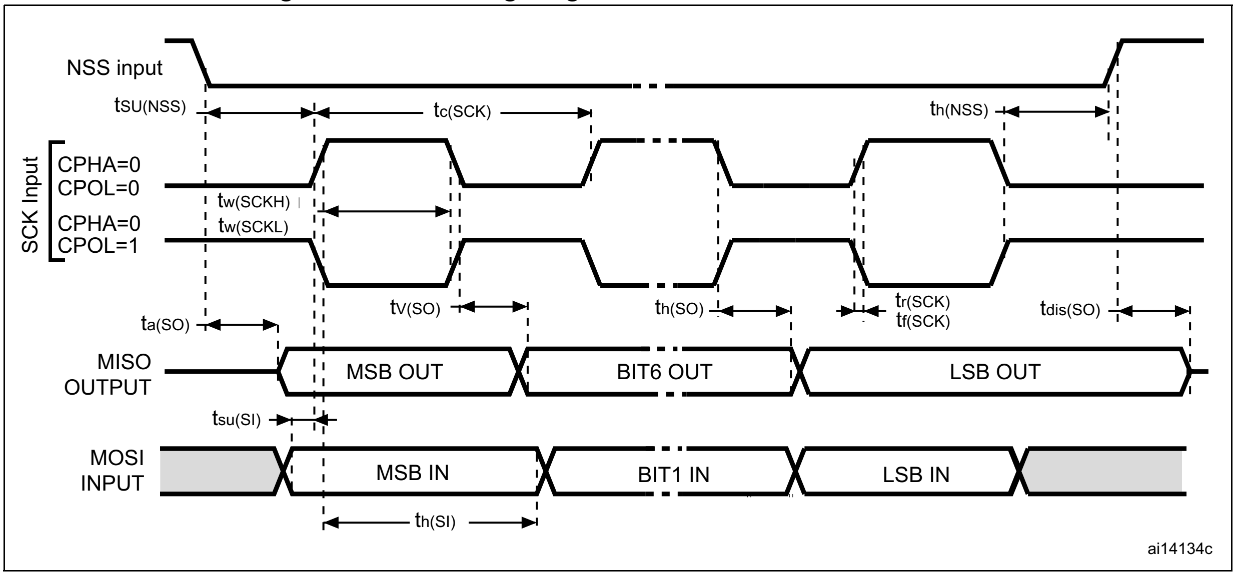
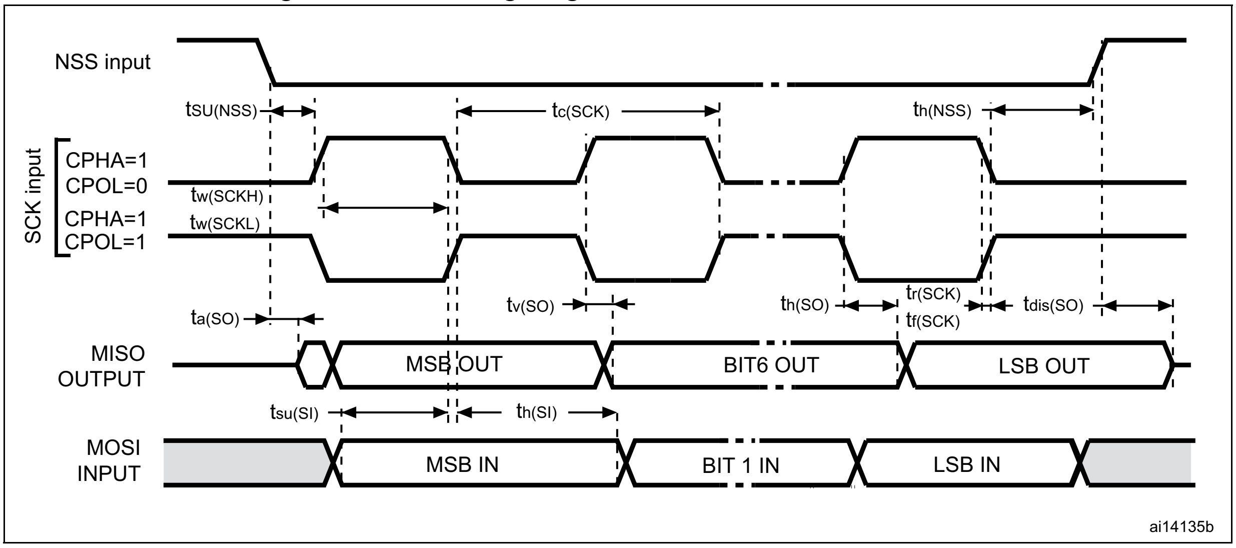


Figure 25. SPI timing diagram - slave mode and CPHA = 1

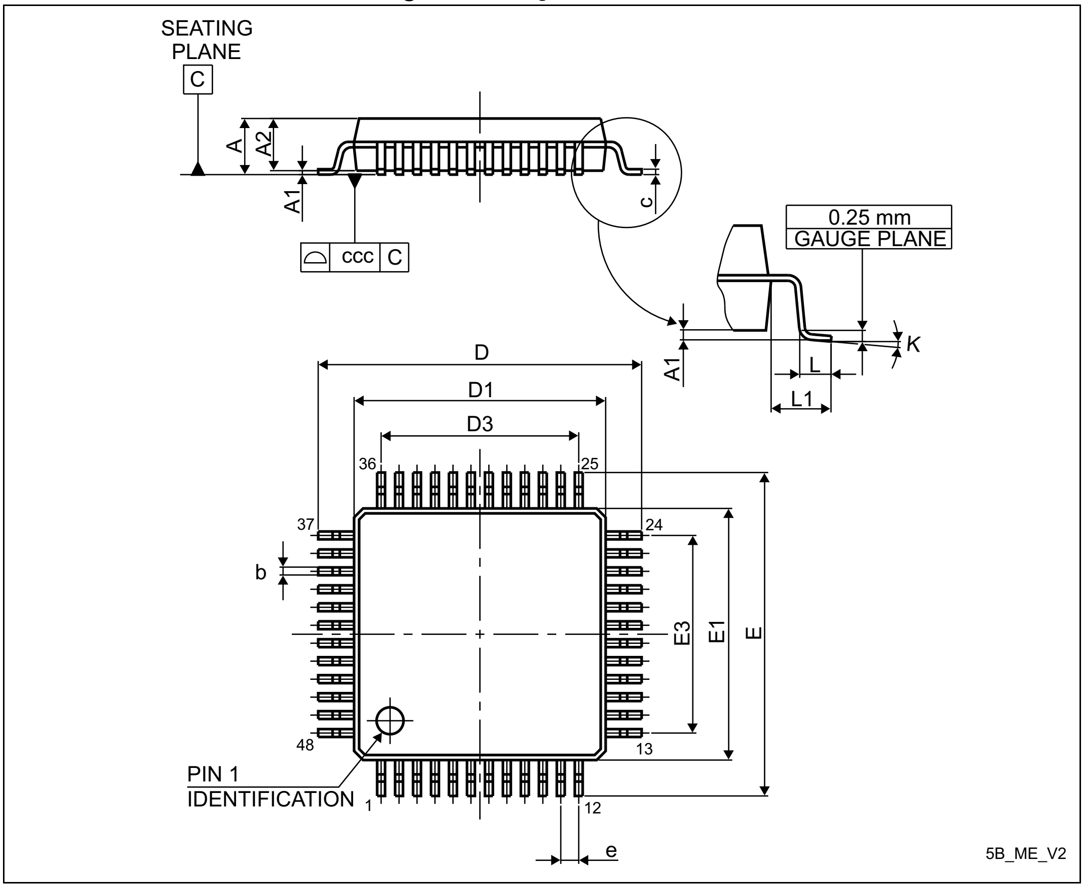


1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

7.2 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package

Figure 30. LQFP48 outline



1. Drawing is not to scale.

Table 60. LQFP48 mechanical data

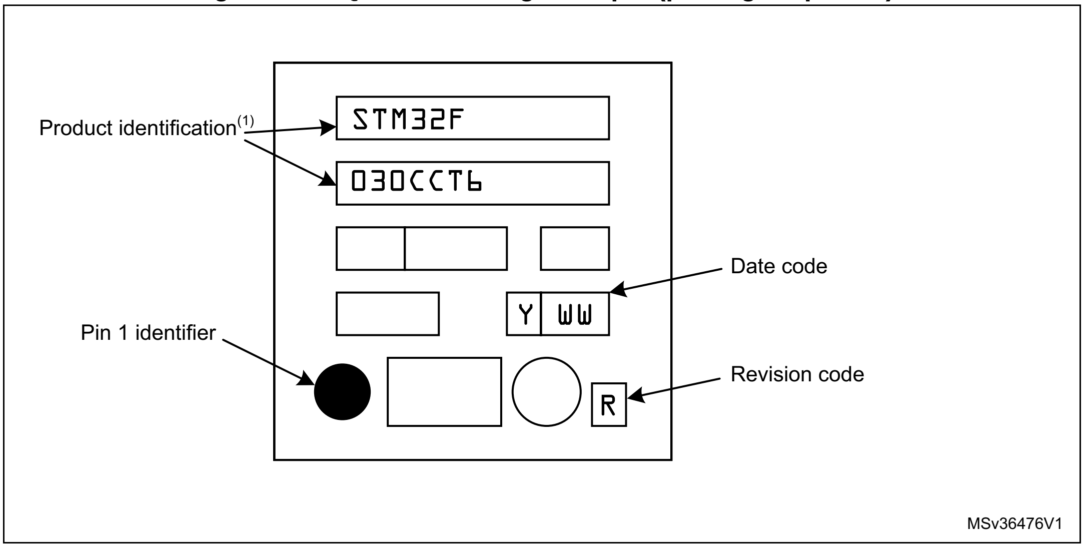
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 32. LQFP48 marking example (package top view)

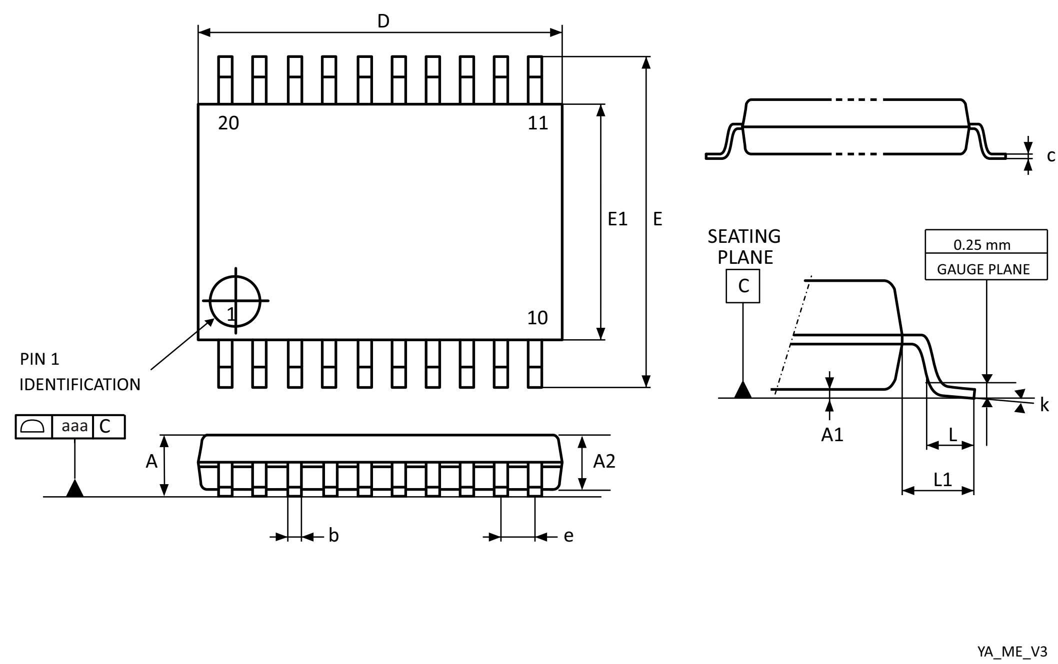


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.4 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch package.

Figure 36.TSSOP20 outline



1. Drawing is not to scale.

Table 62. TSSOP20 mechanical data

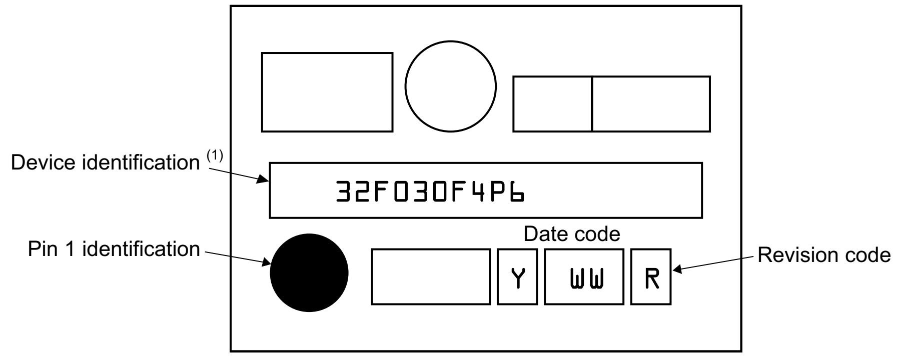
Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 38. TSSOP20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.