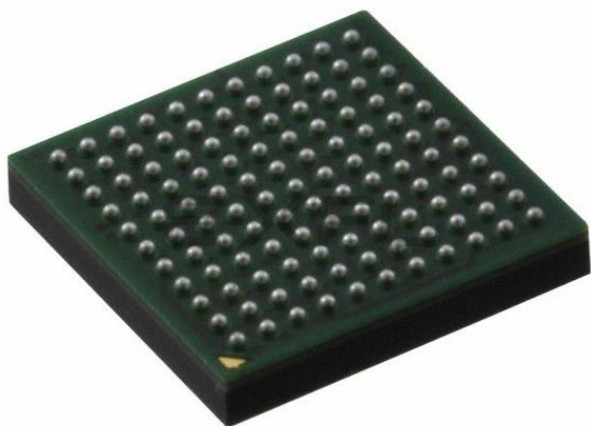




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk21dx256avmc5r

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Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

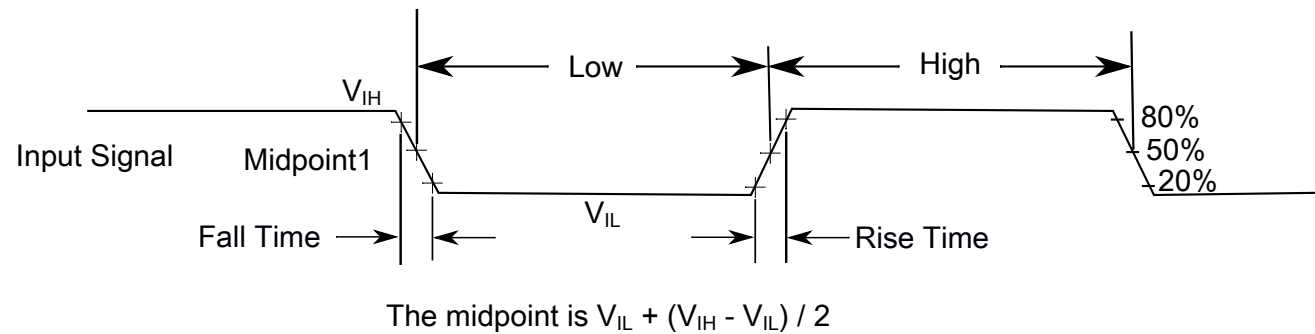


Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	I/O pin DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)	-3 —	— +3	mA	1
I_{Ccont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins - Negative current injection - Positive current injection	-25 —	— +25	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX} , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	1.71 V/(V_{DD} slew rate) ≤ 300 μs 1.71 V/(V_{DD} slew rate) > 300 μs	—	1.7 V / (V _{DD} slew rate)		
	• VLLS0 → RUN	—	150	μs	
	• VLLS1 → RUN	—	150	μs	
	• VLLS2 → RUN	—	79	μs	
	• VLLS3 → RUN	—	79	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash @ 1.8 V @ 3.0 V	— —	12.98 12.93	14 13.8	mA mA	2
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8 V @ 3.0 V @ 25°C @ 125°C	— — —	17.04 17.01 19.8	19.3 18.9 21.3	mA mA mA	3, 4
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.95	9.5	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.88	7.4	mA	5
I _{DD_STOP}	Stop mode current at 3.0 V	—	320	436	μA	

Table continues on the next page...

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	$1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

2.4.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	79	°C/W	¹ , ²
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	°C/W	¹ , ³
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	67	°C/W	¹ , ³

Table continues on the next page...

Board type	Symbol	Description	121 MAPBGA	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	29	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	4	°C/W	6

NOTES:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

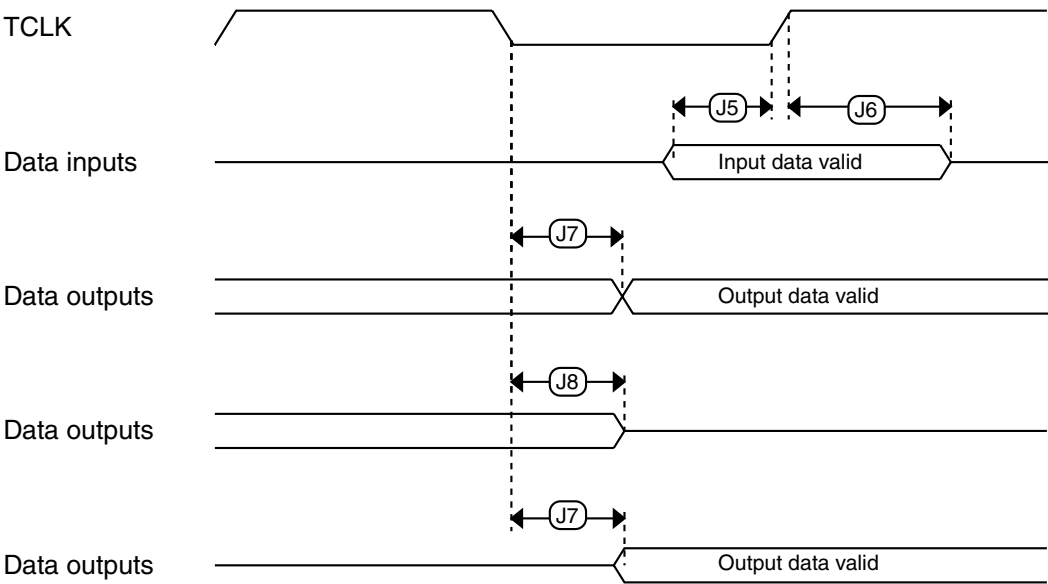


Figure 6. Boundary scan (JTAG) timing

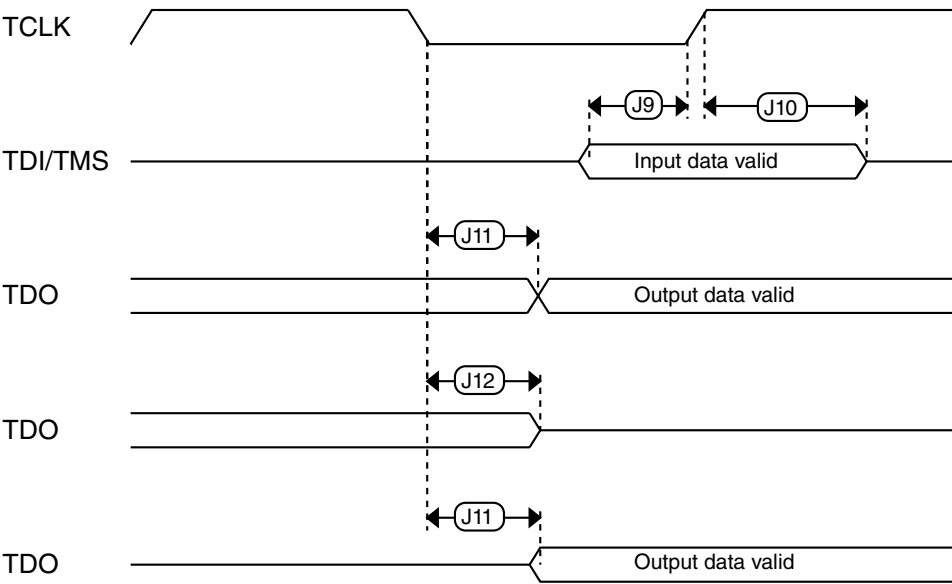


Figure 7. Test Access Port timing

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fil_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fil_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f _{fil_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fil_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fil_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3_2}	DCO output frequency	Low range (DRS=00) 732 × f _{fil_ref}	—	23.99	—	MHz	5,6
		Mid range (DRS=01) 1464 × f _{fil_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fil_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fil_ref}	—	95.98	—	MHz	
J _{cyc_fil}	FLL period jitter - f_{DCO} = 48 MHz - f_{DCO} = 98 MHz		— —	180 150	— —	ps	
t _{fil_acquire}	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f _{vco}	VCO operating frequency		48.0	—	100	MHz	
I _{pll}	PLL operating current PLL @ 96 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1200	—	μA	8
I _{pll}	PLL operating current PLL @ 48 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	700	—	μA	8
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS) - f_{vco} = 48 MHz - f_{vco} = 100 MHz		— —	120 75	— —	ps ps	9
J _{acc_pll}	PLL accumulated jitter over 1μs (RMS)		— —	1350 600	— —	ps ps	9

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	$f_{VCO} = 48 \text{ MHz}$ $f_{VCO} = 100 \text{ MHz}$					
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	5	—	μA	
		—	500	—	μA	
		—	600	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x and C_y can be provided by using either integrated capacitors or external components.

4. When low-power mode is selected, R_F is integrated and must not be attached externally.

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

Table 17. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
R_F	Internal feedback resistor	—	100	—	M Ω
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.3.2 32 kHz oscillator frequency specifications

Table 18. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 19. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpqm4}	Longword Program high-voltage time	—	7.5	18	μ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

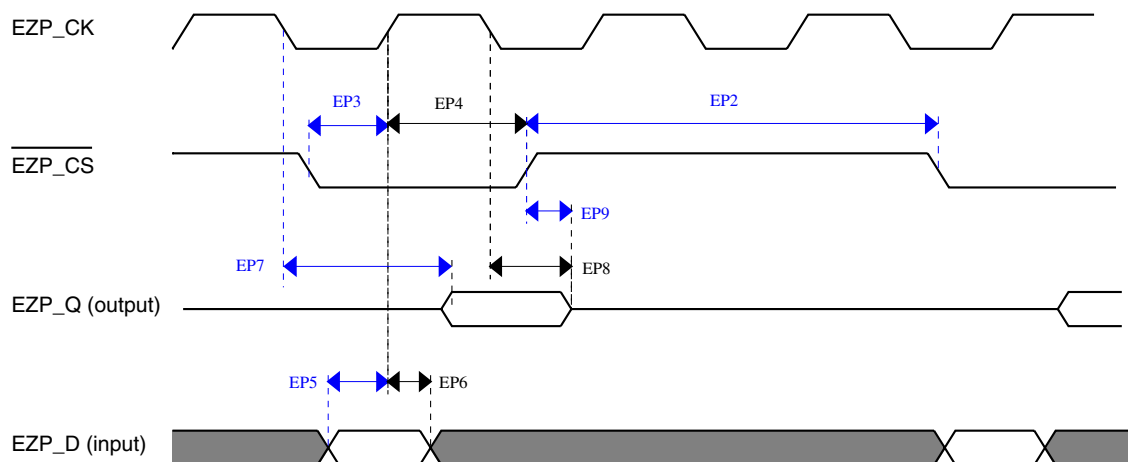


Figure 9. EzPort Timing Diagram

3.5 Security and integrity modules

3.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 24](#) and [Table 25](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 24. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	16-bit differential mode - All other modes	V_{REFL} V_{REFL}	— —	31/32 * V_{REFH} V_{REFH}	V	—
C_{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	k Ω	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes $f_{ADCK} < 4$ MHz	—	—	5	k Ω	3
f_{ADCK}	ADC conversion clock frequency	$\leq$ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	$\leq$ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8 \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

Table 30. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	1
I_{bg}	Bandgap only current	—	—	80	μA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μV	1, 2
T_{stup}	Buffer startup time	—	—	100	μs	—
V_{vdift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 31. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}C$	—

Table 32. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	—

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGFLLCLK does not meet the USB jitter specifications for certification for Host mode operation.

3.8.2 USB DCD electrical specifications

Table 33. USB0 DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 μ A)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μ A
I _{DM_SINK}	USB_DM sink current	50	100	150	μ A
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k Ω
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

3.8.3 VREG electrical specifications

Table 34. VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{REGIN}	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (V _{REGIN}) > 3.6 V	—	125	186	μ A	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μ A	
I _{DDoff}	Quiescent current — Shutdown mode - V_{REGIN} = 5.0 V and temperature=25 °C - Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μ A	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V					

Table continues on the next page...

3.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 37. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

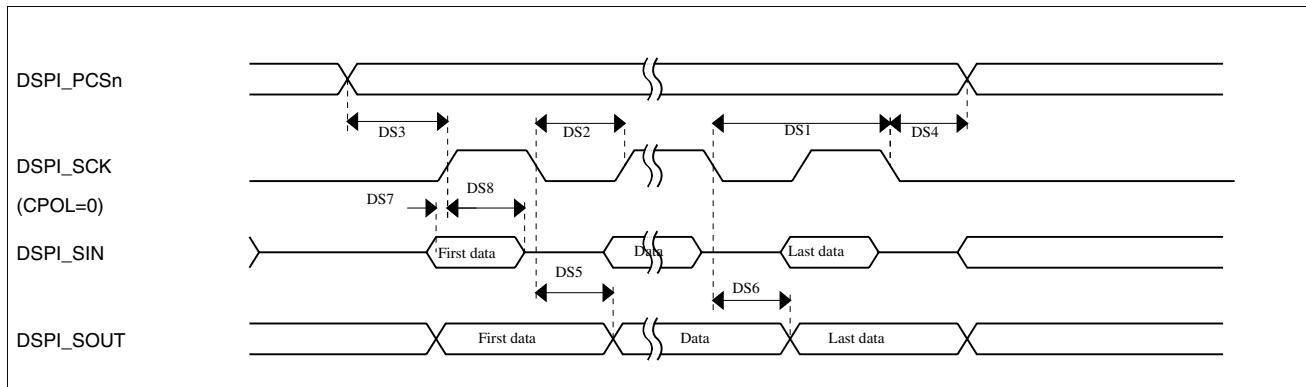


Figure 19. DSPI classic SPI timing — master mode

Table 42. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

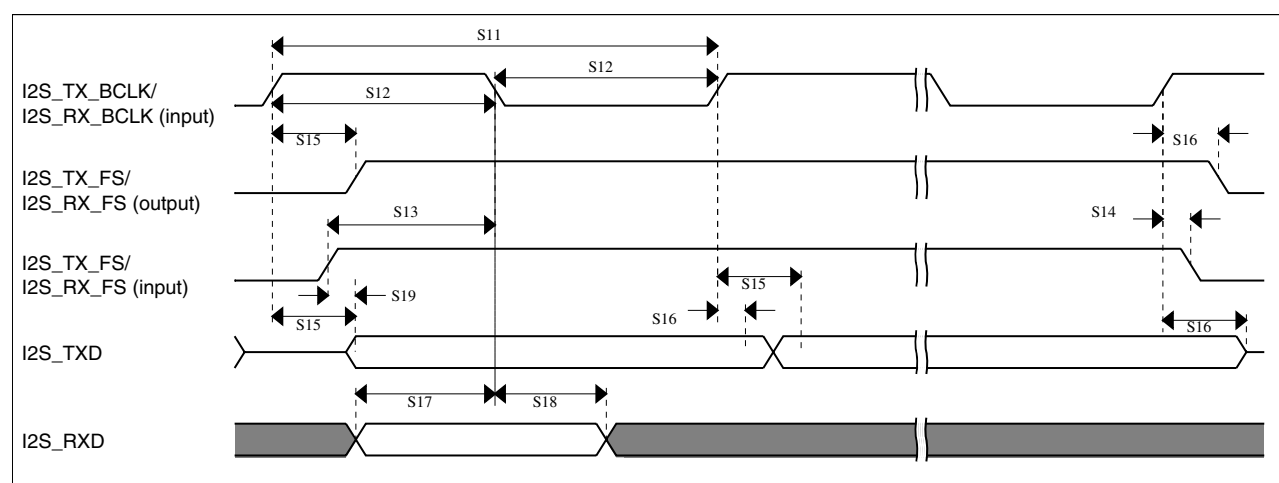


Figure 24. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

Pinout

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K6	VBAT	VBAT								
J6	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	DISABLED		PTA5	USB_CLKIN	FTM0_CH2			I2S0_TX_BCLK	JTAG_TRST_b	
K8	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
L8	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
K9	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	I2S0_TXD1	
L9	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
J10	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b/ UART0_COL_b			I2S0_RX_FS	I2S0_RXD1	
H10	DISABLED		PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
L10	VDD	VDD								
K10	VSS	VSS								
L11	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
J11	RESET_b	RESET_b								
G11	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
G10	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
G9	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
G8	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_b			FTM0_FLT0		
D10	DISABLED		PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1		
C10	DISABLED		PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2		
B11	DISABLED		PTB12	UART3_RTS_b	FTM1_CH0	FTM0_CH4		FTM1_QD_ PHA		
C11	DISABLED		PTB13	UART3_CTS_b	FTM1_CH1	FTM0_CH5		FTM1_QD_ PHB		

Pinout

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B2	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
A1	ADC0_SE22	ADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
F3	NC	NC								
H1	NC	NC								
H2	NC	NC								
J1	NC	NC								
J2	NC	NC								
J3	NC	NC								
H3	NC	NC								
K4	NC	NC								
H6	NC	NC								
J9	NC	NC								
J4	NC	NC								
H11	NC	NC								
F11	NC	NC								
E11	NC	NC								
D11	NC	NC								
E10	NC	NC								
F10	NC	NC								
F9	NC	NC								
F8	NC	NC								
E8	NC	NC								
E7	NC	NC								
F7	NC	NC								
A5	NC	NC								
B5	NC	NC								
B4	NC	NC								
A4	NC	NC								
A9	NC	NC								
B1	NC	NC								
C2	NC	NC								
C1	NC	NC								
D2	NC	NC								
D1	NC	NC								
E1	NC	NC								

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
##	Kinetis family	1# = K11/K12 2# = K21/K22
C	Speed	G = 50 MHz
F	Flash memory configuration	- G = 128 KB + Flex - H = 256 KB + Flex 9 = 512 KB
T	Temperature range (°C)	V = -40 to 105
PP	Package identifier	MC = 121 MAPBGA

This table lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK21DX128VMC5	M21GGVMC
MK21DX256VMC5	M21GHVMC
MK21DN512VMC5	M21G9VMC

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V