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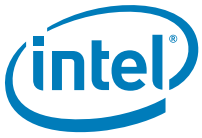
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

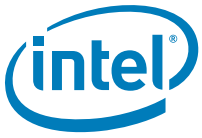
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Celeron Mobile P4500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	1.86GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	988-PGA Module
Supplier Device Package	988-PGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/advantech/96mpcm-1-86-2m9t

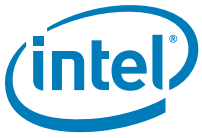


Contents



Revision History

Document Number	Revision Number	Description	Revision Date
442690	1.5	• Initial release	Feburary 2010



Revision Number Descriptions		
Revision	**Associated Life Cycle Milestone**	**Release Information**
0.5	Design Win Phase	Required Release
0.6–0.7	When Needed	Project Dependent
0.7	Simulations Complete	Required Release
0.8–0.9	When Needed	Project Dependent
1.0	First Silicon Samples	Required Release
1.1–1.4	When Needed	Project Dependent
1.5	Qualification Silicon Samples	Project Dependent
1.6–1.9	When Needed	Project Dependent
NDA - 2.0 Public - XXXXXX-001	First SKU Launch	Required Release Product Launch
2.1 and up	When Needed	Project Dependent

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- Re-issues configuration cycles that have been previously completed with the Configuration Retry status.
- PCI Express reference clock is 100-MHz differential clock buffered out of system clock generator.
- Power Management Event (PME) functions.
- Static lane numbering reversal
  - Does not support dynamic lane reversal, as defined (optional) by the *PCI Express Base Specification.*
  - PCI Express 1x16 configuration
    Normal (1x16): PEG_RX[15:0]; PEG_TX[15:0]
    Reversal (1x16): PEG_RX[0:15]; PEG_TX[0:15]
- Supports Half Swing "low-power/low-voltage" mode.
- Message Signaled Interrupt (MSI and MSI-X) messages
- PEG Lanes shared with Embedded DisplayPort* (see eDP, Section 1.3.6).
- Polarity inversion

1.3.3 Direct Media Interface (DMI)

- Compliant to Direct Media Interface second generation (DMI2).
- Four lanes in each direction.
- 2.5 GT/s point-to-point DMI interface to PCH is supported.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s when DMI x4.
- Shares 100-MHz PCI Express reference clock.
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Supports the following traffic types to or from the PCH:
  - DMI -> PCI Express Port 0 write traffic
  - DMI -> DRAM
  - DMI -> processor core (Virtual Legacy Wires (VLWs), Resetwarn, or MSIs only)
  - Processor core -> DMI
- APIC and MSI interrupt messaging support:
  - Message Signaled Interrupt (MSI and MSI-X) messages
- Downstream SMI, SCI and SERR error indication.
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters.
- DC coupling – no capacitors between the processor and the PCH.
- Polarity inversion.

Table 2. PCH Documents

Document	Document Number / Location
Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset Platform Controller Hub (PCH) – External Design Specification (EDS)	401376
Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset Platform Controller Hub (PCH) – Thermal Mechanical Specifications & Design Guidelines	407051

Table 3. Public Specifications

Document	Document Number / Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express Base Specification 2.0	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

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receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets which are used for Link management functions.

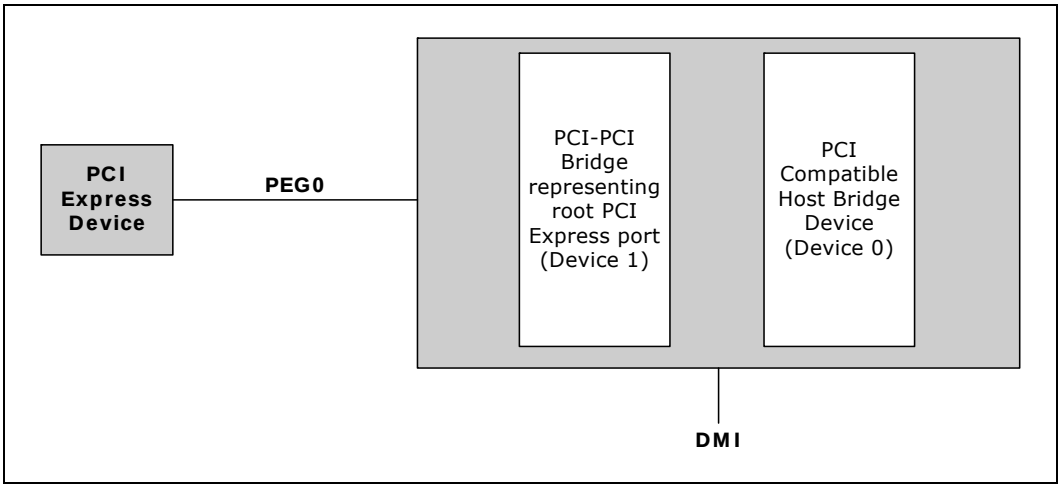
2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 6. PCI Express Related Register Structures in the Processor



PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the *Conventional PCI Specification*. PCI Express configuration space is divided into a PCI-compatible region (which consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (which consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the *PCI Express Enhanced Configuration Mechanism* section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the *PCI Express Base Specification* for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

Table 39. Processor Internal Pull Up/Pull Down

Signal Name	Pull Up/Pull Down	Rail	Value
TMS	Pull Up	VTT	44 - 55 kΩ
TRST#	Pull Up	VTT	1 - 5 kΩ
TDI_M	Pull Up	VTT	44 - 55 kΩ
PREQ#	Pull Up	VTT	44 - 55 kΩ
CFG[17:0]	Pull Up	VTT	5 - 14 kΩ

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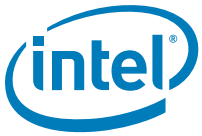


7.3.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 40 for DC specifications and to the *Calpella Platform Design Guide* for decoupling and routing guidelines.

7.4 Voltage Identification (VID)

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of the processor power supply voltages. VID pins for the processor are CMOS outputs driven by the processor VID circuitry. A dedicated graphics voltage regulator is required to deliver voltage to the integrated graphics controller. Like the processor core, the integrated graphics controller will use seven voltage identification pins, GFX_VID[6:0], to set the nominal operating voltage GFX_VID pins for the graphics core are CMOS outputs driven by the graphics core VID circuitry. Table 40 specifies the voltage level for VID[6:0] and GFX_VID[6:0]; 0 refers to a low-voltage level. For more details about VR design and how to satisfy processor power supply requirements, please refer to the *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification*

VID signals are CMOS push/pull drivers. Refer to Table 49 for the DC specifications for these signals. The VID codes will change due to temperature, frequency, and/or power mode load changes in order to minimize the power of the part. A voltage range is provided in Table 40. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 40. The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the loadline.

Note: A low-to-high or high-to-low voltage state change will result in as many VID transitions as necessary to reach the target core voltage. Transitions above the maximum or below the minimum specified VID are not permitted. One VID transition occurs in 2.5 µs.

The VR utilized must be capable of regulating its output to the value defined by the new VID values issued. DC specifications for dynamic VID transitions are included in Table 40, while AC specifications are included in Table 65. See the *Intel® MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulation Specification* for further details.

Several of the VID signals (VID[5:3]/CSC[2:0] and VID[2:0]/MSID[2:0]) serve a dual purpose and are sampled during reset. Refer to the signal description table in Chapter 6 for more information. Refer to the *[Calpella] Platform, for Arrandale, Clarksfield and Mobile Intel® 5 Series Chipset – Design Guide* and the *Intel® MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulation Specification* for additional implementation details.

7.12.3 TAP Signal Group AC Specifications

Table 64. TAP Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1, 2,3
T14: TCK Period	31.25		ns		
T15: TDI, TMS Setup Time	8		ns	23	
T16: TDI, TMS Hold Time	5		ns	23	
T17: TDO Clock to Output Delay	0.5	7	ns	23	
T18: TRST# Assert Time	2		T_{TCK}	24	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. It is recommended that TMS be asserted while TRST# is being deasserted.

7.12.4 VID Signal Group AC Specifications

Table 65. VID Signal Group AC Specifications

T # Parameter	Min	Max	Unit	Figure	Notes[1, 2]
T19: VID Step Time	2.5	-	µs	27	
T20: VID Down Transition to Valid V_{CC} (min)	-	0	µs	26, 27	
T21: VID Up Transition to Valid V_{CC} (min)	-	15	µs	26, 27	
T22: VID Down Transition to Valid V_{CC} (max)	-	15	µs	26, 27	
T23: VID Up Transition to Valid V_{CC} (max)	-	0	µs	26, 27	

NOTES:
1. See the voltage regulator design guidelines for additional information.
2. Platform support for VID transitions is required for the processor to operate within specifications.

7.13 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 63 through Table 65.

Note: For Figure 17 through Figure 27, the following apply:

1. All common clock AC timings signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK, BCLK# at rising edge of BCLK.
2. All source synchronous AC timings are referenced to their associated strobe (address or data). Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe.
3. All AC timings for the TAP signals are referenced to the TCK at 0.5 * V_{TT} at the processor lands. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.5 * V_{TT} at the processor die (pads).
4. All CMOS signal timings are referenced at 0.5 * V_{TT} at the processor pins.

Figure 22. PCI Express Receiver Eye Margins

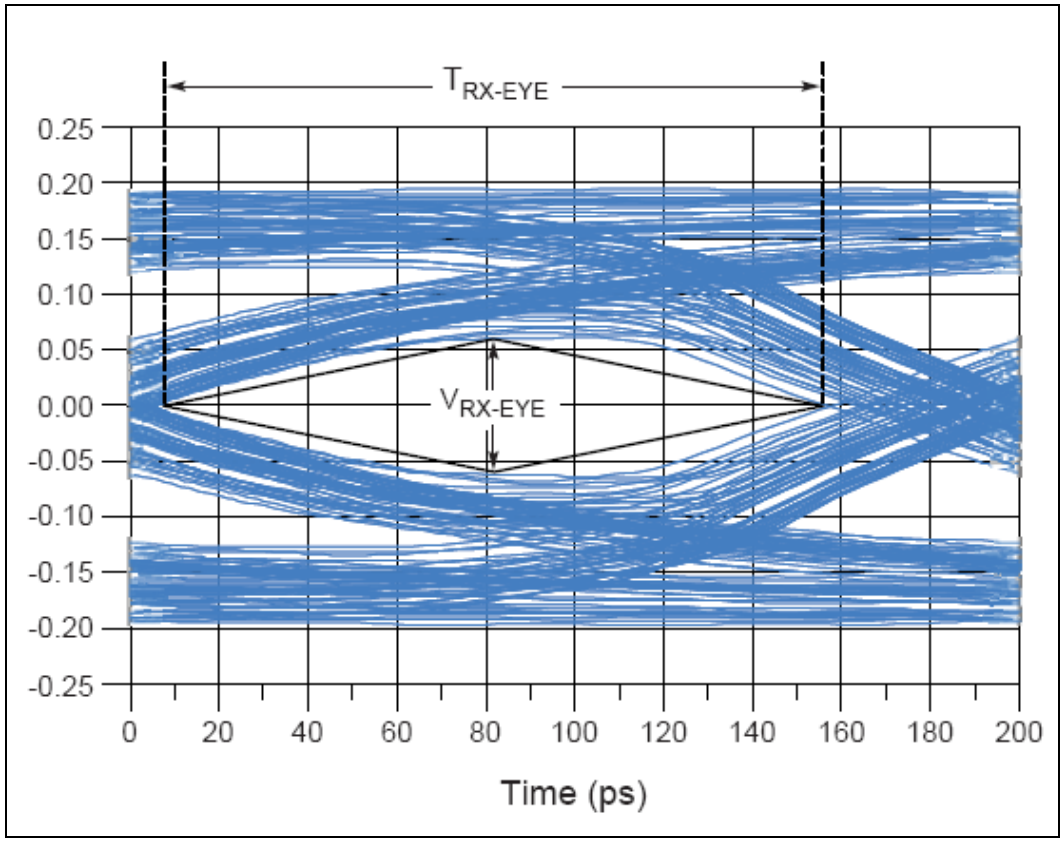
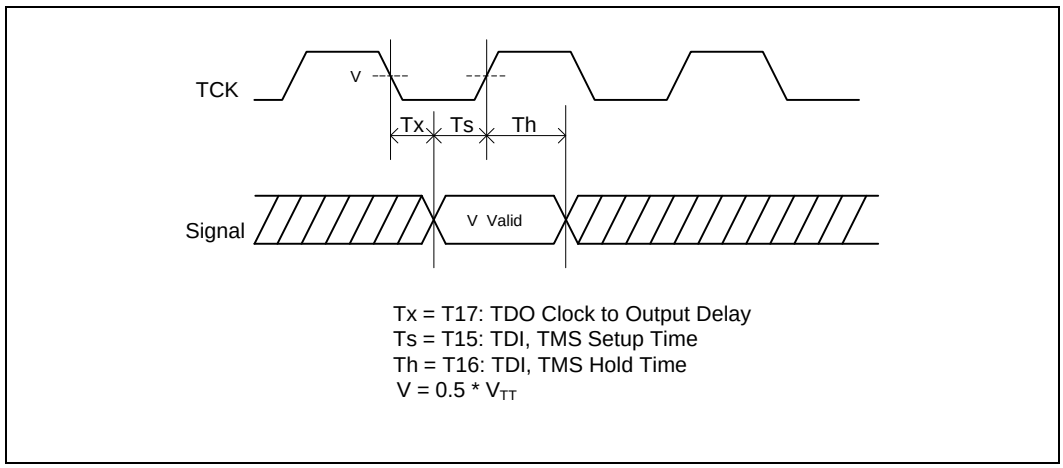


Figure 23. TAP Valid Delay Timing Waveform



NOTE: Refer to Table 49 for TAP Signal Group DC specifications and Table 64 for TAP Signal Group AC specifications.

7.15.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 67. Processor Overshoot/Undershoot Specifications

Signal Group	Maximum Overshoot	Overshoot Duration	Minimum Undershoot	Undershoot Duration	Notes
DDR3	1.2 * V_{DDQ}	0.5 * T_{CH}	-0.2 * V_{DDQ}	0.5 * T_{CH}	1,2
Control Sideband, Graphics and TAP Signals groups	1.2 * V_{TT}	50 ns	-0.2 * V_{TT}	50 ns	1,2
PCIe and eDP	1.2 * V_{TT}	0.25 UI	-0.2 * V_{TT}	0.25 UI	

NOTES:
1. These specifications are measured at the processor pin.
2. Refer to Figure 29 for description of allowable Overshoot/Undershoot magnitude and duration.

Figure 29. Maximum Acceptable Overshoot/Undershoot Waveform

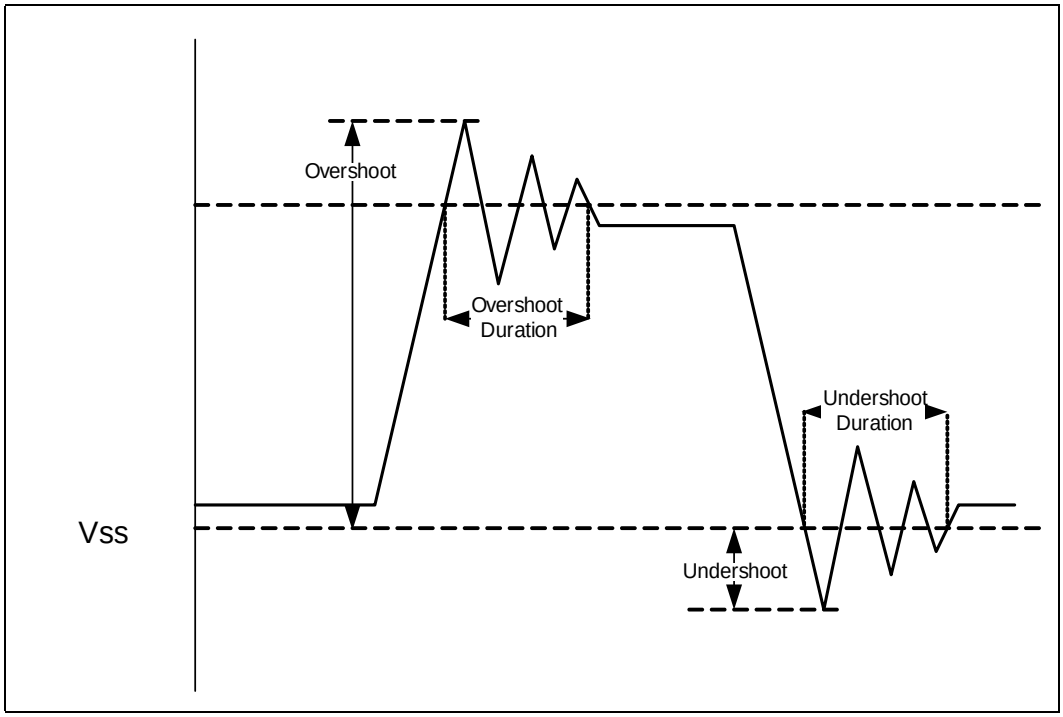


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Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
PEG_TX#[2]	M33	PCIe	O
PEG_TX#[3]	M30	PCIe	O
PEG_TX#[4]	L31	PCIe	O
PEG_TX#[5]	K32	PCIe	O
PEG_TX#[6]	M29	PCIe	O
PEG_TX#[7]	J31	PCIe	O
PEG_TX#[8]	K29	PCIe	O
PEG_TX#[9]	H30	PCIe	O
PEG_TX#[10]	H29	PCIe	O
PEG_TX#[11]	F29	PCIe	O
PEG_TX#[12]	E28	PCIe	O
PEG_TX#[13]	D29	PCIe	O
PEG_TX#[14]	D27	PCIe	O
PEG_TX#[15]	C26	PCIe	O
PM_EXT_TS#[0]	AN15	CMOS	I
PM_EXT_TS#[1]	AP15	CMOS	I
PM_SYNC	AL15	CMOS	I
PRDY#	AT28	Async GTL	O
PREQ#	AP27	Async GTL	I
PROC_DPRSLPVR	AM34	CMOS	O
PROCHOT#	AN26	Async GTL	I/O
PSI#	AN33	Async CMOS	O
RESET_OBS#	AP26	Async CMOS	O
RSTIN#	AL14	CMOS	I
RSVD	A19		
RSVD	A20		
RSVD	AB9		
RSVD	AC9		
RSVD	AG9		
RSVD	AH15		
RSVD	AH25		
RSVD	AJ15		
RSVD	AJ26		

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD	AJ27		
RSVD	AJ33		
RSVD	AL22		
RSVD	AL24		
RSVD	AL25		
RSVD	AL27		
RSVD	AL28		
RSVD	AL29		
RSVD	AP25		
RSVD	AP30		
RSVD	AP32		
RSVD	AP33		
RSVD	AR32		
RSVD	AR33		
RSVD	AT31		
RSVD	AT32		
RSVD	B19		
RSVD	B20		
RSVD	C15		
RSVD	D15		
RSVD	E30		
RSVD	E31		
RSVD	G17		
RSVD	G25		
RSVD	H17		
RSVD	J17		
RSVD	J28		
RSVD	J29		
RSVD	L28		
RSVD	M27		
RSVD	T9		
RSVD	U9		
RSVD_NCTF	A3		
RSVD_NCTF	A33		
RSVD_NCTF	A34		
RSVD_NCTF	AP1		

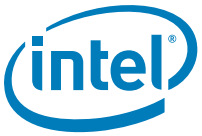

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD_NCTF	AP35		
RSVD_NCTF	AR1		
RSVD_NCTF	AR2		
RSVD_NCTF	AR35		
RSVD_NCTF	AT3		
RSVD_NCTF	AT33		
RSVD_NCTF	AT34		
RSVD_NCTF	B35		
RSVD_NCTF	C1		
RSVD_NCTF	C35		
RSVD_TP	AA1		
RSVD_TP	AA2		
RSVD_TP	AA4		
RSVD_TP	AA5		
RSVD_TP	AD2		
RSVD_TP	AD3		
RSVD_TP	AD5		
RSVD_TP	AD7		
RSVD_TP	AD9		
RSVD_TP	AE3		
RSVD_TP	AE5		
RSVD_TP	AG7		
RSVD_TP	AJ12		
RSVD_TP	AJ13		
RSVD_TP	AK26		
RSVD_TP	AL26		
RSVD_TP	AT2		
RSVD_TP	E15		
RSVD_TP	F15		
RSVD_TP	H16		
RSVD_TP	N2		
RSVD_TP	N3		
RSVD_TP	R8		
RSVD_TP	R9		
RSVD_TP	V4		
RSVD_TP	V5		

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD_TP	W2		
RSVD_TP	W3		
SA_BS[0]	AC3	DDR3	O
SA_BS[1]	AB2	DDR3	O
SA_BS[2]	U7	DDR3	O
SA_CAS#	AE1	DDR3	O
SA_CK[0]	AA6	DDR3	O
SA_CK[1]	Y6	DDR3	O
SA_CK#[0]	AA7	DDR3	O
SA_CK#[1]	Y5	DDR3	O
SA_CKE[0]	P7	DDR3	O
SA_CKE[1]	P6	DDR3	O
SA_CS#[0]	AE2	DDR3	O
SA_CS#[1]	AE8	DDR3	O
SA_DM[0]	B9	DDR3	O
SA_DM[1]	D7	DDR3	O
SA_DM[2]	H7	DDR3	O
SA_DM[3]	M7	DDR3	O
SA_DM[4]	AG6	DDR3	O
SA_DM[5]	AM7	DDR3	O
SA_DM[6]	AN10	DDR3	O
SA_DM[7]	AN13	DDR3	O
SA_DQ[0]	A10	DDR3	I/O
SA_DQ[1]	C10	DDR3	I/O
SA_DQ[2]	C7	DDR3	I/O
SA_DQ[3]	A7	DDR3	I/O
SA_DQ[4]	B10	DDR3	I/O
SA_DQ[5]	D10	DDR3	I/O
SA_DQ[6]	E10	DDR3	I/O
SA_DQ[7]	A8	DDR3	I/O
SA_DQ[8]	D8	DDR3	I/O
SA_DQ[9]	F10	DDR3	I/O
SA_DQ[10]	E6	DDR3	I/O
SA_DQ[11]	F7	DDR3	I/O
SA_DQ[12]	E9	DDR3	I/O
SA_DQ[13]	B7	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_DQ[14]	E7	DDR3	I/O
SA_DQ[15]	C6	DDR3	I/O
SA_DQ[16]	H10	DDR3	I/O
SA_DQ[17]	G8	DDR3	I/O
SA_DQ[18]	K7	DDR3	I/O
SA_DQ[19]	J8	DDR3	I/O
SA_DQ[20]	G7	DDR3	I/O
SA_DQ[21]	G10	DDR3	I/O
SA_DQ[22]	J7	DDR3	I/O
SA_DQ[23]	J10	DDR3	I/O
SA_DQ[24]	L7	DDR3	I/O
SA_DQ[25]	M6	DDR3	I/O
SA_DQ[26]	M8	DDR3	I/O
SA_DQ[27]	L9	DDR3	I/O
SA_DQ[28]	L6	DDR3	I/O
SA_DQ[29]	K8	DDR3	I/O
SA_DQ[30]	N8	DDR3	I/O
SA_DQ[31]	P9	DDR3	I/O
SA_DQ[32]	AH5	DDR3	I/O
SA_DQ[33]	AF5	DDR3	I/O
SA_DQ[34]	AK6	DDR3	I/O
SA_DQ[35]	AK7	DDR3	I/O
SA_DQ[36]	AF6	DDR3	I/O
SA_DQ[37]	AG5	DDR3	I/O
SA_DQ[38]	AJ7	DDR3	I/O
SA_DQ[39]	AJ6	DDR3	I/O
SA_DQ[40]	AJ10	DDR3	I/O
SA_DQ[41]	AJ9	DDR3	I/O
SA_DQ[42]	AL10	DDR3	I/O
SA_DQ[43]	AK12	DDR3	I/O
SA_DQ[44]	AK8	DDR3	I/O
SA_DQ[45]	AL7	DDR3	I/O
SA_DQ[46]	AK11	DDR3	I/O
SA_DQ[47]	AL8	DDR3	I/O
SA_DQ[48]	AN8	DDR3	I/O
SA_DQ[49]	AM10	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_DQ[50]	AR11	DDR3	I/O
SA_DQ[51]	AL11	DDR3	I/O
SA_DQ[52]	AM9	DDR3	I/O
SA_DQ[53]	AN9	DDR3	I/O
SA_DQ[54]	AT11	DDR3	I/O
SA_DQ[55]	AP12	DDR3	I/O
SA_DQ[56]	AM12	DDR3	I/O
SA_DQ[57]	AN12	DDR3	I/O
SA_DQ[58]	AM13	DDR3	I/O
SA_DQ[59]	AT14	DDR3	I/O
SA_DQ[60]	AT12	DDR3	I/O
SA_DQ[61]	AL13	DDR3	I/O
SA_DQ[62]	AR14	DDR3	I/O
SA_DQ[63]	AP14	DDR3	I/O
SA_DQS[0]	C8	DDR3	I/O
SA_DQS[1]	F9	DDR3	I/O
SA_DQS[2]	H9	DDR3	I/O
SA_DQS[3]	M9	DDR3	I/O
SA_DQS[4]	AH8	DDR3	I/O
SA_DQS[5]	AK10	DDR3	I/O
SA_DQS[6]	AN11	DDR3	I/O
SA_DQS[7]	AR13	DDR3	I/O
SA_DQS#[0]	C9	DDR3	I/O
SA_DQS#[1]	F8	DDR3	I/O
SA_DQS#[2]	J9	DDR3	I/O
SA_DQS#[3]	N9	DDR3	I/O
SA_DQS#[4]	AH7	DDR3	I/O
SA_DQS#[5]	AK9	DDR3	I/O
SA_DQS#[6]	AP11	DDR3	I/O
SA_DQS#[7]	AT13	DDR3	I/O
SA_MA[0]	Y3	DDR3	O
SA_MA[1]	W1	DDR3	O
SA_MA[2]	AA8	DDR3	O
SA_MA[3]	AA3	DDR3	O
SA_MA[4]	V1	DDR3	O
SA_MA[5]	AA9	DDR3	O

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
P31	VCC	REF	
P32	VCC	REF	
P33	VCC	REF	
P34	VCC	REF	
P35	VCC	REF	
R1	SB_MA[4]	DDR3	O
R2	SB_MA[6]	DDR3	O
R3	SB_MA[12]	DDR3	O
R4	SB_MA[8]	DDR3	O
R5	SB_MA[9]	DDR3	O
R6	SB_MA[7]	DDR3	O
R7	SB_BS[2]	DDR3	O
R8	RSVD_TP		
R9	RSVD_TP		
R10	VSS	GND	
R26	VCC	REF	
R27	VCC	REF	
R28	VCC	REF	
R29	VCC	REF	
R30	VCC	REF	
R31	VCC	REF	
R32	VCC	REF	
R33	VCC	REF	
R34	VCC	REF	
R35	VCC	REF	
T1	SA_MA[7]	DDR3	O
T2	SA_MA[11]	DDR3	O
T3	SA_MA[14]	DDR3	O
T4	VDDQ	REF	
T5	SB_MA[2]	DDR3	O
T6	VSS	GND	
T7	VDDQ	REF	
T8	SB_MA[5]	DDR3	O
T9	RSVD		
T10	VTT0	REF	
T26	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
T27	VSS	GND	
T28	VSS	GND	
T29	VSS	GND	
T30	VSS	GND	
T31	VSS	GND	
T32	VSS	GND	
T33	VSS	GND	
T34	VSS	GND	
T35	VSS	GND	
U1	VDDQ	REF	
U2	VSS	GND	
U3	SA_MA[12]	DDR3	O
U4	VSS	GND	
U5	SB_MA[0]	DDR3	O
U6	SA_MA[9]	DDR3	O
U7	SA_BS[2]	DDR3	O
U8	VSS	GND	
U9	RSVD		
U10	VTT0	REF	
U26	VCC	REF	
U27	VCC	REF	
U28	VCC	REF	
U29	VCC	REF	
U30	VCC	REF	
U31	VCC	REF	
U32	VCC	REF	
U33	VCC	REF	
U34	VCC	REF	
U35	VCC	REF	
V1	SA_MA[4]	DDR3	O
V2	SB_MA[1]	DDR3	O
V3	SB_MA[3]	DDR3	O
V4	RSVD_TP		
V5	RSVD_TP		
V6	SB_CK#[1]	DDR3	O
V7	SB_CK[1]	DDR3	O

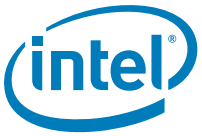

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VAXG	AF17	REF	
VAXG	AF19	REF	
VAXG	AF21	REF	
VAXG	AF23	REF	
VAXG	AF24	REF	
VAXG	AF26	REF	
VAXG	AF28	REF	
VAXG	AH12	REF	
VAXG	AH14	REF	
VAXG	AJ10	REF	
VAXG	AK12	REF	
VAXG	AK14	REF	
VAXG	AL19	REF	
VAXG	AL21	REF	
VAXG	AL23	REF	
VAXG	AL24	REF	
VAXG	AL26	REF	
VAXG	AL28	REF	
VAXG	AL30	REF	
VAXG	AL32	REF	
VAXG	AN19	REF	
VAXG	AN21	REF	
VAXG	AN23	REF	
VAXG	AN24	REF	
VAXG	AN26	REF	
VAXG	AN28	REF	
VAXG	AN30	REF	
VAXG	AN32	REF	
VAXG_SENSE	AF12	Analog	O
VCAP0	AK50	PWR	
VCAP0	AK53	PWR	
VCAP0	AK57	PWR	
VCAP0	AL50	PWR	
VCAP0	AL53	PWR	
VCAP0	AL57	PWR	
VCAP0	AN50	PWR	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCAP0	AN53	PWR	
VCAP0	AN57	PWR	
VCAP0	AR48	PWR	
VCAP0	AR51	PWR	
VCAP0	AR55	PWR	
VCAP0	AU48	PWR	
VCAP0	AU51	PWR	
VCAP0	AU55	PWR	
VCAP0	AW50	PWR	
VCAP0	AW53	PWR	
VCAP0	AW57	PWR	
VCAP0	AY50	PWR	
VCAP0	AY53	PWR	
VCAP0	AY57	PWR	
VCAP0	BB48	PWR	
VCAP0	BB51	PWR	
VCAP0	BB55	PWR	
VCAP0	BD48	PWR	
VCAP0	BD51	PWR	
VCAP0	BD55	PWR	
VCAP1	AK39	PWR	
VCAP1	AK42	PWR	
VCAP1	AK46	PWR	
VCAP1	AL39	PWR	
VCAP1	AL42	PWR	
VCAP1	AL46	PWR	
VCAP1	AN39	PWR	
VCAP1	AN42	PWR	
VCAP1	AN46	PWR	
VCAP1	AR37	PWR	
VCAP1	AR41	PWR	
VCAP1	AR44	PWR	
VCAP1	AU37	PWR	
VCAP1	AU41	PWR	
VCAP1	AU44	PWR	
VCAP1	AW39	PWR	

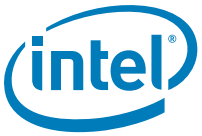

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	D54	REF	
VCC	D55	REF	
VCC	D57	REF	
VCC	D59	REF	
VCC	E42	REF	
VCC	E46	REF	
VCC	E50	REF	
VCC	E53	REF	
VCC	E57	REF	
VCC	E60	REF	
VCC	F55	REF	
VCC	G44	REF	
VCC	G51	REF	
VCC	G55	REF	
VCC	G60	REF	
VCC	H44	REF	
VCC	H51	REF	
VCC	H60	REF	
VCC	J55	REF	
VCC	K44	REF	
VCC	K51	REF	
VCC	K60	REF	
VCC	L55	REF	
VCC	M44	REF	
VCC	M51	REF	
VCC	M60	REF	
VCC	N42	REF	
VCC	N44	REF	
VCC	N48	REF	
VCC	N51	REF	
VCC	N55	REF	
VCC	P60	REF	
VCC	R41	REF	
VCC	R44	REF	
VCC	R48	REF	
VCC	R51	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	R55	REF	
VCC	U41	REF	
VCC	U44	REF	
VCC	U48	REF	
VCC	U51	REF	
VCC	U55	REF	
VCC	W41	REF	
VCC	W44	REF	
VCC	W48	REF	
VCC	W51	REF	
VCC	W55	REF	
VCC_SENSE	F64	Analog	O
VCCPLL	R37	REF	
VCCPLL	R39	REF	
VCCPLL	U37	REF	
VCCPLL	W37	REF	
VCCPLL	W39	REF	
VCCPWRGOOD_0	Y67	Async CMOS	I
VCCPWRGOOD_1	AM7	Async CMOS	I
VDDQ	BB15	REF	
VDDQ	BB17	REF	
VDDQ	BB19	REF	
VDDQ	BB21	REF	
VDDQ	BB23	REF	
VDDQ	BB24	REF	
VDDQ	BB26	REF	
VDDQ	BB28	REF	
VDDQ	BB30	REF	
VDDQ	BB32	REF	
VDDQ	BB33	REF	
VDDQ	BB35	REF	
VDDQ	BD15	REF	
VDDQ	BD17	REF	
VDDQ	BD19	REF	
VDDQ	BD21	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BD53	GND	
VSS	BD57	GND	
VSS	BE1	GND	
VSS	BE65	GND	
VSS	BE70	GND	
VSS	BE9	GND	
VSS	BF13	GND	
VSS	BF30	GND	
VSS	BF62	GND	
VSS	BF8	GND	
VSS	BG36	GND	
VSS	BG51	GND	
VSS	BH15	GND	
VSS	BH20	GND	
VSS	BH24	GND	
VSS	BH47	GND	
VSS	BH55	GND	
VSS	BH57	GND	
VSS	BH70	GND	
VSS	BJ1	GND	
VSS	BJ21	GND	
VSS	BJ64	GND	
VSS	BJ9	GND	
VSS	BK10	GND	
VSS	BK34	GND	
VSS	BK53	GND	
VSS	BK60	GND	
VSS	BK63	GND	
VSS	BL1	GND	
VSS	BL20	GND	
VSS	BL28	GND	
VSS	BL40	GND	
VSS	BL48	GND	
VSS	BL55	GND	
VSS	BL57	GND	
VSS	BL71	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BM17	GND	
VSS	BM24	GND	
VSS	BM32	GND	
VSS	BM44	GND	
VSS	BM51	GND	
VSS	BM70	GND	
VSS	BN1	GND	
VSS	BN6	GND	
VSS	BN64	GND	
VSS	BN71	GND	
VSS	BP42	GND	
VSS	BR3	GND	
VSS	BR68	GND	
VSS	BR69	GND	
VSS	BT68	GND	
VSS	BU11	GND	
VSS	BU14	GND	
VSS	BU18	GND	
VSS	BU21	GND	
VSS	BU25	GND	
VSS	BU32	GND	
VSS	BU37	GND	
VSS	BU44	GND	
VSS	BU48	GND	
VSS	BU51	GND	
VSS	BU55	GND	
VSS	BU58	GND	
VSS	BU62	GND	
VSS	BU7	GND	
VSS	BV64	GND	
VSS	BV66	GND	
VSS	C68	GND	
VSS	D10	GND	
VSS	D13	GND	
VSS	D17	GND	
VSS	D20	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AD50	VSS	GND	
AD51	VCC	REF	
AD53	VSS	GND	
AD55	VCC	REF	
AD57	VSS	GND	
AD59	VCAP2	PWR	
AD60	VCAP2	PWR	
AD62	VSS	GND	
AD69	COMP1	Analog	I
AD71	COMP3	Analog	I
AE2	CFG[13]	CMOS	I
AE64	VSS	GND	
AE66	COMP0	Analog	I
AE70	VSS	GND	
AF1	VSS	GND	
AF4	CFG[8]	CMOS	I
AF10	VSSAXG_SENSE	Analog	O
AF12	VAXG_SENSE	Analog	O
AF14	VAXG	REF	
AF15	VAXG	REF	
AF17	VAXG	REF	
AF19	VAXG	REF	
AF21	VAXG	REF	
AF23	VAXG	REF	
AF24	VAXG	REF	
AF26	VAXG	REF	
AF28	VAXG	REF	
AF30	VTT0	REF	
AF32	VTT0	REF	
AF33	VTT0	REF	
AF35	VTT0	REF	
AF37	VTT0	REF	
AF39	VTT0	REF	
AF41	VCC	REF	
AF42	VCC	REF	
AF44	VCC	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AF46	VCC	REF	
AF48	VCC	REF	
AF50	VCC	REF	
AF51	VCC	REF	
AF53	VCC	REF	
AF55	VCC	REF	
AF57	VCC	REF	
AF59	VCAP2	PWR	
AF6	CFG[16]	CMOS	I
AF60	VCAP2	PWR	
AF62	VSS	GND	
AF69	VSS	GND	
AF71	GFX_VID[0]	CMOS	O
AF8	CFG[15]	CMOS	I
AG2	CFG[9]	CMOS	I
AG6	VSS	GND	
AG7	CFG[7]	CMOS	I
AG9	VSS	GND	
AG64	VSS	GND	
AG67	GFX_VID[1]	CMOS	O
AG70	GFX_VID[2]	CMOS	O
AH1	CFG[10]	CMOS	I
AH4	VSS	GND	
AH12	VAXG	REF	
AH14	VAXG	REF	
AH15	VSS	GND	
AH17	VSS	GND	
AH19	VSS	GND	
AH21	VSS	GND	
AH23	VSS	GND	
AH24	VSS	GND	
AH26	VSS	GND	
AH28	VSS	GND	
AH30	VSS	GND	
AH32	VSS	GND	
AH33	VSS	GND	