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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SD2™ USB and Mass Storage Peripheral Controller
Core Processor	ARM9®
Program Memory Type	-
Controller Series	CYUSB
RAM Size	512K x 8
Interface	I²C, I²S, MMC/SD, SPI, UART, USB
Number of I/O	59
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb2024-bzxi

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Functional Overview

SD2™ is a USB 2.0 High Speed mass-storage controller providing the latest SD/MMC support. SD2 complies with the SD Specification, Version 3.0, and the MMC Specification, Version 4.41.

SD2 offers the following access paths among USB and mass storage ports:

- A USB-port (U-Port) supporting USB 2.0 peripheral
- Two mass-storage ports (S0-Port and S1-Port) supporting mass-storage devices. Following are the possible configurations for the two mass-storage ports:
  - SD and MMC
  - SD and SD
  - MMC and MMC
  - SD and SDIO
  - MMC and SDIO
  - SDIO and SDIO

Combinations of these accesses can happen independently or in an interleaved manner.

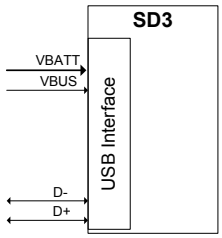
The SD2 complies with the USB 2.0 specification.

USB Interface (U-Port)

SD2 offers the following features:

- Supports USB peripheral functionality compliant with the USB 2.0 Specification
- Supports up to 16 IN and 16 OUT endpoints.
- Supports the USB 2.0 Streams feature. It also supports USB Attached SCSI (UAS) device class to optimize mass-storage access performance.
- As a USB peripheral, SD2 supports UAS and Mass Storage Class (MSC) peripheral classes.
- When the USB port is not in use, the PHY and transceiver may be disabled for power savings.

Figure 1. USB Interface Signals



Mass-Storage Support (S-Port)

The SD2 storage interface port supports the following specifications:

- SD Specification, Version 3.0
- Multimedia Card-System Specification, MMCA Technical Committee, Version 4.4
- SDIO Host controller compliant with SDIO Specification Version 3.00

I^2C Interface

SD2 has an I^2C interface compatible with the I^2C Bus Specification Revision 3. Because SD2's I^2C interface is capable of operating only as an I^2C master, it may be used to communicate with other I^2C slave devices. For example, SD2 may boot from an EEPROM connected to the I^2C interface, as a selectable boot option.

SD2's I^2C master controller also supports multi-master mode functionality.

The power supply for the I^2C interface is VIO5, which is a separate power domain from the other serial peripherals. This is to allow the I^2C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I^2C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I^2C controller supports the clock stretching feature to enable slower devices to exercise flow control.

Both SCL and SDA signals of the I^2C interface require external pull-up resistors. These resistors must be connected to VIO5.

UART Interface

The UART interface of SD2 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then SD2's UART only transmits data when the CTS input is asserted. In addition to this, SD2's UART asserts the RTS output signal, when it is ready to receive data.

I^2S Interface

SD2 has an I^2S port to support external audio codec devices. SD2 functions as I^2S Master as transmitter only. The I^2S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). SD2 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I^2S interface are 32 kHz, 44.1 kHz, and 48 kHz.

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend mode with USB 2.0 PHY disabled (L2 mode)	■ The power consumption in this mode does not exceed ISB_2 ■ USB 2.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory, and all internal RAM are maintained ■ All transactions must be completed before SD2 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on the core can put SD2 into suspend mode. For example, on USB suspend condition, firmware may decide to put SD2 into suspend mode	■ D+ transitioning to low or high ■ D– transitioning to low or high ■ Resume condition on SSRX +/- ■ Detection of VBUS ■ Assertion of GPIO[17] ■ Assertion of RESET#

Pin Description for BGA

Table 7. Pin List

Pin No.	Power Domain	I/O	Name	Description		
S2-PORT (GPIO)						
F10	VI01	I/O	GPIO[0]	GPIO		
F9	VI01	I/O	GPIO[1]	GPIO		
F7	VI01	I/O	GPIO[2]	GPIO		
G10	VI01	I/O	GPIO[3]	GPIO		
G9	VI01	I/O	GPIO[4]	GPIO		
F8	VI01	I/O	GPIO[5]	GPIO		
H10	VI01	I/O	GPIO[6]	GPIO		
H9	VI01	I/O	GPIO[7]	GPIO		
J10	VI01	I/O	GPIO[8]	GPIO		
J9	VI01	I/O	GPIO[9]	GPIO		
K11	VI01	I/O	GPIO[10]	GPIO		
L10	VI01	I/O	GPIO[11]	GPIO		
K10	VI01	I/O	GPIO[12]	GPIO		
K9	VI01	I/O	GPIO[13]	GPIO		
J8	VI01	I/O	GPIO[14]	GPIO		
G8	VI01	I/O	GPIO[15]	GPIO		
J6	VI01	I/O	GPIO[16]	GPIO		
K8	VI01	I/O	GPIO[17]	GPIO		
K7	VI01	I/O	GPIO[18]	GPIO		
J7	VI01	I/O	GPIO[19]	GPIO		
H7	VI01	I/O	GPIO[20]	GPIO		
G7	VI01	I/O	GPIO[21]	GPIO		
G6	VI01	I/O	GPIO[22]	GPIO		
K6	VI01	I/O	GPIO[23]	GPIO		
H8	VI01	I/O	GPIO[24]	GPIO		
G5	VI01	I/O	GPIO[25]	GPIO		
H6	VI01	I/O	GPIO[26]	GPIO		
K5	VI01	I/O	GPIO[27]	GPIO		
J5	VI01	I/O	GPIO[28]	GPIO		
H5	VI01	I/O	GPIO[29]	GPIO		
G4	VI01	I/O	GPIO[30]	PMODE[0]		
H4	VI01	I/O	GPIO[31]	PMODE[1]		
L4	VI01	I/O	GPIO[32]	PMODE[2]		
L8			NC	No Connect		
C5	CVDDQ	I	RESET#	Active Low. Hardware Reset.		
				8b MMC Configuration	**SD+GPIO Configuration**	**GPIO Configuration**
K2	VI02	I/O	GPIO[33]	S0_SD0	S0_SD0	GPIO
J4	VI02	I/O	GPIO[34]	S0_SD1	S0_SD1	GPIO
K1	VI02	I/O	GPIO[35]	S0_SD2	S0_SD2	GPIO
J2	VI02	I/O	GPIO[36]	S0_SD3	S0_SD3	GPIO
J3	VI02	I/O	GPIO[37]	S0_SD4	GPIO	GPIO
J1	VI02	I/O	GPIO[38]	S0_SD5	GPIO	GPIO

Table 7. Pin List (continued)

Pin No.	Power Domain	I/O	Name	Description							
H2	VI02	I/O	GPIO[39]	S0_SD6		GPIO			GPIO		
H3	VI02	I/O	GPIO[40]	S0_SD7		GPIO			GPIO		
F4	VI02	I/O	GPIO[41]	S0_CMD		S0_CMD			GPIO		
G2	VI02	I/O	GPIO[42]	S0_CLK		S0_CLK			GPIO		
G3	VI02	I/O	GPIO[43]	S0_WP		S0_WP			GPIO		
F3	VI02	I/O	GPIO[44]	S0S1_INS		S0S1_INS			GPIO		
F2	VI02	I/O	GPIO[45]	MMC0_RST_OUT		GPIO			GPIO		
				8b MMC	**SD+UART**	**SD+SPI**	**SD+GPIO**	**GPIO**	**GPIO+ UART+I2S**	**SD+I2S**	**UART+SPI+ I2S**
F5	VI03	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
E1	VI03	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E5	VI03	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
E4	VI03	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D1	VI03	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
D2	VI03	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
D3	VI03	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D4	VIO4	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
C9			NC	No Connect							
A3			NC	USB 3.0 SuperSpeed Receive Minus							
A4			NC	USB 3.0 SuperSpeed Receive Plus							
A6			NC	USB 3.0 SuperSpeed Transmit Minus							
A5			NC	USB 3.0 SuperSpeed Transmit Plus							
A9	VBATT/ VBUS	I/O	D+	USB (HS/FS) Data Plus							
A10	VBATT/ VBUS	I/O	D-	USB (HS/FS) Data Minus							
A11			NC	No Connect							
B2	CVDDQ	I	FSLC[0]	FSLC[0]							
C6	AVDD	I/O	XTALIN	XTALIN							
C7	AVDD	I/O	XTALOUT	XTALOUT							
B4	CVDDQ	I	FSLC[1]	FSLC[1]							
E6	CVDDQ	I	FSLC[2]	FSLC[2]							
D7	CVDDQ	I	CLKIN	CLKIN							
D6	CVDDQ	I	CLKIN_32	CLKIN_32							
D9	VIO5	I/O	I^2C_GPIO[58]	SCL (Serial Clock) for I^2C Bus Interface							
D10	VIO5	I/O	I^2C_GPIO[59]	SDA (Serial Data) for I^2C Bus Interface							
E7			NC	No Connect							
C10			NC	No Connect							
B11			NC	No Connect							
E8			NC	No Connect							
F6			NC	No Connect							
D11	VIO5	O	O[60]	Output only							

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} ..... 1.25 V

$S2_{VDDQ}$,$S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, V_{IO5} ..... 3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ..... 1.25 V

DC input voltage to any input pin ..... VCC + 0.3

DC voltage applied to outputs in High Z State ..... VCC + 0.3

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ±2.2-KV human body model (HBM) based on JESD22-A114
- Additional ESD Protection levels on D+, D–, VBUS, GND pins U-port and GPIO pins LPP-Port
- ±6-KV contact discharge, ±8-KV air gap discharge based on IEC61000-4-2 level 3A, ±8-KV contact discharge, and ±15-KV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ..... > 200 mA

Maximum output short circuit current for all I/O configurations. (Vout = 0 V) ..... –100 mA

Operating Conditions

TA (ambient temperature under bias) Industrial ..... –40 °C to +85 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$ supply voltage ..... 1.15 V to 1.25 V

V_{BATT} supply voltage ..... 3.2 V to 6 V

$S2_{VDDQ}$, $S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, C_{VDDQ} supply voltage ..... 1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

DC Specifications

Table 12. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO2}	SD/ MMC/ CF I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	SD/MMC I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO1}	GPIO/ CF I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	GPIO/ I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C voltage supply	1.2	3.3	V	1.2-,1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port).VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC - 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	0.9 × VCC	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.

Table 12. DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os that have a pull-up/down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at VDDQ
I_{CC} Core	Core and Analog Voltage Operating Current	–	150	mA	Total current through AVDD, VDD
I_{CC} USB	USB voltage supply operating current	–	20	mA	
I_{SB1}	Total suspend current during Suspend Mode with USB 3.0 PHY enabled (L1 mode)	–	–	mA	Core current: 1.5 mA I/O current: 20 uA USB current: 2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB2}	Total suspend current during Suspend Mode with USB 3.0 PHYdisabled (L2 mode)	–	–	mA	Core current: 250 uA I/O current: 20 uA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total Standby Current during Standby Mode (L3 mode)	–	–	µA	Core current: 60 uA I/O current: 20 uA USB current: 40 uA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total Standby Current during Core Power Down Mode (L4 mode)	–	–	µA	Core current: 0 uA I/O current: 20 uA USB current: 40 uA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage Ramp Rate on Core and I/O Supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise Level Permitted on VDD and I/O Supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise Level Permitted on AVDD Supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

Reset Sequence

The hard reset sequence requirements for SD2 are specified in the following table.

Table 13. Reset and Standby Timing Parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
tRH	Minimum high on RESET#		5	–
tRR	Reset Recovery Time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
tSBY	Time to enter Standby/Suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)		–	1
tWU	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted		5	–

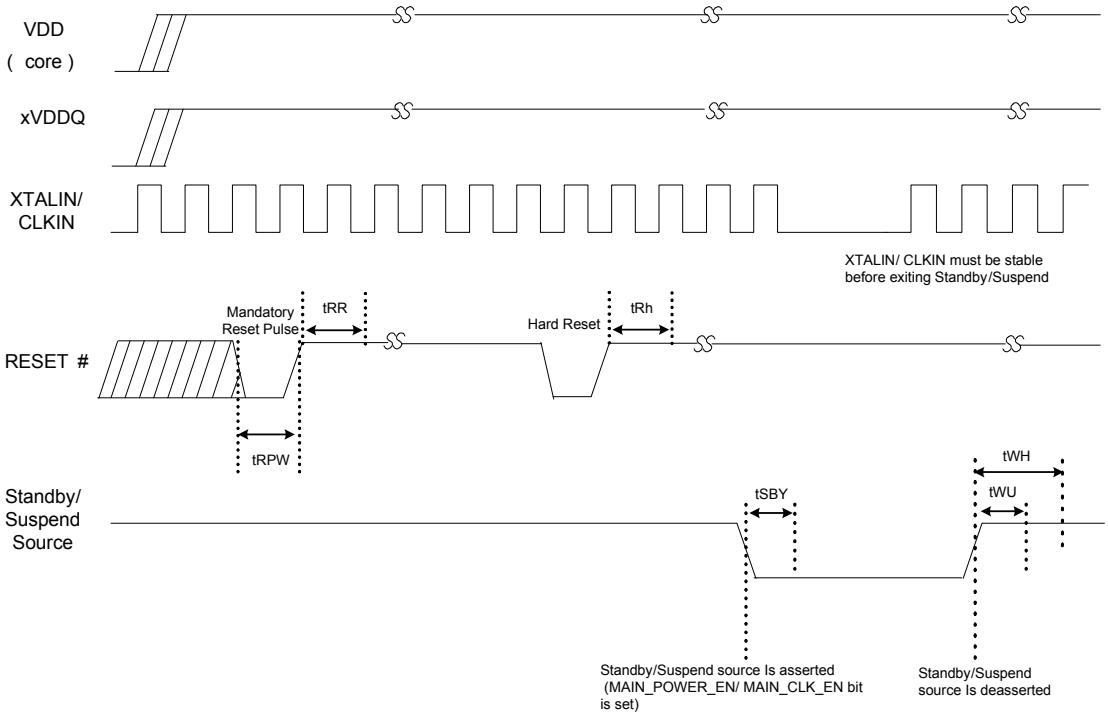



Figure 6. Reset Sequence