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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	6
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27143-24pxi

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC[®] 1, PowerPSoC[®], and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
 - □ Getting Started with PSoC[®] 1 AN75320
 - □ PSoC[®] 1 Getting Started with GPIO AN2094
 - □ PSoC[®] 1 Analog Structure and Configuration AN74170
 - □ PSoC[®] 1 Switched Capacitor Analog Blocks AN2041
 - Selecting Analog Ground and Reference AN2219

Note: For CY8C27X43 devices related Application note please click here.

- Development Kits:
 - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
 - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C27X43 devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

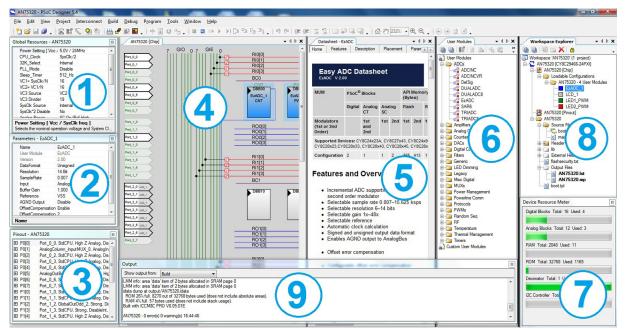
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

- 1. Global Resources all device hardware settings.
- 2. **Parameters –** the parameters of the currently selected User Modules.
- 3. Pinout information related to device pins.
- 4. Chip-Level Editor a diagram of the resources available on the selected chip.
- 5. Datasheet the datasheet for the currently selected UM
- 6. User Modules all available User Modules for the selected device.
- 7. **Device Resource Meter –** device resource usage for the current project configuration.
- 8. Workspace a tree level diagram of files associated with the project.
- 9. Output output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC[®] Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout





PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based components with low-cost system one, single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture lets you to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated in Logic Block Diagram on page 1, consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C27x43 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to eight digital blocks and 12 analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

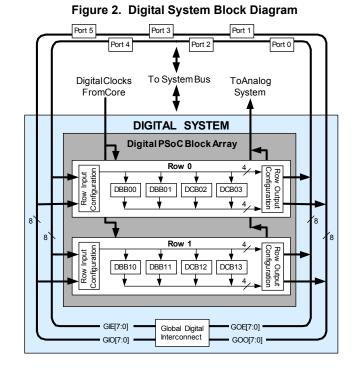
Memory encompasses 16 KB of flash for program storage, 256 bytes of SRAM for data storage, and up to 2 K of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. The 24-MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32-kHz internal low speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the 32.768-kHz external crystal oscillator (ECO) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24-MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Digital System

The digital system is composed of eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.



Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit) [1, 2]
- UART 8-bit with selectable parity (up to two)
- SPI slave and master (up to two) [3]
- I²C slave and multi-master (one available as a system resource)
- CRC/generator (8- to 32-bit)
- IrDA (up to two)
- Pseudo random sequence (PRS) generators (8- to 32-bit)

Notes

- 1. Errata: When operated between 4.75 V to 5.25 V, the input capture signal cannot be sourced from Row Output signals or the Broadcast clock signals. This problem has been fixed in silicon Rev B. For more information, see "Errata" on page 61.
- Errata: When operated between 3.0V to 4.75V, the input capture signal can only be sourced from Row input signal that has been re-synchronized. This problem has been fixed in silicon Rev B. For more information, see "Errata" on page 61.
 Errata: Development of the problem has been fixed in silicon Rev B. For more information, see "Errata" on page 61.

Errata: In PSoC, when one output of one SPI Slave block is connected to the input of other SPI slave block, data is shifted correctly but last bit is read incorrectly. For the workaround and more information related to this problem, see "Errata" on page 61.



Pinouts

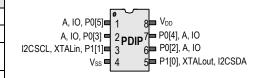
The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital I/O. However, Vss, V_{DD} , SMP, and XRES are not capable of Digital I/O.

8-pin Part Pinout

Table 2. Pin Definitions – 8-pin PDIP

Pin	Ту	ре	Pin	Description
No.	Digital	Analog	Name	Description
1	I/O	I/O	P0[5]	Analog column mux input and column output
2	I/O I/O		P0[3]	Analog column mux input and column output
3	I/O		P1[1]	Crystal Input (XTALin), I ² C serial clock (SCL), ISSP-SCLK ^[6]
4	Power		Vss	Ground connection.
5	I/O		P1[0]	Crystal output (XTALout), I ² C serial data (SDA), ISSP-SDATA ^[6]
6	I/O	I/O I/O P		Analog column mux input and column output
7	I/O	I/O I/O P0[4]		Analog column mux input and column output
8	Power V		V _{DD}	Supply voltage
I FGF		nalog I = I	nnut and	$\Omega = \Omega utput$

Figure 4. CY8C27143 8-pin PSoC Device



END: A = Analog, I = Input, and O = Output.

20-pin Part Pinout

Table 3. Pin Definitions – 20-pin SSOP, SOIC

Pin	Ту	pe	Pin	Description		
No.	Digital	Analog	Name	Description		
1	I/O	I	P0[7]	Analog column mux input		
2	I/O	I/O	P0[5]	Analog column mux input and column output		
3	I/O I/O		P0[3]	Analog column mux input and column output		
4	I/O	I	P0[1]	Analog column mux input		
5	Po	wer	SMP	Switch Mode Pump (SMP) connection to external components required		
6	I/O		P1[7]	I ² C Serial Clock (SCL)		
7	I/O		I/O		P1[5]	I ² C Serial Data (SDA)
8	I/O		P1[3]			
9	I/O		P1[1]	Crystal input (XTALin), I ² C SCL, ISSP-SCLK ^[6]		
10	Power		Vss	Ground connection.		
11	I/O		P1[0]	Crystal output (XTALout), I ² C SDA, ISSP-SDATA ^[6]		
12	I/O		P1[2]			
13	I/O		P1[4]	Optional external clock input (EXTCLK)		
14	I/O		P1[6]			
15	Input		XRES	Active high external reset with internal pull down		
16	I/O I		P0[0]	Analog column mux input		
17	I/O	I/O I/O P0[2		Analog column mux input and column output		
18	I/O	I/O	P0[4]	Analog column mux input and column output		
19	I/O	I	P0[6]	Analog column mux input		
20	Po	wer	V _{DD}	Supply voltage		

Figure 5. CY8C27243 20-pin PSoC Device

LEGEND: A = Analog, I = Input, and O = Output.

Note

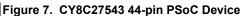
6. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Programmable System-on-Chip Technical Reference Manual for details.

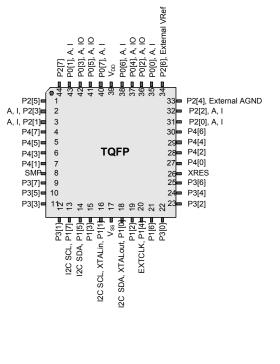


44-pin Part Pinout

Table 5. Pin Definitions – 44-pin TQFP

No. Digital Analog 1 I/O P2[5] 2 I/O I P2[1] 3 I/O I P2[1] 4 I/O P4[7] 5 I/O P4[3] 6 I/O P4[3] 7 I/O P4[1] 8 Power SMP 9 I/O P3[7] 10 I/O P3[3] 11 I/O P3[3] 12 I/O P3[1] 13 I/O P1[7] 14 I/O P3[3] 15 I/O P1[7] 16 I/O P1[3] 16 I/O P1[1] 17 Power Vss 18 I/O P1[2] 20 I/O P1[4] 0ptional external clock input (EXTCLK) 21 I/O P1[6] 22 I/O P3[2] 23 </th <th>Pin</th> <th>Ту</th> <th>ре</th> <th>Pin Name</th> <th>Description</th>	Pin	Ту	ре	Pin Name	Description
2 I/O I P2[3] Direct switched capacitor block input 3 I/O I P2[1] Direct switched capacitor block input 4 I/O P4[7] Direct switched capacitor block input 5 I/O P4[5] End 6 I/O P4[1] Patas 7 I/O P4[1] Patas 8 Power SMP SMP connection to external components require 9 I/O P3[5] Patas Patas 11 I/O P3[3] Patas Patas 12 I/O P3[1] I/C SCL Patas 13 I/O P1[7] I/C SCL Patas 14 I/O P1[5] I/C SDA Patas 15 I/O P1[3] I/C SCL, ISSP-SCLK ^[8] 16 I/O P1[1] Crystal output (XTALout), I/C SDA, ISSP-SDATa ^[8] 18 I/O P1[2] Patas Patas 20 I/O P1[4] <t< th=""><th>No.</th><th>Digital</th><th>Analog</th><th>Pin Name</th><th>Description</th></t<>	No.	Digital	Analog	Pin Name	Description
3 I/O I P2[1] Direct switched capacitor block input 4 I/O P4[7]	1	I/O		P2[5]	
4 I/O P4[7] 5 I/O P4[5] 6 I/O P4[5] 6 I/O P4[1] 7 I/O P4[1] 8 Power SMP 9 I/O P3[7] 10 I/O P3[5] 11 I/O P3[3] 12 I/O P3[1] 13 I/O P1[5] 14 I/O P1[5] 15 I/O P1[5] 16 I/O P1[1] 17 Power Vss 18 I/O P1[2] 20 I/O P1[2] 20 I/O P1[4] 19 I/O P1[2] 20 I/O P1[4] 21 I/O P1[4] 23 I/O P3[2] 24 I/O P3[4] 25 I/O P3[6] 26 Input	2	I/O	I	P2[3]	Direct switched capacitor block input
5 I/O P4[5] 6 I/O P4[3] 7 I/O P4[1] 8 Power SMP 9 I/O P3[5] 11 I/O P3[5] 11 I/O P3[5] 11 I/O P3[3] 12 I/O P3[1] 13 I/O P1[7] 14 I/O P1[5] 15 I/O P1[1] 16 I/O P1[1] 17 Power Vss 18 I/O P1[2] 20 I/O P1[2] 20 I/O P1[4] 21 I/O P1[6] 22 I/O P3[4] 23 I/O P3[4] 24 I/O P3[4] 25 I/O P3[6] 26 Input XRES Active high external reset with internal pull dow 27 I/O	3	I/O	I	P2[1]	Direct switched capacitor block input
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16 I/O P1[1] Crystal input (XTALin), I ² C SCL, ISSP-SCLK ^[8] 17 Power Vss Ground connection. 18 I/O P1[0] Crystal output (XTALout), I ² C SDA, ISSP-SDATA ^[8] 19 I/O P1[2] 20 I/O P1[4] Optional external clock input (EXTCLK) 21 I/O P1[6] 22 22 I/O P3[0] 23 23 I/O P3[2] 24 24 I/O P3[6] 25 26 Input XRES Active high external reset with internal pull dow 27 I/O P4[0] 28 28 I/O P4[2] 29 29 I/O P4[6] 31 I/O P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input	14	I/O		P1[5]	I ² C SDA
17 Power Vss Ground connection. 18 I/O P1[0] Crystal output (XTALout), I ² C SDA, ISSP-SDATA ^[8] 19 I/O P1[2] 20 I/O P1[4] Optional external clock input (EXTCLK) 21 I/O P1[6] 22 22 I/O P3[0] 23 23 I/O P3[4] 25 24 I/O P3[6] 26 26 Input XRES Active high external reset with internal pull dow 27 I/O P4[0] 28 I/O P4[2] 29 I/O P4[4] 30 I/O P4[6] 31 I/O P 2[0] Direct switched capacitor block input 32 I/O I P2[0] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog co	15	I/O		P1[3]	
18 I/O P1[0] Crystal output (XTALout), I ² C SDA, ISSP-SDATA ^[8] 19 I/O P1[2] 20 I/O P1[4] Optional external clock input (EXTCLK) 21 I/O P1[6] 22 I/O P3[0] 23 I/O P3[2] 24 I/O P3[4] 25 I/O P3[6] 26 Input XRES Active high external reset with internal pull dow 27 I/O P4[0] 28 I/O P4[2] 29 I/O P4[6] 31 I/O P2[2] Direct switched capacitor block input 32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input	16	I/O		P1[1]	Crystal input (XTALin), I ² C SCL, ISSP-SCLK ^[8]
19 I/O P1[2] 20 I/O P1[4] Optional external clock input (EXTCLK) 21 I/O P1[6] P3[0] 23 I/O P3[2] P3[2] 24 I/O P3[6] P3[6] 26 Input XRES Active high external reset with internal pull dow 27 I/O P4[0] P4[0] 28 I/O P4[6] P4[2] 29 I/O P4[6] P4[6] 30 I/O P4[6] P2[2] 29 I/O P4[6] P3[3] 31 I/O I P2[0] Direct switched capacitor block input 32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[4]	17	Po	wer	Vss	
20 I/O P1[4] Optional external clock input (EXTCLK) 21 I/O P1[6]	18	I/O		P1[0]	Crystal output (XTALout), I ² C SDA, ISSP-SDATA ^[8]
21 I/O P1[6] 22 I/O P3[0] 23 I/O P3[2] 24 I/O P3[6] 25 I/O P3[6] 26 Input XRES 27 I/O P4[0] 28 I/O P4[2] 29 I/O P4[4] 30 I/O P4[6] 31 I/O P2[2] 29 I/O P4[6] 31 I/O P2[2] 33 I/O P2[2] 33 I/O P2[4] 34 I/O P2[6] External Analog Ground (AGND) 34 34 I/O P2[6] External Voltage Reference (VRef) 35 35 I/O I 36 I/O I/O 37 I/O I/O 38 I/O I 90[6] Analog column mux input	19	I/O		P1[2]	
22 I/O P3[0] 23 I/O P3[2] 24 I/O P3[4] 25 I/O P3[6] 26 Input XRES 27 I/O P4[0] 28 I/O P4[2] 29 I/O P4[4] 30 I/O P4[6] 31 I/O I 32 I/O I 33 I/O P2[4] 33 I/O P2[4] 33 I/O P2[6] 34 I/O P2[6] 35 I/O I 36 I/O P0[0] 36 I/O I/O 37 I/O I/O 38 I/O I 90[6] Analog column mux input 38 I/O I	20	I/O			Optional external clock input (EXTCLK)
23 I/O P3[2] 24 I/O P3[4] 25 I/O P3[6] 26 Input XRES 27 I/O P4[0] 28 I/O P4[2] 29 I/O P4[6] 30 I/O P4[6] 31 I/O I 32 I/O I 33 I/O P2[4] 33 I/O P2[6] 34 I/O P2[6] 35 I/O I 36 I/O P0[0] 36 I/O I 37 I/O P0[2] 38 I/O I 38 I/O I	21	I/O			
24 I/O P3[4] 25 I/O P3[6] 26 Input XRES Active high external reset with internal pull dow 27 I/O P4[0] 28 I/O P4[2] 29 I/O P4[4] 30 I/O P4[6] 31 I/O I P2[0] Direct switched capacitor block input 32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[6] Analog column mux input	22	I/O		P3[0]	
25I/OP3[6]26InputXRESActive high external reset with internal pull dow27I/OP4[0]28I/OP4[2]29I/OP4[4]30I/OP4[6]31I/OI22I/OI33I/OP2[4]34I/OP2[6]55I/OI92[6]External Analog Ground (AGND)34I/OP2[6]35I/OI90[0]Analog column mux input36I/OI/O90[2]Analog column mux input and column output38I/OI90[6]Analog column mux input	23	I/O		P3[2]	
26InputXRESActive high external reset with internal pull dow27I/OP4[0]28I/OP4[2]29I/OP4[4]30I/OP4[6]31I/OI22I/OI33I/OP2[4]34I/OP2[6]55I/OI92[6]External Voltage Reference (VRef)35I/OI36I/OI/O90[0]Analog column mux input37I/OI/O38I/OI90[6]Analog column mux input	24	I/O		P3[4]	
27I/OP4[0]28I/OP4[2]29I/OP4[4]30I/OP4[6]31I/OI32I/OI33I/OP2[2]Direct switched capacitor block input33I/O94P2[4]External Analog Ground (AGND)34I/O92[6]External Voltage Reference (VRef)35I/O1/OP0[0]Analog column mux input36I/O1/OP0[4]Analog column mux input and column output37I/O1/OI90[6]Analog column mux input	25			P3[6]	
28 I/O P4[2] 29 I/O P4[4] 30 I/O P4[6] 31 I/O I P2[0] Direct switched capacitor block input 32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input 38 I/O I P0[6] Analog column mux input	26	Inp	but		Active high external reset with internal pull down
29I/OP4[4]30I/OP4[6]31I/OI32I/OI33I/OP2[2]Direct switched capacitor block input33I/O92[4]External Analog Ground (AGND)34I/O92[6]External Voltage Reference (VRef)35I/O10P0[0]Analog column mux input36I/O1/OP0[2]Analog column mux input and column output37I/O10I90[6]Analog column mux input	27	I/O		P4[0]	
30 I/O P4[6] 31 I/O I P2[0] Direct switched capacitor block input 32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input 38 I/O I P0[6] Analog column mux input	28	I/O			
31 I/O I P2[0] Direct switched capacitor block input 32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input	29	I/O		P4[4]	
32 I/O I P2[2] Direct switched capacitor block input 33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input	30	I/O		P4[6]	
33 I/O P2[4] External Analog Ground (AGND) 34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input	31	I/O	I	P2[0]	Direct switched capacitor block input
34 I/O P2[6] External Voltage Reference (VRef) 35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input	32	I/O	I		Direct switched capacitor block input
35 I/O I P0[0] Analog column mux input 36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input		I/O			
36 I/O I/O P0[2] Analog column mux input and column output 37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input					External Voltage Reference (VRef)
37 I/O I/O P0[4] Analog column mux input and column output 38 I/O I P0[6] Analog column mux input	35	I/O	I	P0[0]	
38 I/O I P0[6] Analog column mux input	36	I/O	I/O		Analog column mux input and column output
			I/O		
39 Power V _{DD} Supply voltage	38	I/O	I		Analog column mux input
			wer	V _{DD}	Supply voltage
40 I/O I P0[7] Analog column mux input	-	-		P0[7]	- ·
41 I/O I/O P0[5] Analog column mux input and column output	41	I/O	I/O		Analog column mux input and column output
42 I/O I/O P0[3] Analog column mux input and column output	42	-	I/O	P0[3]	Analog column mux input and column output
43 I/O I P0[1] Analog column mux input	43	-	I		Analog column mux input
44 I/O P2[7]	44	I/O		P2[7]	





LEGEND: A = Analog, I = Input, and O = Output.

8. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Programmable System-on-Chip Technical Reference Manual for details.



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Table 11. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	1D			5D		ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E			5E		ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27	1	ALT_CR0	67	RW		A7	1	1	E7	1
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDIORI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	1
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	1
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW	1	FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW	1	BF	1	CPU SCR0	FF	#



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C27x43 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C \leq T_A \leq 70 °C and T_J \leq 82 °C.

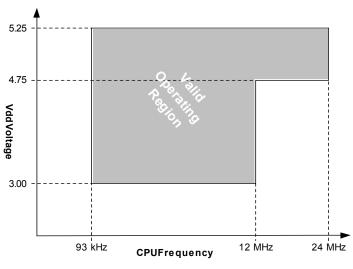


Figure 11. Voltage versus CPU Frequency

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Min	Тур	Max	Unit	Notes
T _{STG}	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
T _{BAKETEMP}	Bake temperature	-	125	See package label	°C	
^t вакетіме	Bake time	See package label	-	72	Hours	
T _A	Ambient temperature with power applied	-40	-	+85	°C	
V _{DD}	Supply voltage on V _{DD} relative to Vss	-0.5	-	+6.0	V	
V _{IO}	DC input voltage	Vss - 0.5	-	V _{DD} + 0.5	V	
V _{IOZ}	DC voltage applied to tristate	Vss – 0.5	-	V _{DD} + 0.5	V	
I _{MIO}	Maximum current into any port pin	-25	_	+50	mA	
I _{MAIO}	Maximum current into any port pin configured as analog driver	-50	_	+50	mA	
ESD	Electrostatic discharge voltage	2000	-	-	V	Human body model ESD.
LU	Latch-up current	-	-	200	mA	



DC GPIO Specifications

Table 15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq 85$ °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq 85$ °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 15. DC GPIO Specifications

Symbol	Description	Min	Тур	Max	Unit	Notes
R _{PU}	Pull-up resistor	4	5.6	8	kΩ	
R _{PD}	Pull-down resistor	4	5.6	8	kΩ	
V _{OH}	High output level	V _{DD} – 1.0	-	-	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V _{OL}	Low output level	-	-	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
I _{OH}	High-level source current	10	-	-	mA	$V_{OH} = V_{DD} - 1.0 V$, see the limitations of the total current in the note for V_{OH}
I _{OL}	Low-level sink current	25	-	-	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V _{IL}	Input low level	-	_	0.8	V	V _{DD} = 3.0 to 5.25
V _{IH}	Input high level	2.1	_		V	V _{DD} = 3.0 to 5.25
V _H	Input hysterisis	-	60	-	mV	
IIL	Input leakage (absolute value)	-	1	_	nA	Gross tested to 1 µA.
C _{IN}	Capacitive load on pins as input	-	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C _{OUT}	Capacitive load on pins as output	_	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Operational Amplifier Specifications

Table 16 and Table 17 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and –40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched cap PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

	Table 16.	5-V DC	Operational Am	plifier S	pecifications
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Symbol	Description	Min	Тур	Max	Units	Notes
V _{osoa}	Input offset voltage (absolute value) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high		1.6 1.6 1.6 1.6 1.6	10 10 10 10 10 10	mV mV mV mV mV mV	
TCV _{OSOA}	Average input offset voltage drift	-	4	20	µV/∘C	
I _{EBOA}	Input leakage current (port 0 analog pins)	-	20	-	pА	Gross tested to 1 µA.
CINOA	Input capacitance (port 0 analog pins)	-	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V _{CMOA}	Common mode voltage range	0	_	V _{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common mode voltage range (high power or high Opamp bias)	0.5	-	V _{DD} – 0.5	V	



Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Тур	Max	Unit
	RefPower = high	V _{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
ARF_CR [5:3] F 0b011 F 0b011 F 0b100 F 0b100 F	Opamp bias = high	V _{AGND}	AGND	2 × Bandgap	2.500	2.604	3.699	V
		V _{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = high	V _{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
	Opamp bias = low	V _{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
06011		V _{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
ARF_CR [5:3] 0b011 - 0b100	RefPower = medium	V _{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
	Opamp bias = high	V _{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V _{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = medium	V _{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
	Opamp bias = low	V _{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V _{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.657 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.662 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
05100		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
0b100	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 – P2[6]	2.592 – P2[6]	2.662 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 – P2[6]	2.594 – P2[6]	2.665 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V



Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Тур	Max	Unit
	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
[5:3] 0b101		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
0b101 F 0b110 F 0 F 0 F 0 F 0 F 0 F 0 F 0 F		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
05101		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
00101	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
	RefPower = high	V _{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
	Opamp bias = high	V _{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.009	V _{SS} + 0.038	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V _{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
06110		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.005	V _{SS} + 0.024	V
00110	RefPower = medium	V _{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
	Opamp bias = high	V _{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.026	V
	RefPower = medium	V _{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
[5:3] 0b101 -	Opamp bias = low	V _{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.018	V
	RefPower = high	V _{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
	Opamp bias = high	V _{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.010	V _{SS} + 0.038	V
	RefPower = high	V _{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
	Opamp bias = low	V _{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
0b111		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.024	V
00111	RefPower = medium	V _{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
	Opamp bias = high	V _{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.026	V
	RefPower = medium	V _{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
	Opamp bias = low	V _{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.018	V



DC Programming Specifications

Table 26 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. DC Programming Specifications

Symbol	Description	Min	Тур	Max	Unit	Notes
V _{DDP}	V _{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools.
V _{DDLV}	Low V _{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V _{DDHV}	High V _{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
V _{DDIWRITE}	Supply voltage for flash write operation	3		5.25	V	This specification applies to this device when it is executing internal flash writes.
I _{DDP}	Supply current during programming or verify	-	5	25	mA	
V _{ILP}	Input low voltage during programming or verify	-	-	0.8	V	
V _{IHP}	Input high voltage during programming or verify	2.2	-	-	V	
I _{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	-	-	0.2	mA	Driving internal pull-down resistor.
I _{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	-	-	1.5	mA	Driving internal pull-down resistor.
V _{OLV}	Output low voltage during programming or verify	-	-	Vss + 0.75	V	
V _{OHV}	Output high voltage during programming or verify	V _{DD} – 1.0	-	V _{DD}	V	
Flash _{ENPB}	Flash endurance (per block)	50,000 ^[19]	-	-	Cycles	Erase/write cycles per block.
Flash _{ENT}	Flash endurance (total) ^[20]	1,800,000	-	-	Cycles	Erase/write cycles.
Flash _{DR}	Flash data retention	10	1	-	Years	

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. DC I²C Specifications

Parameter	Description	Min	Тур	Max	Units	Notes
V _{ILI2C} ^[21]	Input low level	-	-	0.3 × V _{DD}	V	$3.0~V \leq V_{DD} \leq 3.6~V$
		-	-	0.25 × V _{DD}	V	$4.75~V \leq V_{DD} \leq 5.25~V$
V _{IHI2C} ^[21]	Input high level	$0.7 \times V_{DD}$	-	-	V	$3.0~V \leq V_{DD} \leq 5.25~V$

Notes

^{19.} The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V. 19: The 50,000 cycle hash endurance per block is only guaranteed in the hash is operating within one voltage range. Voltage ranges are 3.0 v to 3.6 v and 4.7 v to 5.25 v.
 20: A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles).
 For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC[®] Flash – AN2015 for more information.
 21. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections. The I²C GPIO pins also meet the above specs.



AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and –40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 28. AC Chip-Level Specifications

Symbol	Description	Min	Тур	Мах	Unit	Notes
F _{IMO}	Internal main oscillator (IMO) frequency	23.4	24	24.6 ^[22]	MHz	Trimmed. Utilizing factory trim values.
F _{CPU1}	CPU frequency (5 V nominal)	0.0914	24	24.6 ^[22]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F _{CPU2}	CPU frequency (3.3 V nominal)	0.0914	12	12.3 ^[23]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F _{48M}	Digital PSoC block frequency	0	48	49.2 ^[22, 24]	MHz	Refer to AC Digital Block Specifications on page 40.
F _{24M}	Digital PSoC block frequency	0	24	24.6 ^[24]	MHz	
F _{32K1}	Internal low speed oscillator (ILO) frequency	15	32	64	kHz	
F _{32K2}	External crystal oscillator	-	32.768	_	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F _{32K_U}	ILO untrimmed frequency	5	-	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
F _{PLL}	PLL frequency	-	23.986	_	MHz	Multiple (x732) of crystal frequency.
t _{PLLSLEW}	PLL lock time	0.5	-	10	ms	
t _{PLLSLEWSLOW}	PLL lock time for low gain setting	0.5	-	50	ms	
t _{OS}	External crystal oscillator startup to 1%	-	1700	2620	ms	
tosacc	External crystal oscillator startup to 100 ppm	_	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{osacc} period. Correct operation assumes a properly loaded 1 μ W maximum drive level 32.768 kHz crystal. 3.0 V \leq V _{DD} \leq 5.5 V, -40 °C \leq T _A \leq 85 °C.
t _{XRST}	External reset pulse width	10	-	_	μs	
DC _{24M}	24 MHz duty cycle	40	50	60	%	
DC _{ILO}	ILO duty cycle	20	50	80	%	
Step _{24M}	24 MHz trim step size	-	50	-	kHz	
t _{POWERUP}	Time from end of POR to CPU executing code	-	16	100	ms	wer-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
Fout _{48M}	48 MHz output frequency	46.8	48.0	49.2 ^[22, 23]	MHz	Trimmed. Utilizing factory trim values.
F _{MAX}	Maximum frequency of signal on row input or row output.	-	-	12.3	MHz	
SR _{POWER_UP}	Power supply slew rate	_	-	250	V/ms	V _{DD} slew rate during power-up.

Notes

22.4.75 V < V_{DD} < 5.25 V. 23.3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC[®] Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V. 24. See the individual user module datasheets for information on maximum frequencies for user modules.



AC GPIO Specifications

Table 29 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 29. AC GPIO Specifications

Symbol	Description	Min	Тур	Max	Unit	Notes
F _{GPIO}	GPIO operating frequency	0	-	12	MHz	Normal strong mode
t _{RiseF}	Rise time, normal strong mode, Cload = 50 pF	3	-	18	ns	V _{DD} = 4.5 to 5.25 V, 10% to 90%
t _{FallF}	Fall time, normal strong mode, Cload = 50 pF	2	-	18	ns	V _{DD} = 4.5 to 5.25 V, 10% to 90%
t _{RiseS}	Rise time, slow strong mode, Cload = 50 pF	10	27	-	ns	V _{DD} = 3 to 5.25 V, 10% to 90%
t _{FallS}	Fall time, slow strong mode, Cload = 50 pF	10	22	-	ns	V _{DD} = 3 to 5.25 V, 10% to 90%

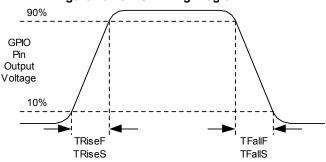


Figure 16. GPIO Timing Diagram

AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and –40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V.

Table 30.	5-V AC	Operational	Amplifier	Specifications
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Symbol	Description	Min	Тур	Max	Unit
t _{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	_ _ _	_ _ _	3.9 0.72 0.62	μs μs μs
t _{SOA}	Falling settling time from 20% of ∆V to 0.1% of ∆V (10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	_ _ _	_ _ _	5.9 0.92 0.72	μs μs μs
SR _{ROA}	Rising slew rate (20% to 80%)(10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	0.15 1.7 6.5	_ _ _		V/μs V/μs V/μs
SR _{FOA}	Falling slew rate (20% to 80%)(10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	0.01 0.5 4.0	- - -	- - -	V/μs V/μs V/μs
BW _{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	0.75 3.1 5.4	_ _ _	_ _ _	MHz MHz MHz
E _{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	-	100	_	nV/rt-Hz



Table 31. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units
t _{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = low, Opamp bias = low Power = low, Opamp bias = high			3.92 0.72	μs μs
t _{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high			5.41 0.72	μs μs
SR _{ROA}	Rising slew rate (20% to 80%)(10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	0.31 2.7		-	V/μs V/μs
SR _{FOA}	Falling slew rate (20% to 80%)(10 pF load, Unity Gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	0.24 1.8		-	V/μs V/μs
BW _{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	0.67 2.8		-	MHz MHz
E _{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	-	100	1	nV/rt-Hz

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 K resistance and the external capacitor.

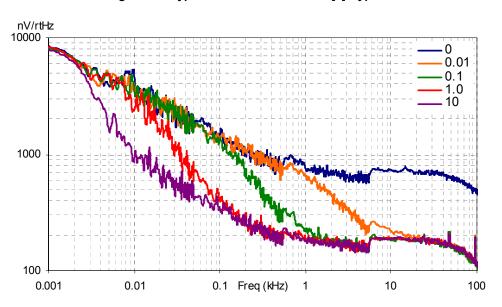


Figure 17. Typical AGND Noise with P2[4] Bypass



AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C \leq T_A \leq 85 °C, or 3.0 V to 3.6 V and –40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 34. 5-V AC Analog Output Buffer Specifications

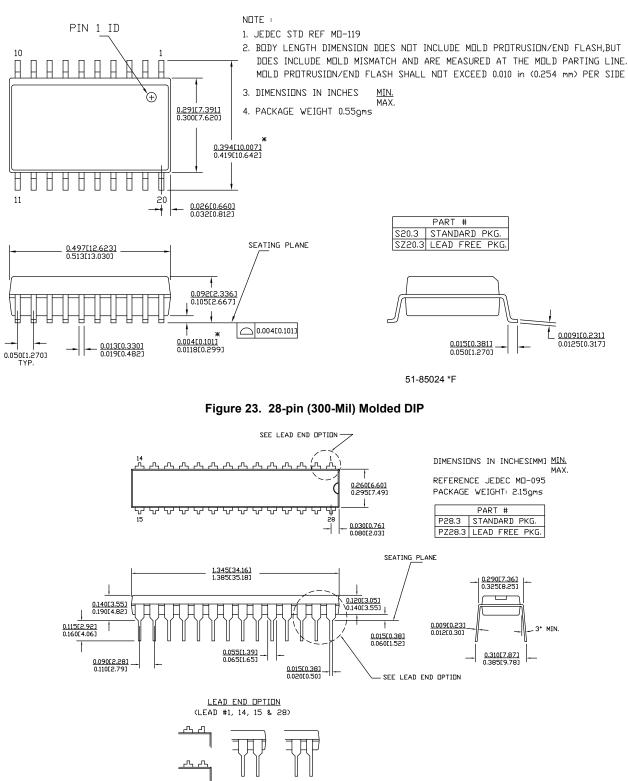
Symbol	Description	Min	Тур	Max	Unit
t _{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high			2.5 2.5	μs μs
t _{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high			2.2 2.2	μs μs
SR _{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	0.65 0.65		_ _	V/μs V/μs
SR _{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	0.65 0.65			V/μs V/μs
BW _{OB}	Small signal bandwidth, 20 mV _{pp} , 3 dB BW, 100 pF load Power = low Power = high	0.8 0.8		_ _	MHz MHz
BW _{OB}	Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load Power = low Power = high	300 300		_ _	kHz kHz

Table 35. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Unit
t _{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high		-	3.8 3.8	μs μs
t _{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high		-	2.6 2.6	μs μs
SR _{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	0.5 0.5	-		V/μs V/μs
SR _{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	0.5 0.5			V/μs V/μs
BW _{OB}	Small signal bandwidth, 20m V _{pp} , 3 dB BW, 100 pF load Power = low Power = high	0.7 0.7			MHz MHz
BW _{OB}	Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load Power = low Power = high	200 200			kHz kHz



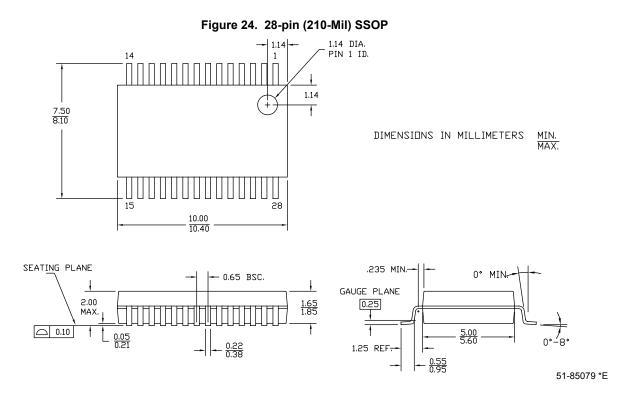
Figure 22. 20-pin SOIC (0.513 × 0.300 × 0.0932 Inches) Package Outline, 51-85024



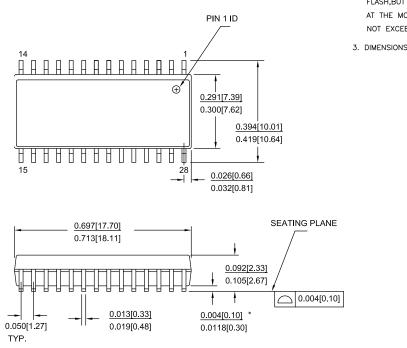
51-85014 *G



CY8C27143/CY8C27243 CY8C27443/CY8C27543 CY8C27643



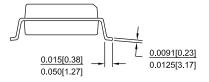




NOTE :

- 1. JEDEC STD REF MO-119
- BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
- 3. DIMENSIONS IN INCHES MIN.

PART #			
STANDARD PKG.			
LEAD FREE PKG.			
LEAD FREE PKG.			

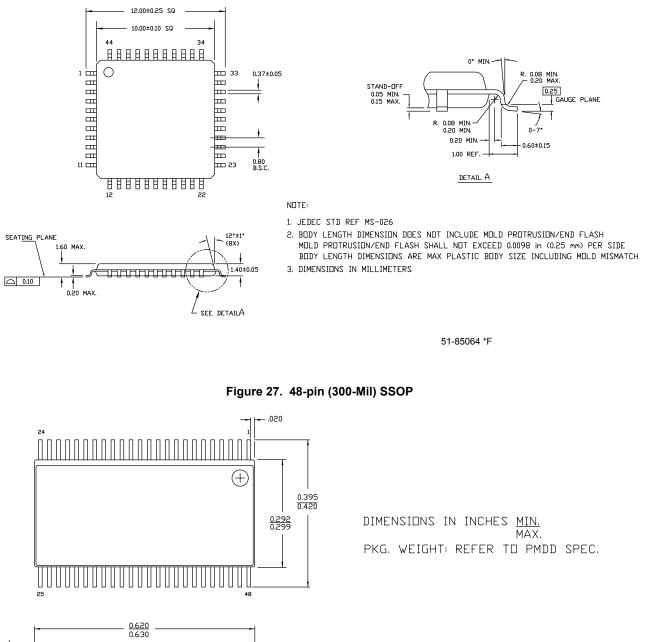


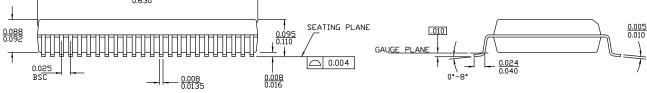
51-85026 *H



CY8C27143/CY8C27243 CY8C27443/CY8C27543 CY8C27643

Figure 26. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064





51-85061 *F



Thermal Impedances

Table 40. Thermal Impedances per Package

Package	Typical θ _{JA} ^[34]
8-pin PDIP	120 °C/W
20-pin SSOP	116 °C/W
20-pin SOIC	79 °C/W
28-pin PDIP	67 °C/W
28-pin SSOP	95 °C/W
28-pin SOIC	68 °C/W
44-pin TQFP	61 °C/W
48-pin SSOP	69 °C/W
48-pin QFN ^[35]	18 °C/W
56-pin SSOP	47 °C/W

Capacitance on Crystal Pins

Table 41. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8-pin PDIP	2.8 pF
20-pin SSOP	2.6 pF
20-pin SOIC	2.5 pF
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
44-pin TQFP	2.6 pF
48-pin SSOP	3.3 pF
48-pin QFN	2.3 pF
56-pin SSOP	3.3 pF

Solder Reflow Specifications

The following table shows the solder reflow temperature limits that must not be exceeded. Thermap ramp rate should 3 °C or lower.

Table 42. Solder Reflow Specifications

Package	Maximum Peak Temperature (T _C) ^[36]	Maximum Time above T _C – 5 °C
8-pin PDIP	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
20-pin SOIC	260 °C	30 seconds
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes

34. T_J = T_A + POWER × θ_{JA}.
 35. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.
 36. Refer to Table 44 on page 53.



Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	 A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V _{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V _{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.



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