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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27243-24pvxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C27X43 devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C27X43 devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

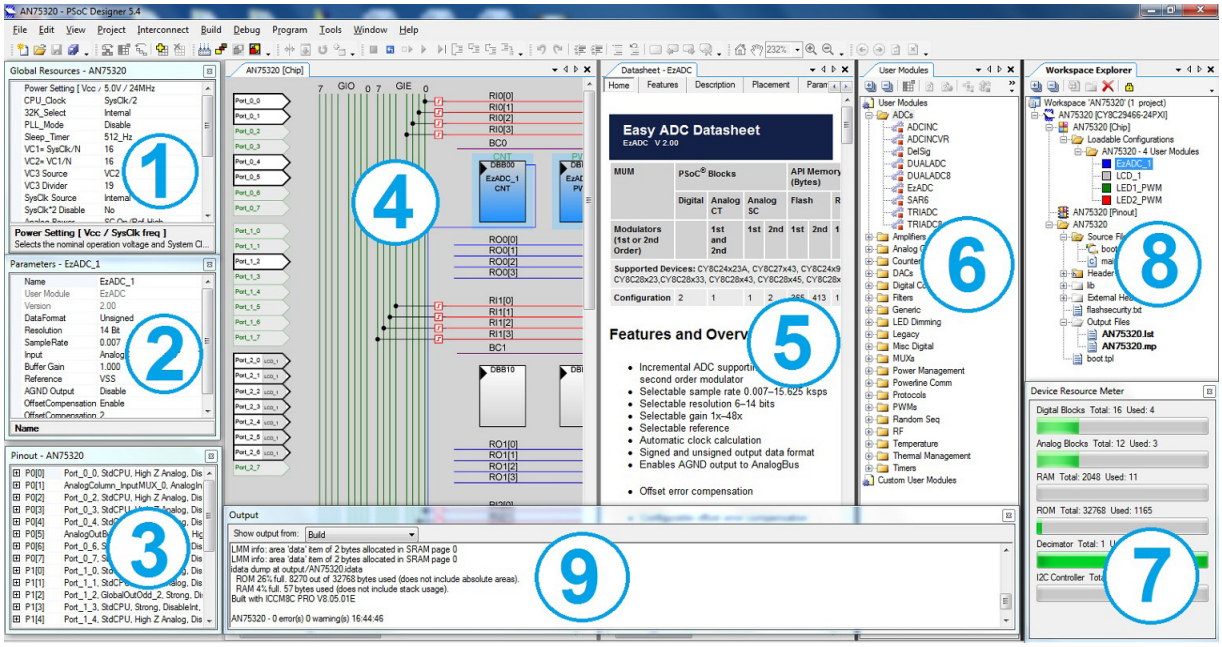
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



Pinouts

The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, V_{DD}, SMP, and XRES are not capable of Digital I/O.

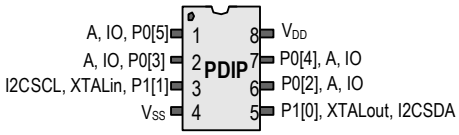
8-pin Part Pinout

Table 2. Pin Definitions – 8-pin PDIP

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I/O	P0[5]	Analog column mux input and column output
2	I/O	I/O	P0[3]	Analog column mux input and column output
3	I/O		P1[1]	Crystal Input (XTALin), I^2C serial clock (SCL), ISSP-SCLK[6]
4	Power		Vss	Ground connection.
5	I/O		P1[0]	Crystal output (XTALout), I^2C serial data (SDA), ISSP-SDATA[6]
6	I/O	I/O	P0[2]	Analog column mux input and column output
7	I/O	I/O	P0[4]	Analog column mux input and column output
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C27143 8-pin PSoC Device



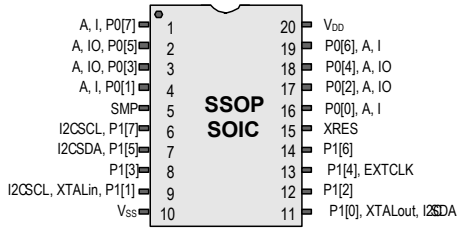
20-pin Part Pinout

Table 3. Pin Definitions – 20-pin SSOP, SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	Switch Mode Pump (SMP) connection to external components required
6	I/O		P1[7]	I^2C Serial Clock (SCL)
7	I/O		P1[5]	I^2C Serial Data (SDA)
8	I/O		P1[3]	
9	I/O		P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[6]
10	Power		Vss	Ground connection.
11	I/O		P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[6]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional external clock input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I/O	P0[2]	Analog column mux input and column output
18	I/O	I/O	P0[4]	Analog column mux input and column output
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C27243 20-pin PSoC Device



Note
6. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip* Technical Reference Manual for details.

Table 17. 3.3-V DC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	50	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

DC Low-Power Comparator Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 18. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
V_{REFLPC}	Low-power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

DC Analog Output Buffer Specifications

Table 19 and Table 20 on page 24 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – –	 3 3 3 3	 19 19 19 19	 mV mV mV mV	
TCV_{OSOB}	Average input offset voltage drift	–	5	30	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = low Power = high	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD}/2$)	–	–	–		
	Power = low	–	–	0.5 × V_{DD} – 1.3	V	
	Power = high	–	–	0.5 × V_{DD} – 1.3	V	

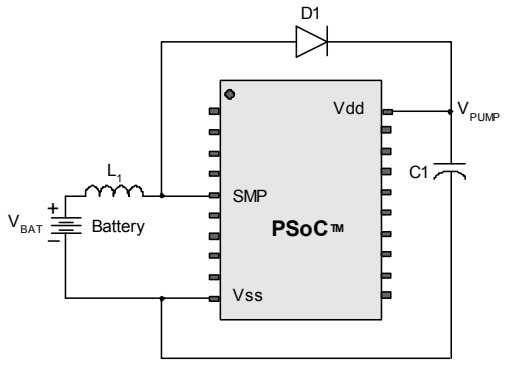
DC Switch Mode Pump Specifications

Table 21 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{PUMP} 5 V	5 V output voltage	4.75	5.0	5.25	V	Configured as in Note 15. Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3 V output voltage	3.00	3.25	3.60	V	Configured as in Note 15. Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	 8 5	 – –	 – –	 mA mA	Configured as in Note 15. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 15. SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 15. SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.1	–	–	V	Configured as in Note 15.
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configured as in Note 15. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 25 on page 33.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configured as in Note 15. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 25 on page 33.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configured as in Note 15. Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configured as in Note 15. Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Figure 12. Basic Switch Mode Pump Circuit



Note
15. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 12.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the analog continuous time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 22. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.078	$V_{DD}/2$ – 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.336	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.250	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.056	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.255	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.057	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.337	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.256	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.047	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.258	V

Note
16. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.009	V_{SS} + 0.038	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V_{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
		V_{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
		V_{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.010	V_{SS} + 0.038	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V

Table 28. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
tjit_IMO[25]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	N = 32
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900		
	24 MHz IMO period jitter (RMS)	–	100	400		
tjit_PLL [25]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	N = 32
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200		
	24 MHz IMO period jitter (RMS)	–	100	700		

Figure 13. PLL Lock Timing Diagram

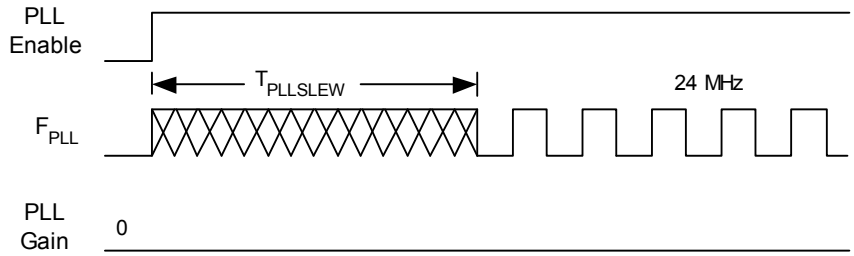


Figure 14. PLL Lock for Low Gain Setting Timing Diagram

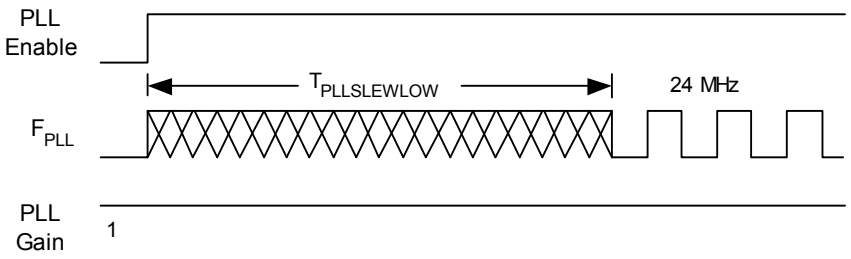
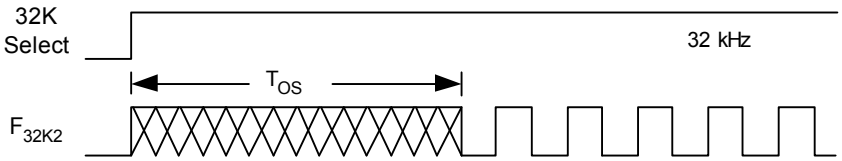


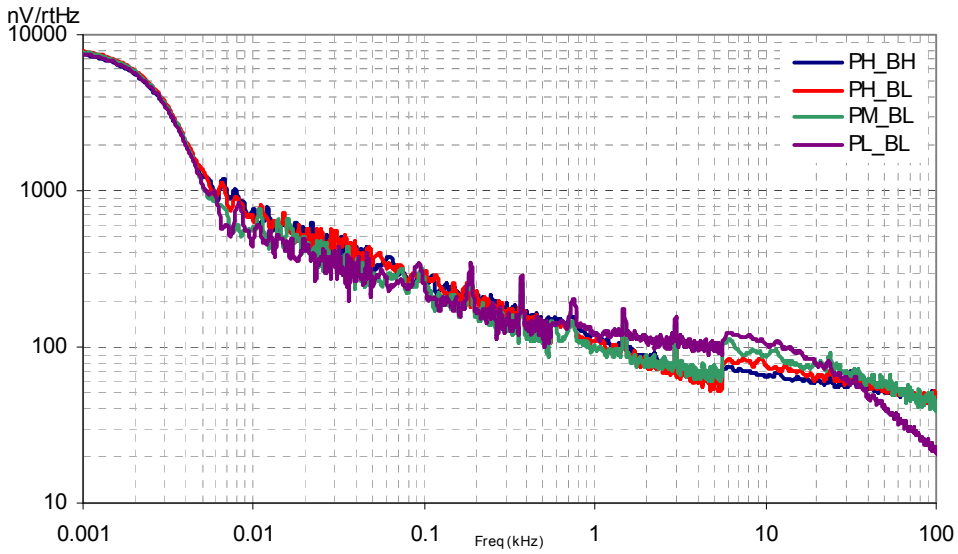
Figure 15. External Crystal Oscillator Startup Timing Diagram



Note
25. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 18. Typical Opamp Noise



AC Low-Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 32. AC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

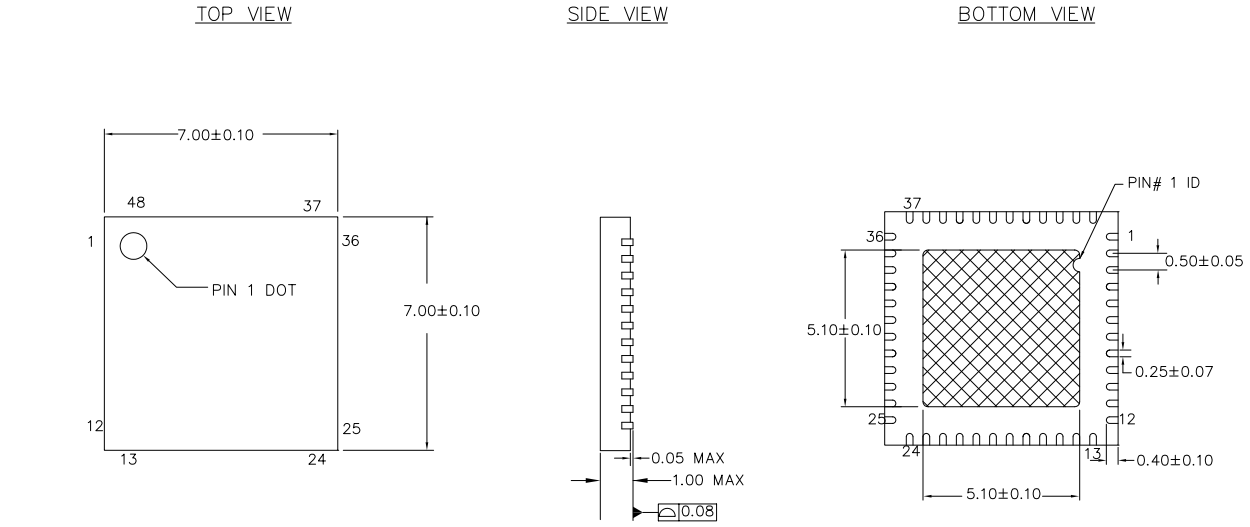
Table 33. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer [26, 27]	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[28]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[28]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[28]	–	–	ns	
	Disable mode	50[28]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS [29]	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[28]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Notes

26. Errata: When operated between 4.75V to 5.25V, the input capture signal cannot be sourced from Row Output signals or the Broadcast clock signals. This problem has been fixed in silicon Rev B. For more information, see "Errata" on page 61.
27. Errata: When operated between 3.0V to 4.75V, the input capture signal can only be sourced from Row input signal that has been re-synchronized. This problem has been fixed in silicon Rev B. For more information, see "Errata" on page 61.
28. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
29. Errata: In PSoC, when one output of one SPI Slave block is connected to the input of other SPI slave block, data is shifted correctly but last bit is read incorrectly. For the workaround and more information related to this problem, see "Errata" on page 61.

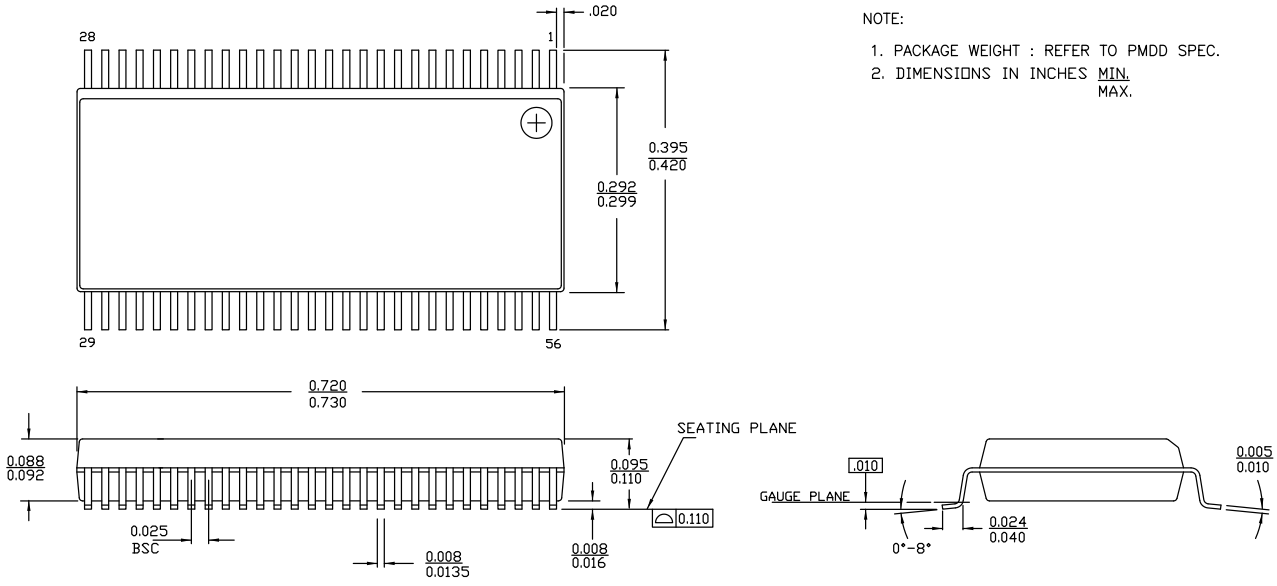
Figure 28. 48-pin QFN 7 × 7 × 1 mm (Sawn Type)



NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *G

Figure 29. 56-pin (300-Mil) SSOP



NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN.
MAX.

51-85062 *F

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Development Tool Selection

This chapter presents the development tools available for all current PSoC device families including the CY8C27x43 family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface lets you to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit lets you to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 43. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[37]	Foot Kit[38]	Adapter[39]
CY8C27143-24PXI	8-pin PDIP	CY3250-27XXX	CY3250-8PDIP-FK	Adapters can be found at http://www.emulation.com.
CY8C27243-24PVXI	20-pin SSOP	CY3250-27XXX	CY3250-20SSOP-FK	
CY8C27243-24SXI	20-pin SOIC	CY3250-27XXX	CY3250-20SOIC-FK	
CY8C27443-24PXI	28-pin PDIP	CY3250-27XXX	CY3250-28PDIP-FK	
CY8C27443-24PVXI	28-pin SSOP	CY3250-27XXX	CY3250-28SSOP-FK	
CY8C27443-24SXI	28-pin SOIC	CY3250-27XXX	CY3250-28SOIC-FK	
CY8C27543-24AXI	44-pin TQFP	CY3250-27XXX	CY3250-44TQFP-FK	
CY8C27643-24PVXI	48-pin SSOP	CY3250-27XXX	CY3250-48SSOP-FK	
CY8C27643-24LTXI	48-pin QFN	CY3250-27XXXQFN	CY3250-48QFN-FK	

Notes
37. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
38. Foot kit includes surface mount feet that can be soldered to the target PCB.
39. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the CY8C27x43 PSoC device's key package features and ordering codes.

Table 44. CY8C27x43 PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
8-pin (300-Mil) DIP	CY8C27143-24PXI	16 K	256	No	–40 °C to +85 °C	8	12	6	4	4	No
20-pin (210-Mil) SSOP	CY8C27243-24PVXI	16 K	256	Yes	–40 °C to +85 °C	8	12	16	8	4	Yes
20-pin (210-Mil) SSOP (Tape and Reel)	CY8C27243-24PVXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	16	8	4	Yes
20-pin (300-Mil) SOIC	CY8C27243-24SXI	16 K	256	Yes	–40 °C to +85 °C	8	12	16	8	4	Yes
20-pin (300-Mil) SOIC (Tape and Reel)	CY8C27243-24SXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	16	8	4	Yes
28-pin (300-Mil) DIP	CY8C27443-24PXI	16 K	256	Yes	–40 °C to +85 °C	8	12	24	12	4	Yes
28-pin (210-Mil) SSOP	CY8C27443-24PVXI	16 K	256	Yes	–40 °C to +85 °C	8	12	24	12	4	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C27443-24PVXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	24	12	4	Yes
28-pin (300-Mil) SOIC	CY8C27443-24SXI	16 K	256	Yes	–40 °C to +85 °C	8	12	24	12	4	Yes
28-pin (300-Mil) SOIC (Tape and Reel)	CY8C27443-24SXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	24	12	4	Yes
44-pin TQFP	CY8C27543-24AXI	16 K	256	Yes	–40 °C to +85 °C	8	12	40	12	4	Yes
44-pin TQFP (Tape and Reel)	CY8C27543-24AXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	40	12	4	Yes
48-pin (300-Mil) SSOP	CY8C27643-24PVXI	16 K	256	Yes	–40 °C to +85 °C	8	12	44	12	4	Yes
48-pin (300-Mil) SSOP (Tape and Reel)	CY8C27643-24PVXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	44	12	4	Yes
48-pin (7 × 7 × 1 mm) QFN (Sawn)	CY8C27643-24LTXI	16 K	256	Yes	–40 °C to +85 °C	8	12	44	12	4	Yes
48-pin (7 × 7 × 1 mm) QFN (Sawn)	CY8C27643-24LTXIT	16 K	256	Yes	–40 °C to +85 °C	8	12	44	12	4	Yes
56-pin OCD SSOP	CY8C27002-24PVXI[40]	16 K	256	Yes	–40 °C to +85 °C	8	12	44	14	4	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Note
40. This part may be used for in-circuit debugging. It is NOT available for production.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes.

■ **Problem Definition**

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ **Parameters Affected**

The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70°C and within the upper and lower datasheet temperature range is ±5%.

■ **Trigger Condition(s)**

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ± 2.5% when operated beyond the temperature range of 0 to +70 °C.

■ **Scope of Impact**

This problem may affect UART, IrDA, and FSK implementations.

■ **Workaround**

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ **Fix Status**

There are no fixes planned. The workaround listed above should be used.

Not in Production

Part Numbers Affected

Part Number
CY8C27143
CY8C27243
CY8C27443
CY8C27543
CY8C27643

Qualification Status

CY8C27X43 Rev. A – Not in production

Errata Summary

The following table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
1. The Timer Capture Input signal is limited to re-synchronized Row Inputs or Analog Comparator bus inputs when operating over 4.75 V.	All parts affected	A	Fix confirmed in Silicon Rev B
2. The Timer Capture Inputs are limited to re-synchronized Row Inputs when operating at less than 4.75 V.	All parts affected	A	Fix confirmed in Silicon Rev B
3. The I2C_CFG, I2C_SCR, and I2C_MSCR registers have some restrictions as to the CPU frequency that must be in effect when these registers are written.	All parts affected	A	Fix confirmed in Silicon Rev B

1. The Timer Capture Input signal is limited to re-synchronized Row Inputs or Analog Comparator bus inputs when operating over 4.75 V.

■ Problem Definition

When the device is operating at 4.75 V to 5.25 V, the Input Capture signal source for a digital block operating in Timer mode is limited to either a Row Input signal that has been re-synchronized, or an Analog Comparator bus input. The Row Output signals, or the Broadcast clock signals, cannot be used as a source for the Timer Capture signal.

■ Parameters Affected

NA

■ Trigger Condition(S)

Device operating with VCC between 4.75 V to 5.25 V.

■ Scope of Impact

Digital blocks operating in timer mode and user modules relying on the timer's output are affected by this errata element.

■ Workaround

To connect the Input Capture signal to the output of another block in the same row, run the output of that block to a Row Output, then to a Global Output, then back to a Global Input, then a Row Input, where the signal can be resynchronized. When connecting the Input Capture signal to an output of a block in a different row, the connection will naturally follow the path of Global Output, to Global Input, then to Row Input.

■ Fix Status

Fix in silicon rev B

2. The Timer Capture Inputs are limited to re-synchronized Row Inputs when operating at less than 4.75 V.

■ **Problem Definition**

When the device is operating at 3.0 V to 4.75 V, the Input Capture signal source for a digital block operating in Timer mode is limited to a Row Input signal that has been re-synchronized. Maximum width is 16-bits Timer Capture less than 4.75 V. The Row Output signals, Analog Comparator input signals, or the Broadcast Clock signals cannot be used as a source for the Timer Capture signal.

■ **Parameters Affected**

NA

■ **Trigger Condition(S)**

Device operating with VCC between 3.0 V to 4.75 V.

■ **Scope of Impact**

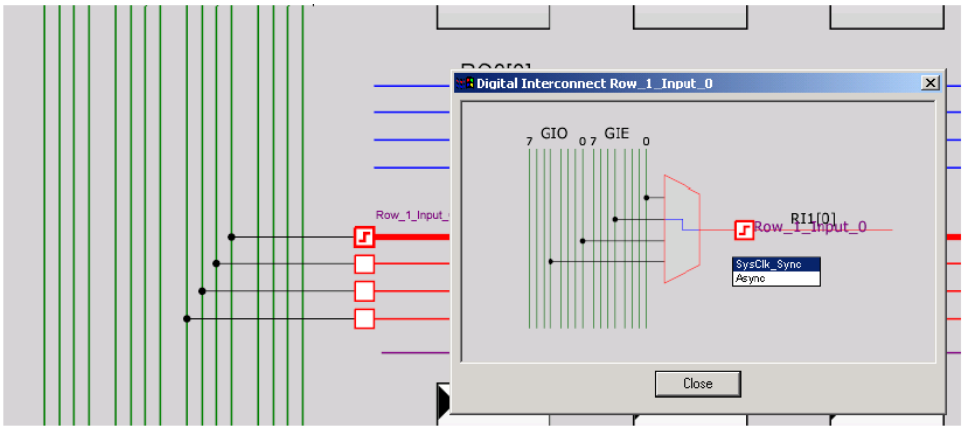
Digital blocks operating in timer mode and user modules relying on the timer's output are affected by this errata element.

■ **Workaround**

To connect the input capture signal to the output of another block, run the output of that block to a row output, then to a global output, back to a global input, then a row input, where the signal can be re-synchronized.

To connect an analog comparator bus signal to an input capture, this signal must be routed to pass through a re-synchronizer. The only way this can be accomplished is to route the analog comparator on an analog output bus to connect with an I/O pin. This will use up the resource of the analog output bus, and even though this bus is designed for analog signals, the digital signal from the Analog Comparator operates correctly when transmitted on this bus. After the signal reaches the pin, it is converted back to a digital signal and is communicated back to the digital array using the global input bus for that pin. To make this connection, the port pin must be setup with the global input bus enabled. To enable this configuration within PSoC Designer™, first turn ON the analog output, and then enable the global input.

Figure 30. Resynchronized



■ **Fix Status**

Fix in silicon rev B

3. The I2C_CFG, I2C_SCR, and I2C_MSCR registers have some restrictions as to the CPU frequency that must be in effect when these registers are written.

■ **Problem Definition**

The CPU frequency must be set to one of the recommended values just prior to a write to these registers and can be immediately set back to the original operating frequency in the instruction just following the register write. A write instruction to these registers occurring at a CPU frequency that is not recommended could result in unpredictable behavior. The table below lists the possible selections of the CPU memory for writes to the I2C_CFG, I2C_SCR, and I2C_MSCR registers, and it highlights the particular settings that are recommended (Rec) and not recommended (NR).

I2C_SCR Write and I2C_MSCR Write	I2C_CFG Write							
	24 MHz	12 MHz	6 MHz	3 MHz	1.5 MHz	375 K	180 K	93 K
24 MHz	NR	NR	NR	NR	NR	NR	NR	NR
12 MHz	NR	NR	Rec	Rec	Rec	Rec	NR	NR
6 MHz	NR	Rec	Rec	NR	NR	Rec	NR	NR
3 MHz	NR	Rec	NR	Rec	Rec	Rec	Rec	Rec
1.5 MHz	NR	Rec	NR	Rec	Rec	Rec	Rec	Rec
375 K	NR	Rec	NR	Rec	Rec	Rec	Rec	Rec
180 K	NR	Rec	NR	Rec	Rec	Rec	Rec	Rec
93 K	NR	Rec	NR	Rec	Rec	Rec	Rec	Rec

■ **Parameters Affected**

NA

■ **Trigger Condition(S)**

See the mentioned table for CPU settings which trigger false writes.

■ **Scope of Impact**

I^2C operation is affected by this Errata element.

■ **Workaround**

The I2CHW User Module is designed to implement the recommended combination of register write frequencies. This user module has a parameter that must be set by users of CY8C27x43 Silicon Revision A devices. When this parameter is set, the user module code temporarily changes the CPU frequency to the recommended values when writing to the affected registers. Users of PSoC Designer should download and install the PSoC Designer 4.1 Service Pack 1 which is available on the web at http://www.cypress.com/psoc.

■ **Fix Status**

Fix in silicon rev B.

Document History Page (continued)

Document Title: CY8C27143/CY8C27243/CY8C27443/CY8C27543/CY8C27643, PSoC® Programmable System-on-Chip™ Document Number: 38-12012				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*P	2899847	NJF / HMI	03/26/10	Added CY8C27643-24LKXI and CY8C27643-24LTXI to Emulation and Programming Accessories on page 52. Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings on page 19. Updated AC electrical specs. Updated Note in Packaging Information on page 44. Updated package diagrams. Updated Thermal Impedances, Solder Reflow Specifications, and Capacitance on Crystal Pins. Removed Third Party Tools and Build a PSoC Emulator into your Board. Updated Ordering Code Definitions on page 54. Updated Ordering Information table. Updated links in Sales, Solutions, and Legal Information.
*Q	2949177	ECU	06/10/2010	Updated content to match current style guide and data sheet template. No technical updates
*R	3032514	NJF	09/17/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*S	3092470	GDK	11/22/10	Removed the following pruned parts from the data sheet. CY8C27643-24LFXIT CY8C27643-24LFXI
*T	3180303	HMI	02/23/2011	Updated Packaging Information.
*U	3378917	GIR	09/28/2011	The text “Pin must be left floating” is included under Description of NC pin in Table 8 on page 14. Updated Table 42 on page 50 for improved clarity. Removed Footnote # 31 and its reference under Table 42 on page 50. Removed inactive part CY8C27643-24LKXI from Table 43 on page 52.
*V	3525102	UVS	02/14/2012	Updated 48-pin sawn QFN package revision. No technical update.
*W	3598316	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*X	3959251	GVH	04/09/2013	Updated Packaging Information: spec 51-85014 – Changed revision from *F to *G. spec 51-85061 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *F to *G. spec 51-85062 – Changed revision from *E to *F. Added Errata.
*Y	3997627	GVH	05/11/2013	Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. Updated Errata.

Document History Page (continued)

Document Title: CY8C27143/CY8C27243/CY8C27443/CY8C27543/CY8C27643, PSoC® Programmable System-on-Chip™ Document Number: 38-12012				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*Z	4066294	GVH	07/17/2013	Added Errata footnotes (Note 1, 2, 3, 26, 27, 29). Updated PSoC Functional Overview: Updated Digital System: Added Note 1, 2 and referred the same notes in “Timers (8- to 32-bit)”. Added Note 3 and referred the same note in “SPI slave and master (up to two)”. Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC Digital Block Specifications: Added Note 26, 27 and referred the same notes in “Timer” parameter. Added Note 29 and referred the same note in “SPIS” parameter. Updated in new template.
AA	4416806	ASRI	07/09/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Removed “Getting Started”. Updated Packaging Information: spec 51-85024 – Changed revision from *E to *F. spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F. Updated Reference Documents: Removed references of spec 001-17397 and spec 001-14503 as these specs are obsolete.
AB	4507916	ASRI	09/19/2014	Updated Errata. Completing Sunset Review.