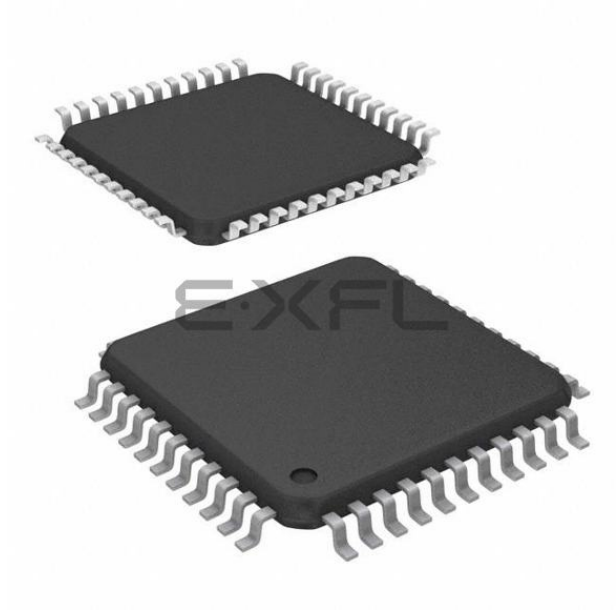

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27543-24axi

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This lets you the optimum choice of system resources for your application. Family resources are shown in the table titled PSoC Device Characteristics on page 6.

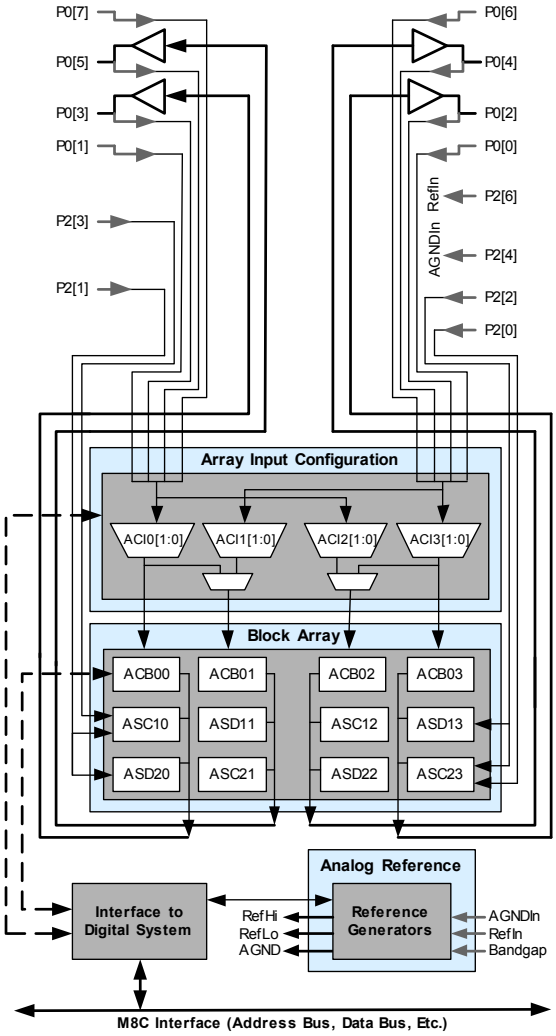
Analog System

The analog system is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are as follows:

- ADCs (up to 4, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band pass, low pass, and notch)
- Amplifiers (up to four, with selectable gain to 48x)
- Instrumentation amplifiers (up to two, with selectable gain to 93x)
- Comparators (up to four, with 16 selectable thresholds)
- DACs (up to four, with 6- to 9-bit resolution)
- Multiplying DACs (up to four, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a core resource)
- 1.3-V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in the following figure.

Figure 3. Analog System Block Diagram



Pinouts

The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, V_{DD}, SMP, and XRES are not capable of Digital I/O.

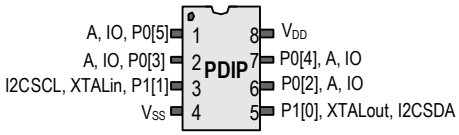
8-pin Part Pinout

Table 2. Pin Definitions – 8-pin PDIP

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I/O	P0[5]	Analog column mux input and column output
2	I/O	I/O	P0[3]	Analog column mux input and column output
3	I/O		P1[1]	Crystal Input (XTALin), I^2C serial clock (SCL), ISSP-SCLK[6]
4	Power		Vss	Ground connection.
5	I/O		P1[0]	Crystal output (XTALout), I^2C serial data (SDA), ISSP-SDATA[6]
6	I/O	I/O	P0[2]	Analog column mux input and column output
7	I/O	I/O	P0[4]	Analog column mux input and column output
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C27143 8-pin PSoC Device



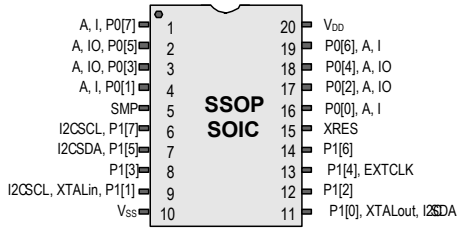
20-pin Part Pinout

Table 3. Pin Definitions – 20-pin SSOP, SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	Switch Mode Pump (SMP) connection to external components required
6	I/O		P1[7]	I^2C Serial Clock (SCL)
7	I/O		P1[5]	I^2C Serial Data (SDA)
8	I/O		P1[3]	
9	I/O		P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[6]
10	Power		Vss	Ground connection.
11	I/O		P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[6]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional external clock input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I/O	P0[2]	Analog column mux input and column output
18	I/O	I/O	P0[4]	Analog column mux input and column output
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C27243 20-pin PSoC Device



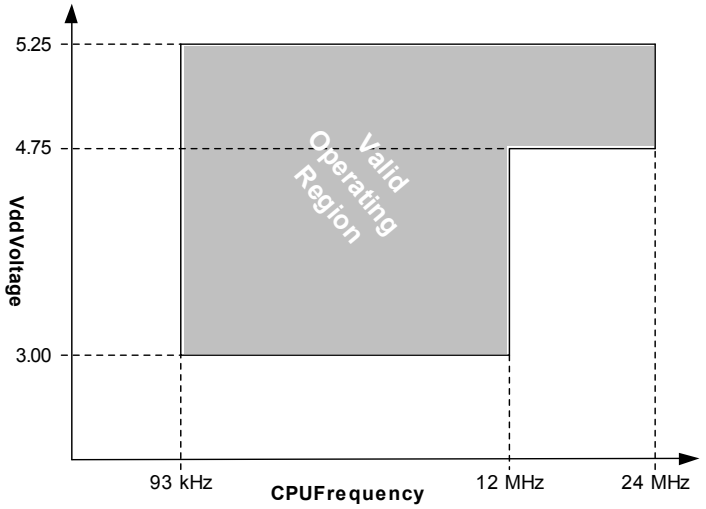
Note
6. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip* Technical Reference Manual for details.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C27x43 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C ≤ T_A ≤ 70 °C and T_J ≤ 82 °C.

Figure 11. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to Vss	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	Vss – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	Vss – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Table 19. 5-V DC Analog Output Buffer Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
I_{SOB}	Supply current including opamp bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
I_{OMAX}	Maximum output current	–	40	–	mA	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

Table 20. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – –	 3.2 3.2 6 6	 20 20 25 25	 mV mV mV mV	High power setting is not recommended.
TCV_{OSOB}	Average input offset voltage drift Power = low, Opamp bias = low Power = low, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – –	 9 9 12 12	 55 55 70 70	 µV/°C µV/°C µV/°C µV/°C	High power setting is not recommended.
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including opamp bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 2 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

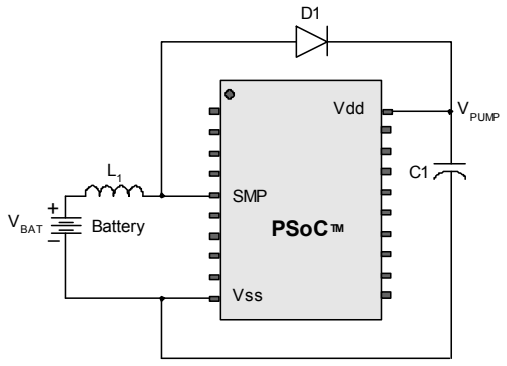
DC Switch Mode Pump Specifications

Table 21 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{PUMP} 5 V	5 V output voltage	4.75	5.0	5.25	V	Configured as in Note 15. Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3 V output voltage	3.00	3.25	3.60	V	Configured as in Note 15. Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	 8 5	 – –	 – –	 mA mA	Configured as in Note 15. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 15. SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 15. SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.1	–	–	V	Configured as in Note 15.
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configured as in Note 15. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 25 on page 33.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configured as in Note 15. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 25 on page 33.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configured as in Note 15. Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configured as in Note 15. Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Figure 12. Basic Switch Mode Pump Circuit



Note
15. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 12.

Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	3.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.657 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 – P2[6]	2.592 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 – P2[6]	2.594 – P2[6]	2.665 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 23. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.225	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.361	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.067	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.35	$V_{DD}/2$ – 1.293	$V_{DD}/2$ – 1.210	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.218	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.370	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.038	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.259	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.221	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.366	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.050	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.046	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.331	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.260	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.295	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.262	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.018	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.055	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 0.086	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.082	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.037	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.054	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.079	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.080	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.042	V

Table 23. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.507	2.598	2.698	V
		V_{AGND}	AGND	Bandgap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.516	2.598	2.683	V
		V_{AGND}	AGND	Bandgap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.510	2.599	2.693	V
		V_{AGND}	AGND	Bandgap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.598	2.683	V
		V_{AGND}	AGND	Bandgap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

Table 24 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Unit
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ
C_{SC}	Capacitor unit value (switch cap)	–	80	–	fF

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 28. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
F_{IMO}	Internal main oscillator (IMO) frequency	23.4	24	24.6[22]	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU frequency (5 V nominal)	0.0914	24	24.6[22]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.0914	12	12.3[23]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	49.2[22, 24]	MHz	Refer to AC Digital Block Specifications on page 40.
F_{24M}	Digital PSoC block frequency	0	24	24.6[24]	MHz	
F_{32K1}	Internal low speed oscillator (ILO) frequency	15	32	64	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
F_{PLL}	PLL frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
$t_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	
$t_{PLLSLEWSLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	
t_{OS}	External crystal oscillator startup to 1%	–	1700	2620	ms	
t_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{24M}	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
$Step_{24M}$	24 MHz trim step size	–	50	–	kHz	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	wer-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
$Fout_{48M}$	48 MHz output frequency	46.8	48.0	49.2[22, 23]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.

Notes
22. 4.75 V < V_{DD} < 5.25 V.
23. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
24. See the individual user module datasheets for information on maximum frequencies for user modules.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 36. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Table 37. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency with CPU clock divide by 1[30]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[31]	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 38. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (Block)	–	30	–	ms	
t_{WRITE}	Flash block write time	–	10	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	V_{DD} > 3.6
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
$t_{ERASEALL}$	Flash erase time (Bulk)	–	95	–	ms	Erase all Blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	80[32]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	160[32]	ms	–40 °C ≤ Tj ≤ 0 °C

Notes
30. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
31. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
32. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

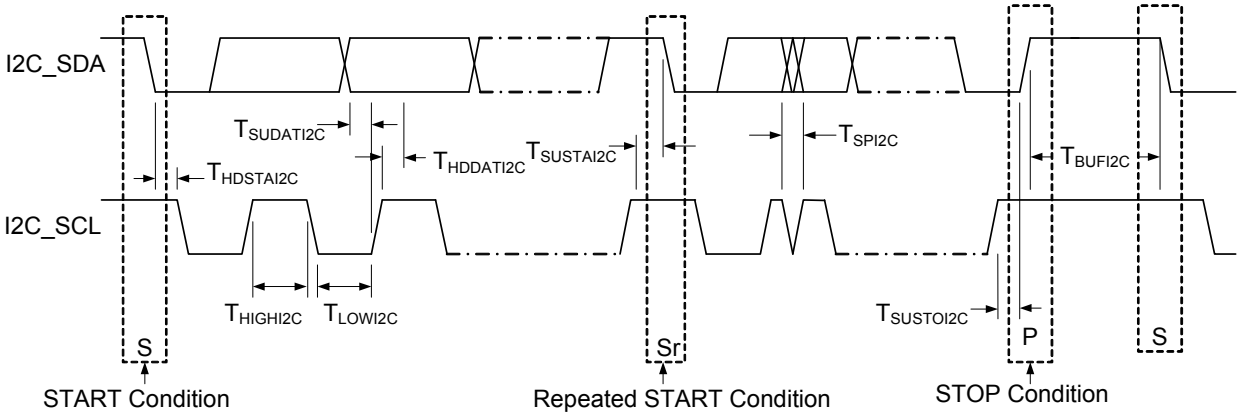
AC I²C Specifications

Table 39 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 39. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Set up time for a repeated start condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data set up time	250	–	100[33]	–	ns
$t_{SUSTOI2C}$	Set up time for stop condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus-free time between a stop and start condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 19. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note
33. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8C27x43 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com/design/MR10161.

Packaging Dimensions

Figure 20. 8-pin (300-Mil) PDIP

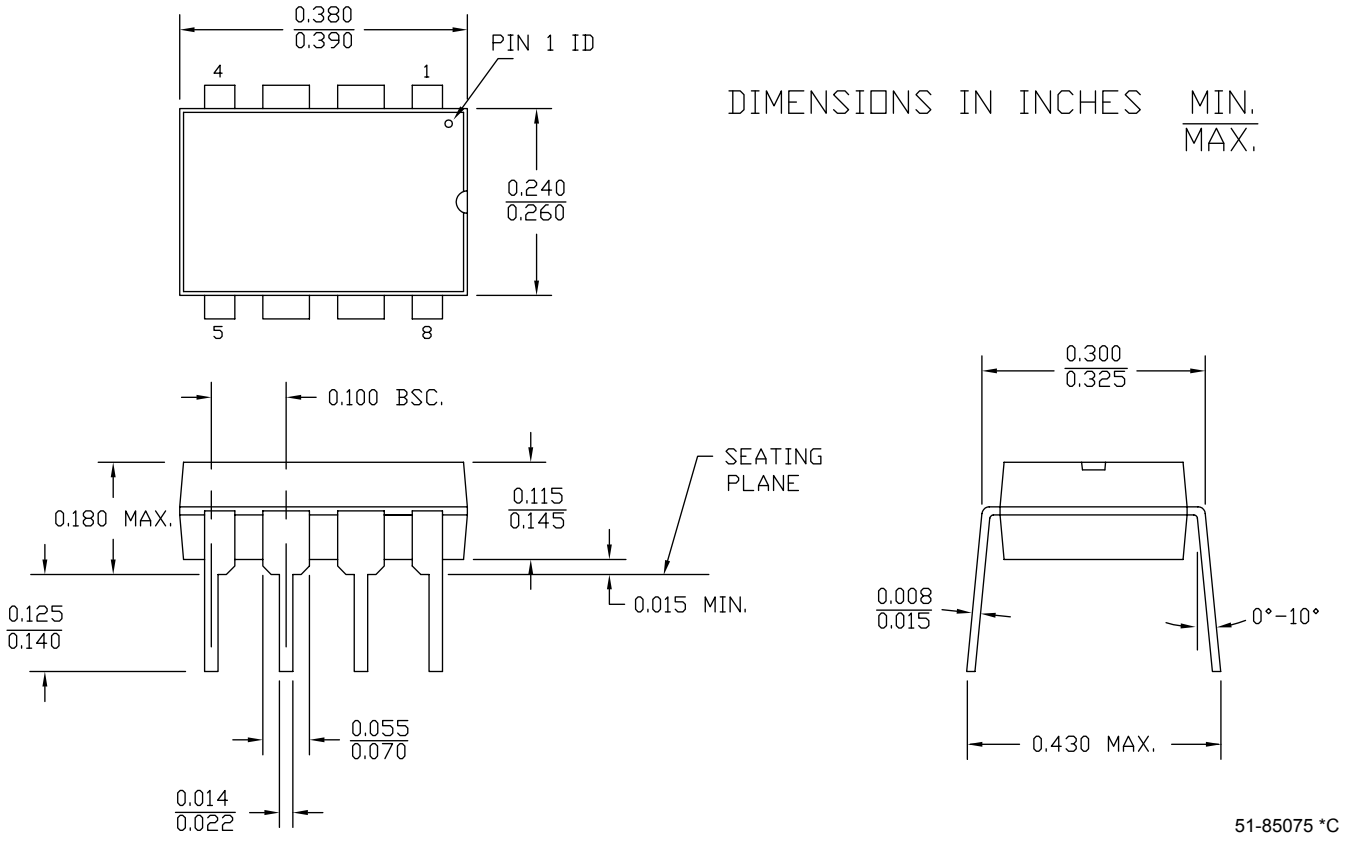


Figure 24. 28-pin (210-Mil) SSOP

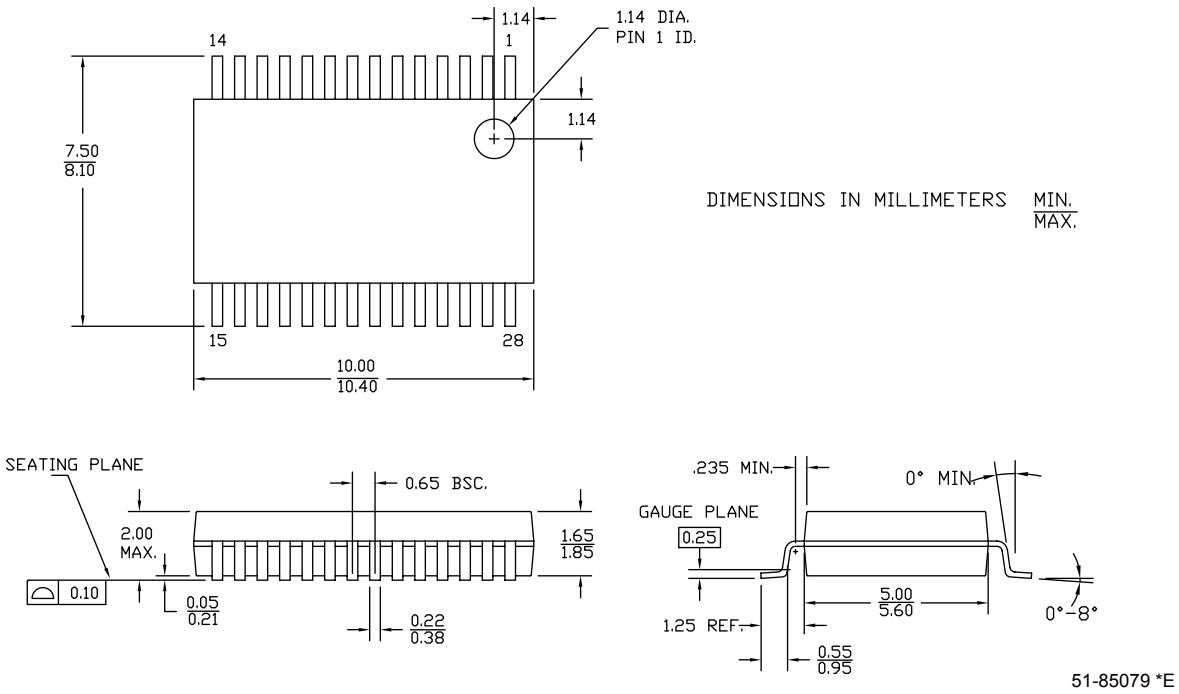


Figure 25. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026

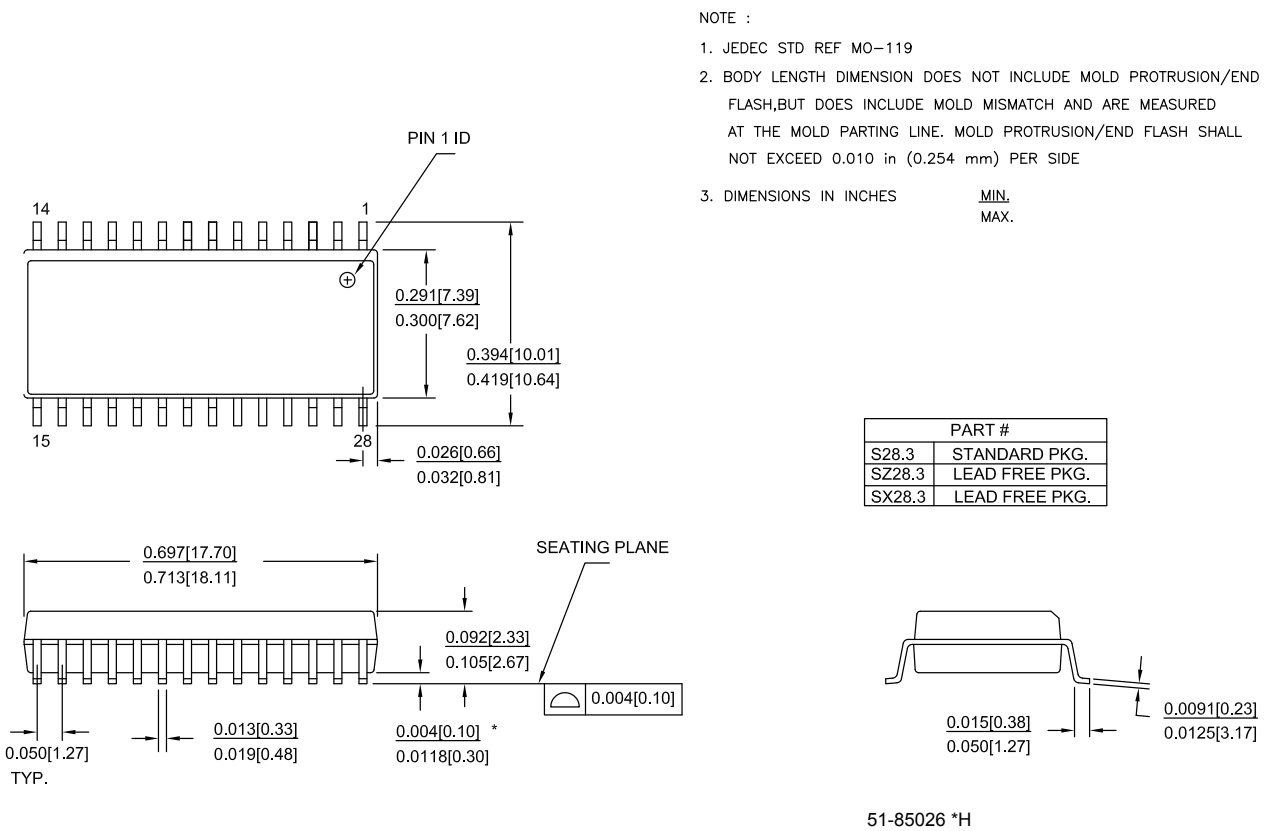


Figure 26. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064

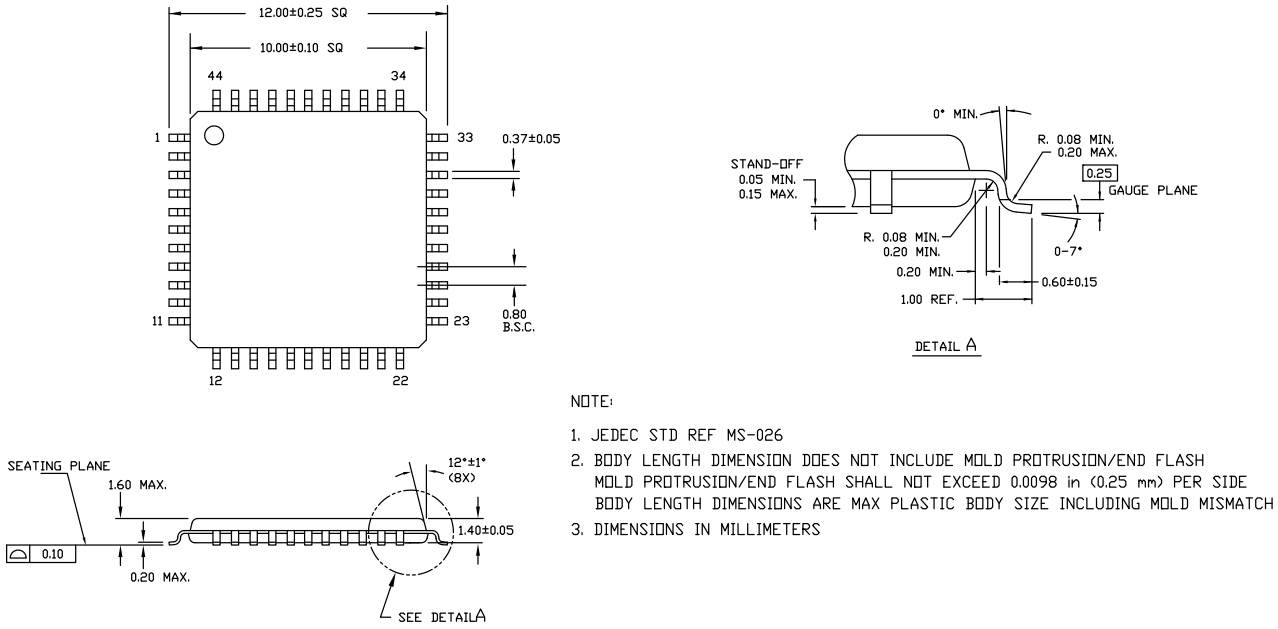


Figure 27. 48-pin (300-Mil) SSOP

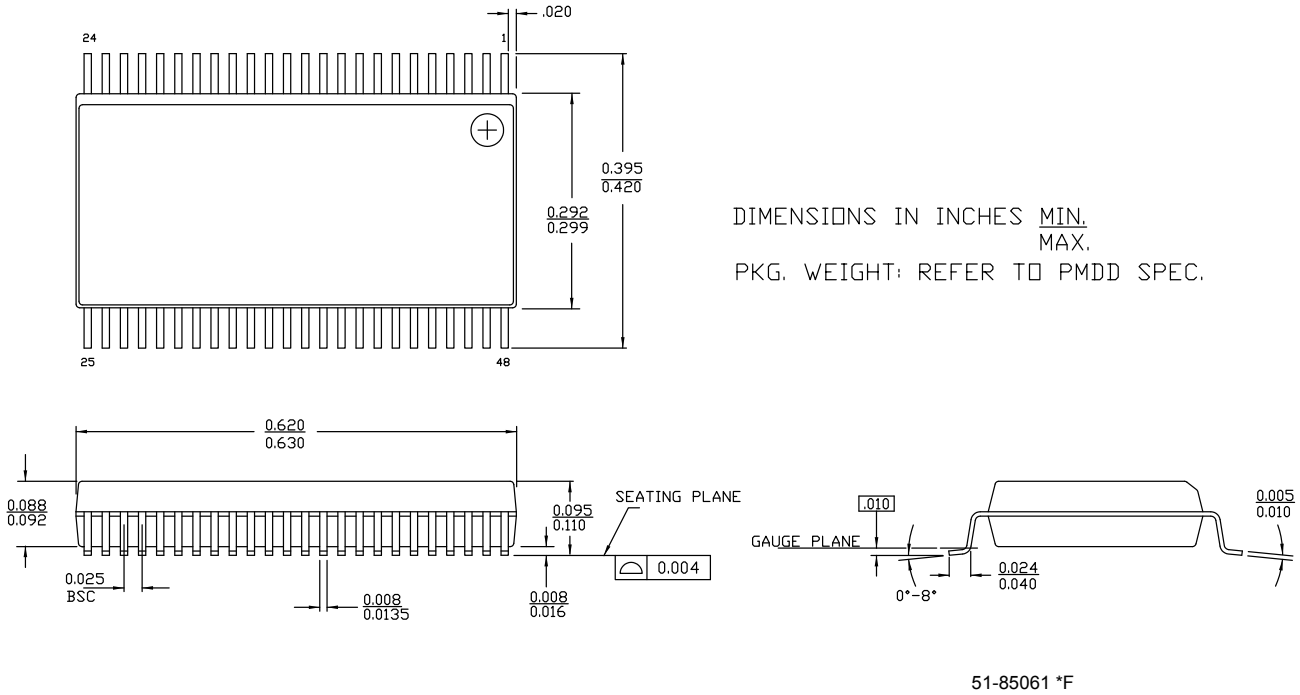
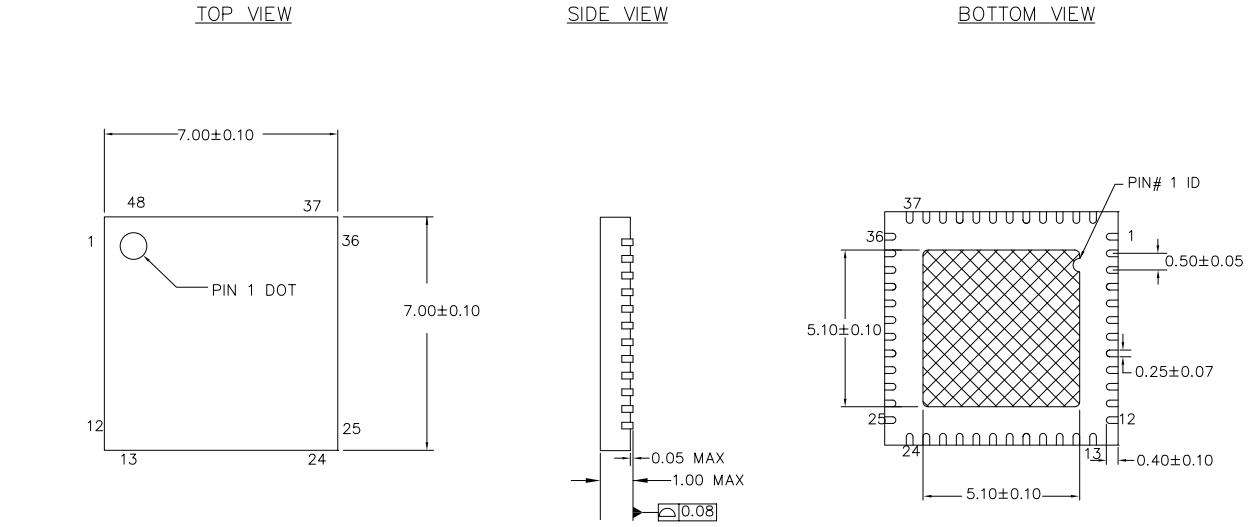


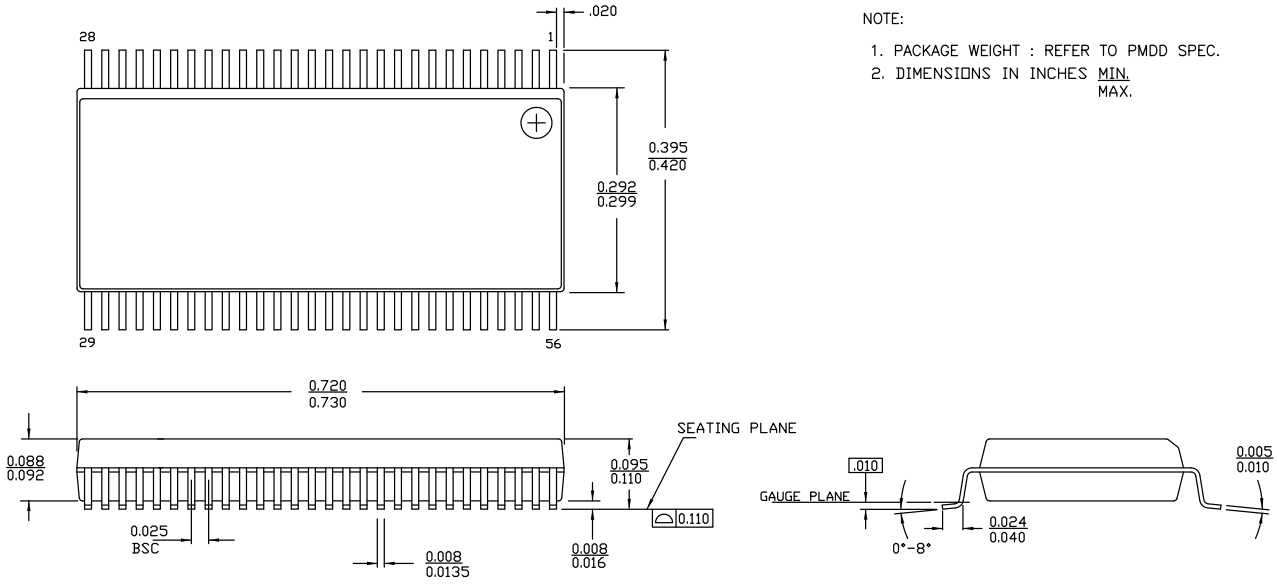
Figure 28. 48-pin QFN 7 × 7 × 1 mm (Sawn Type)



NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *G

Figure 29. 56-pin (300-Mil) SSOP



NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN.
MAX.

51-85062 *F

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes.

■ **Problem Definition**

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ **Parameters Affected**

The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70°C and within the upper and lower datasheet temperature range is ±5%.

■ **Trigger Condition(s)**

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ± 2.5% when operated beyond the temperature range of 0 to +70 °C.

■ **Scope of Impact**

This problem may affect UART, IrDA, and FSK implementations.

■ **Workaround**

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ **Fix Status**

There are no fixes planned. The workaround listed above should be used.

Document History Page (continued)

Document Title: CY8C27143/CY8C27243/CY8C27443/CY8C27543/CY8C27643, PSoC® Programmable System-on-Chip™ Document Number: 38-12012				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*Z	4066294	GVH	07/17/2013	Added Errata footnotes (Note 1, 2, 3, 26, 27, 29). Updated PSoC Functional Overview: Updated Digital System: Added Note 1, 2 and referred the same notes in “Timers (8- to 32-bit)”. Added Note 3 and referred the same note in “SPI slave and master (up to two)”. Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC Digital Block Specifications: Added Note 26, 27 and referred the same notes in “Timer” parameter. Added Note 29 and referred the same note in “SPIS” parameter. Updated in new template.
AA	4416806	ASRI	07/09/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Removed “Getting Started”. Updated Packaging Information: spec 51-85024 – Changed revision from *E to *F. spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F. Updated Reference Documents: Removed references of spec 001-17397 and spec 001-14503 as these specs are obsolete.
AB	4507916	ASRI	09/19/2014	Updated Errata. Completing Sunset Review.