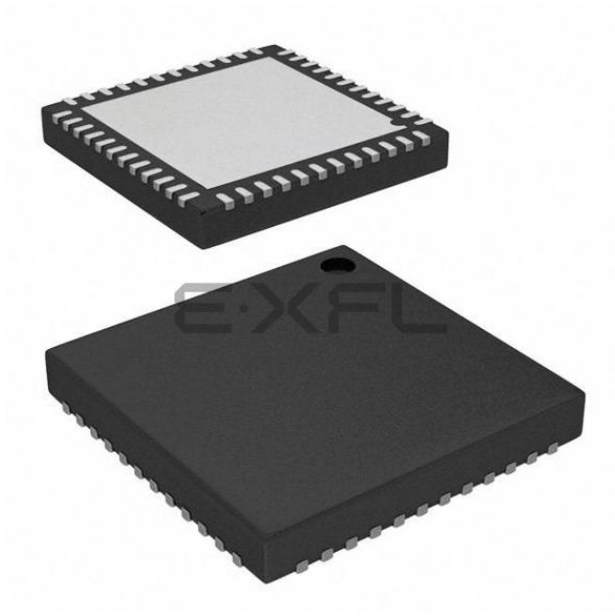

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Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	44
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27643-24ltxi

Contents

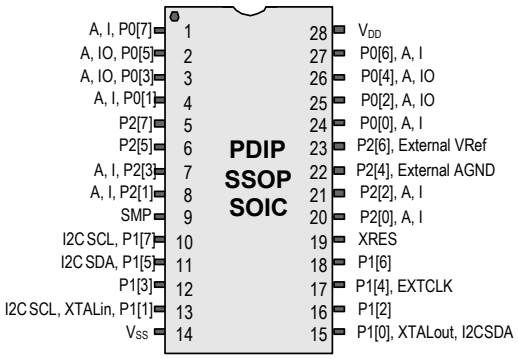
28-pin Part Pinout

Table 4. Pin Definitions – 28-pin PDIP, SSOP, SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		SMP	Switch mode pump (SMP) connection to external components required
10	I/O		P1[7]	I^2C SCL
11	I/O		P1[5]	I^2C SDA
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[7]
14	Power		Vss	Ground connection.
15	I/O		P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[7]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional external clock input (EXTCLK)
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External analog ground (AGND)
23	I/O		P2[6]	External voltage reference (V_{REF})
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I/O	P0[2]	Analog column mux input and column output
26	I/O	I/O	P0[4]	Analog column mux input and column output
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 6. CY8C27443 28-pin PSoC Device



Note
7. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip* Technical Reference Manual for details.

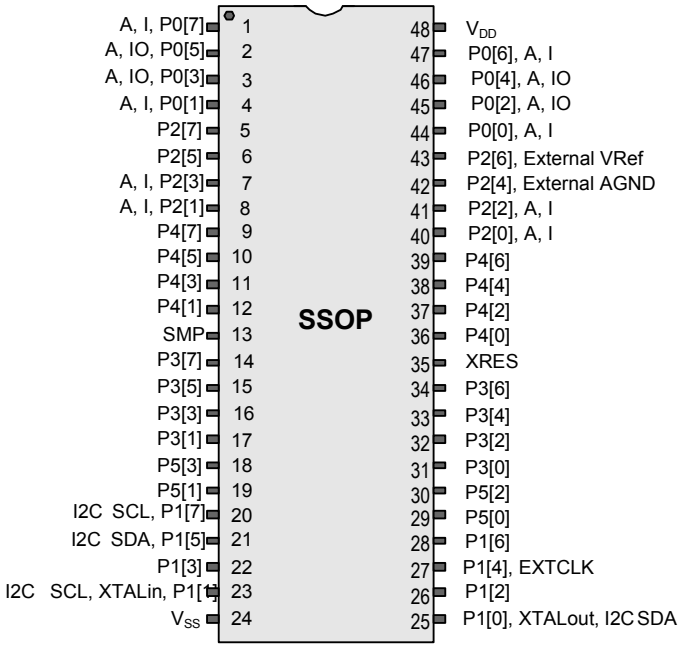
48-pin Part Pinout

Table 6. Pin Definitions – 48-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	I/O		P4[7]	
10	I/O		P4[5]	
11	I/O		P4[3]	
12	I/O		P4[1]	
13	Power		SMP	SMP connection to external components required
14	I/O		P3[7]	
15	I/O		P3[5]	
16	I/O		P3[3]	
17	I/O		P3[1]	
18	I/O		P5[3]	
19	I/O		P5[1]	
20	I/O		P1[7]	I^2C SCL
21	I/O		P1[5]	I^2C SDA
22	I/O		P1[3]	
23	I/O		P1[1]	Crystal Input (XTALin), I^2C SCL, ISSP-SCLK[9]
24	Power		Vss	Ground connection
25	I/O		P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA.[9]
26	I/O		P1[2]	
27	I/O		P1[4]	Optional external clock input (EXTCLK)
28	I/O		P1[6]	
29	I/O		P5[0]	
30	I/O		P5[2]	
31	I/O		P3[0]	
32	I/O		P3[2]	
33	I/O		P3[4]	
34	I/O		P3[6]	
35	Input		XRES	Active high external reset with internal pull down
36	I/O		P4[0]	
37	I/O		P4[2]	
38	I/O		P4[4]	
39	I/O		P4[6]	
40	I/O	I	P2[0]	Direct switched capacitor block input
41	I/O	I	P2[2]	Direct switched capacitor block input
42	I/O		P2[4]	External analog ground (AGND)
43	I/O		P2[6]	External voltage reference (VRef)
44	I/O	I	P0[0]	Analog column mux input
45	I/O	I/O	P0[2]	Analog column mux input and column output
46	I/O	I/O	P0[4]	Analog column mux input and column output
47	I/O	I	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 8. CY8C27643 48-pin PSoC Device



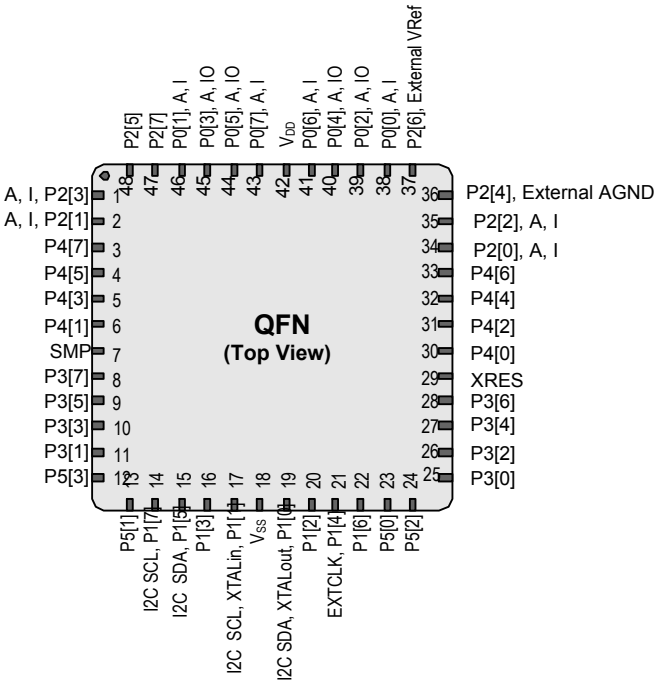
Note
9. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip* Technical Reference Manual for details.

Table 7. Pin Definitions – 48-pin Part Pinout (QFN)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	SMP connection to external components required
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I^2C SCL
15	I/O		P1[5]	I^2C SDA
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[11]
18	Power		Vss	Ground connection.
19	I/O		P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[11]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional external clock input (EXTCLK)
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input
35	I/O	I	P2[2]	Direct switched capacitor block input
36	I/O		P2[4]	External analog ground (AGND)
37	I/O		P2[6]	External voltage reference (V_{REF})
38	I/O	I	P0[0]	Analog column mux input
39	I/O	I/O	P0[2]	Analog column mux input and column output
40	I/O	I/O	P0[4]	Analog column mux input and column output
41	I/O	I	P0[6]	Analog column mux input
42	Power		V_{DD}	Supply voltage
43	I/O	I	P0[7]	Analog column mux input
44	I/O	I/O	P0[5]	Analog column mux input and column output
45	I/O	I/O	P0[3]	Analog column mux input and column output
46	I/O	I	P0[1]	Analog column mux input
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 9. CY8C27643 48-pin PSoC Device[10]



Notes
10. The QFN package has a center pad that must be connected to ground (Vss).
11. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.

56-pin Part Pinout

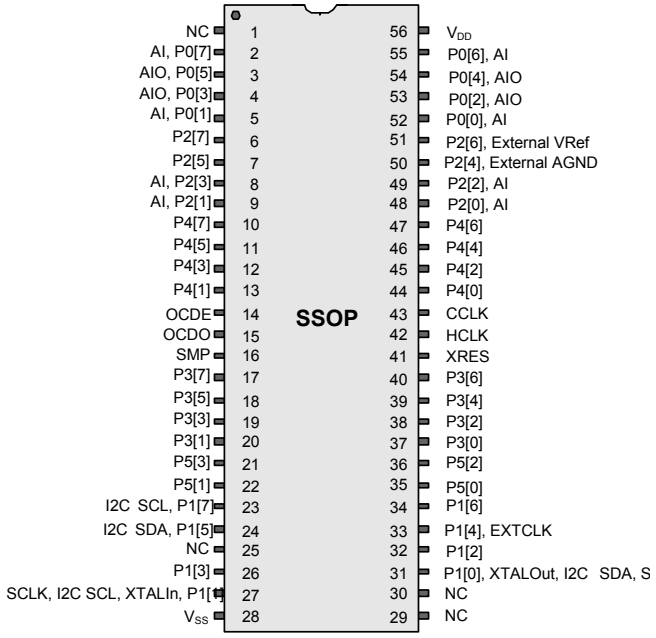
The 56-pin SSOP part is for the CY8C27002 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 8. Pin Definitions – 56-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No connection. Pin must be left floating
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10	I/O		P4[7]	
11	I/O		P4[5]	
12	I/O	I	P4[3]	
13	I/O	I	P4[1]	
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17	I/O		P3[7]	
18	I/O		P3[5]	
19	I/O		P3[3]	
20	I/O		P3[1]	
21	I/O		P5[3]	
22	I/O		P5[1]	
23	I/O		P1[7]	I^2C SCL
24	I/O		P1[5]	I^2C SDA
25			NC	No connection. Pin must be left floating
26	I/O		P1[3]	
27	I/O		P1[1]	Crystal Input (XTALin), I^2C SCL, ISSP-SCLK[12]
28	Power		V_{DD}	Supply voltage
29			NC	No connection. Pin must be left floating
30			NC	No connection. Pin must be left floating
31	I/O		P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[12]
32	I/O		P1[2]	
33	I/O		P1[4]	Optional external clock input (EXTCLK)
34	I/O		P1[6]	
35	I/O		P5[0]	
36	I/O		P5[2]	
37	I/O		P3[0]	
38	I/O		P3[2]	
39	I/O		P3[4]	
40	I/O		P3[6]	

Figure 10. CY8C27002 56-pin PSoC Device



Not for Production

Note
12. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip* Technical Reference Manual for details.

Table 8. Pin Definitions – 56-pin Part Pinout (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
42	OCD		HCLK	OCD high-speed clock output
43	OCD		CCLK	OCD CPU clock output
44	I/O		P4[0]	
45	I/O		P4[2]	
46	I/O		P4[4]	
47	I/O		P4[6]	
48	I/O	I	P2[0]	Direct switched capacitor block input
49	I/O	I	P2[2]	Direct switched capacitor block input
50	I/O		P2[4]	External Analog Ground (AGND)
51	I/O		P2[6]	External Voltage Reference (VRef)
52	I/O	I	P0[0]	Analog column mux input
53	I/O	I	P0[2]	Analog column mux input and column output
54	I/O	I	P0[4]	Analog column mux input and column output
55	I/O	I	P0[6]	Analog column mux input
56	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

Register Reference

This section lists the registers of the CY8C27x43 PSoC device. For detailed register information, see the PSoC Programmable System-on-Chip Technical Reference Manual.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 9. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 10. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW		D0	
PRT4IE	11	RW		51		ASD20CR1	91	RW		D1	
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW		D3	
PRT5DR	14	RW		54		ASC21CR0	94	RW		D4	
PRT5IE	15	RW		55		ASC21CR1	95	RW		D5	
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW		DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 10. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 11. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48		ASC12CR0	88	RW		C8	
PRT2DM1	09	RW		49		ASC12CR1	89	RW		C9	
PRT2IC0	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3DM1	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW		50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54		ASC21CR0	94	RW		D4	
PRT5DM1	15	RW		55		ASC21CR1	95	RW		D5	
PRT5IC0	16	RW		56		ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18			58		ASD22CR0	98	RW		D8	
	19			59		ASD22CR1	99	RW		D9	
	1A			5A		ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C			5C		ASC23CR0	9C	RW		DC	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 16. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$CMRR_{OA}$	Common mode rejection ratio Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 60	 – – –	 – – –	 dB dB dB	Specification is applicable at both High and Low opamp bias.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at High opamp bias. For Low opamp bias mode, minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	60	–	–	dB	$Vss \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 17. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 1.4 1.4 1.4 1.4 1.4 –	 10 10 10 10 10 –	 mV mV mV mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7	40	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1µA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common mode rejection ratio Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 50 50 50	 – – –	 – – –	 dB dB dB	Specification is applicable at Low opamp bias. For High bias mode (except High Power, High opamp bias), minimum is 60 dB.
G_{OLOA}	Open loop gain Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at Low opamp bias. For High opamp bias mode (except High Power, High opamp bias), minimum is 60 dB.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the analog continuous time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 22. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.078	$V_{DD}/2$ – 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.336	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.250	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.056	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.255	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.057	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.337	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.256	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.047	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.258	V

Note
16. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	3.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.657 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 – P2[6]	2.592 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 – P2[6]	2.594 – P2[6]	2.665 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 23. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.225	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.361	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.067	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.35	$V_{DD}/2$ – 1.293	$V_{DD}/2$ – 1.210	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.218	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.370	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.038	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.259	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.221	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.366	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.050	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.046	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.331	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.260	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.295	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.262	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.018	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.055	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 0.086	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.082	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.037	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.054	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.079	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.080	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.042	V

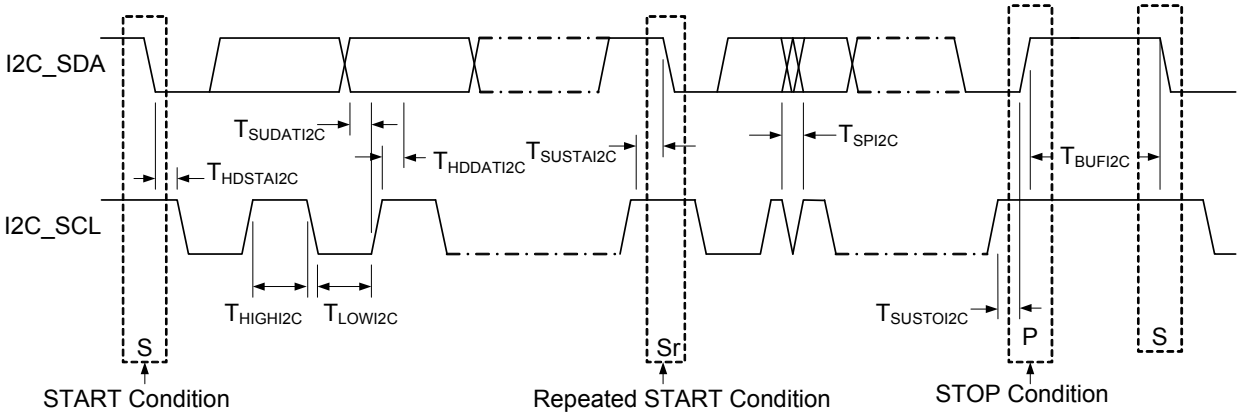
AC I²C Specifications

Table 39 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 39. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Set up time for a repeated start condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data set up time	250	–	100[33]	–	ns
$t_{SUSTOI2C}$	Set up time for stop condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus-free time between a stop and start condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 19. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note
33. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 22. 20-pin SOIC (0.513 × 0.300 × 0.0932 Inches) Package Outline, 51-85024

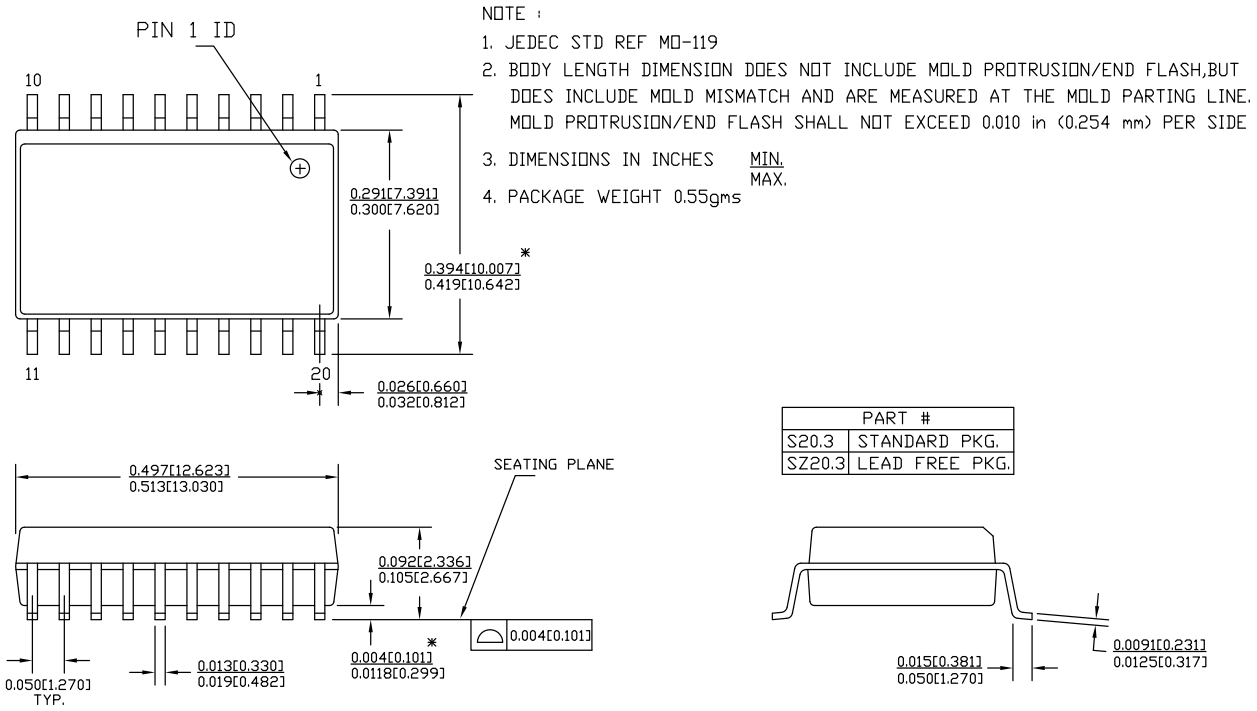


Figure 23. 28-pin (300-Mil) Molded DIP

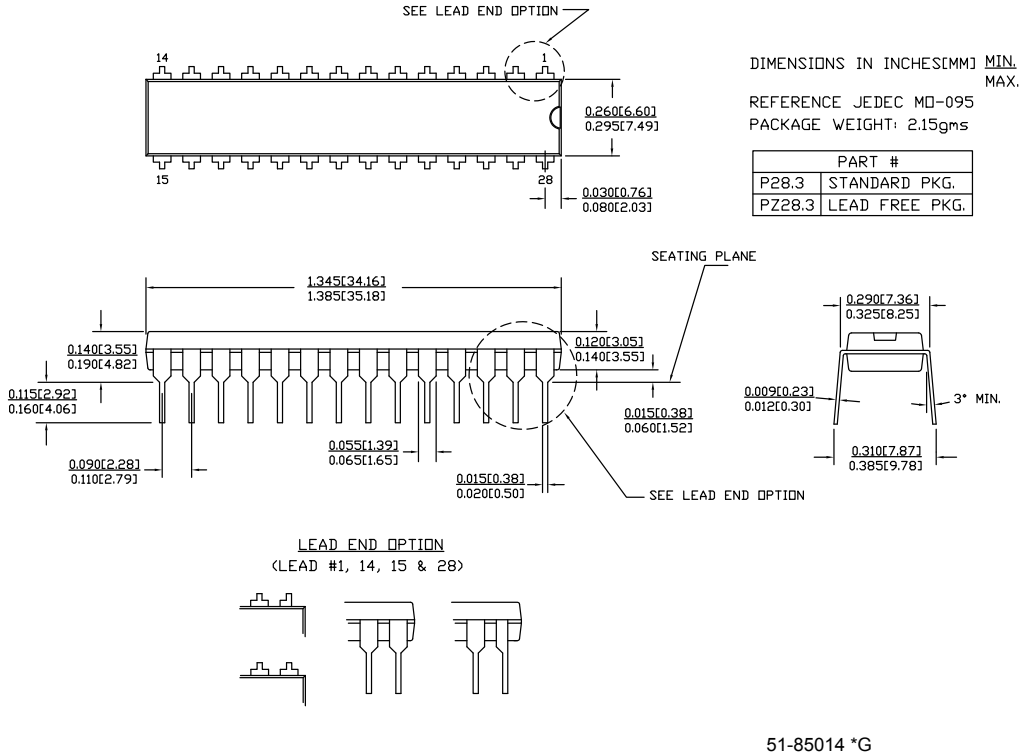


Figure 24. 28-pin (210-Mil) SSOP

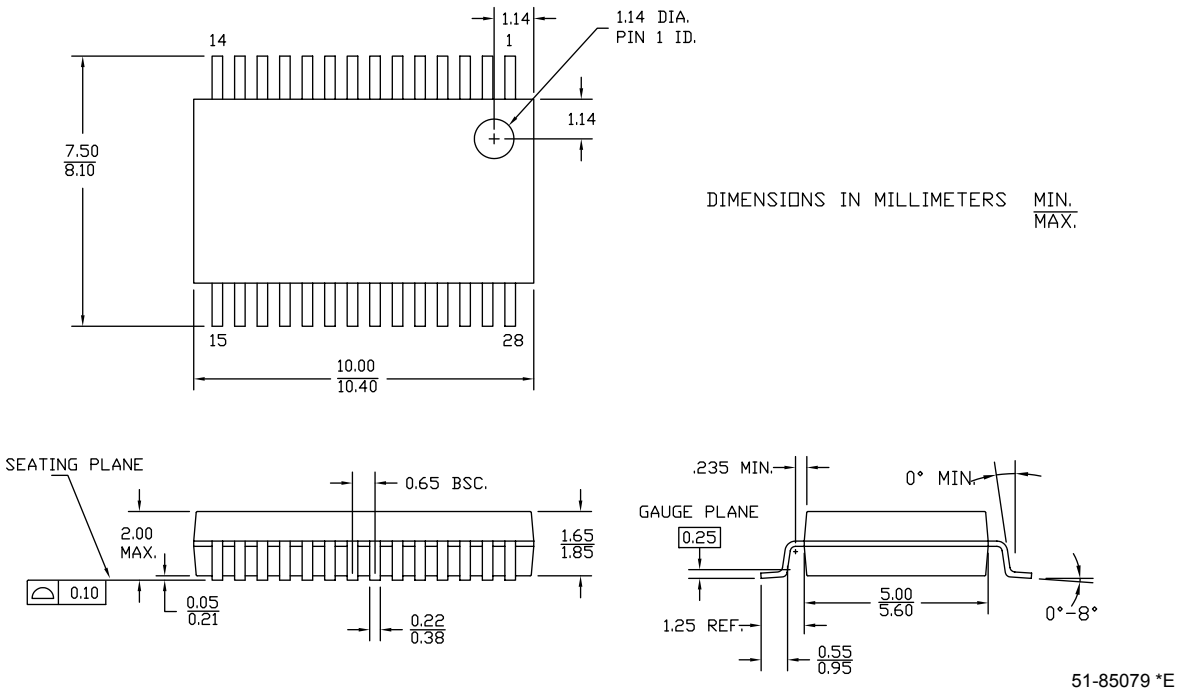


Figure 25. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026

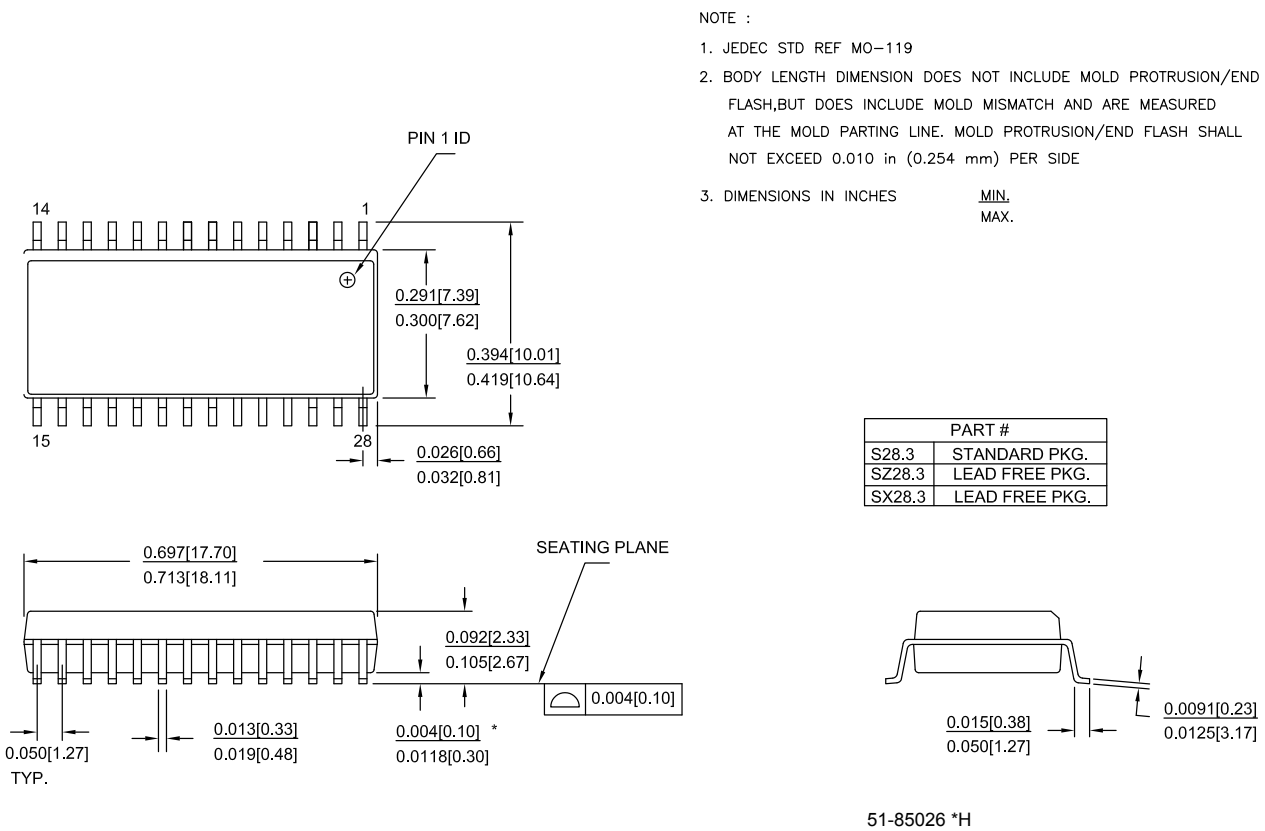


Figure 26. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064

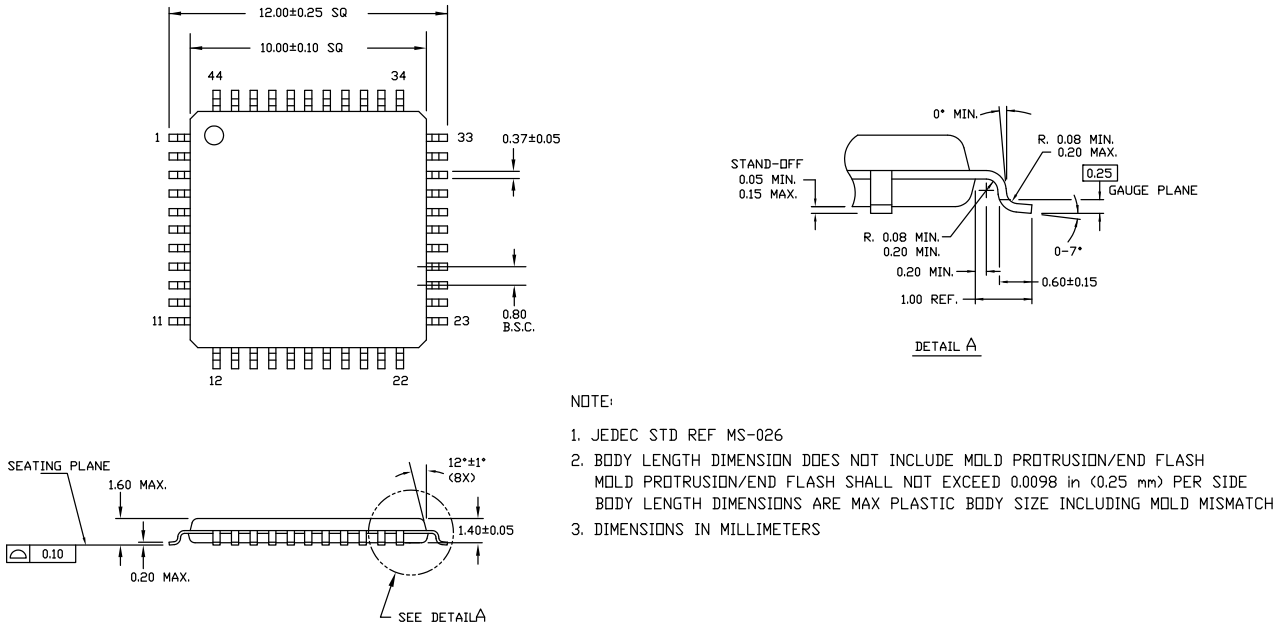


Figure 27. 48-pin (300-Mil) SSOP

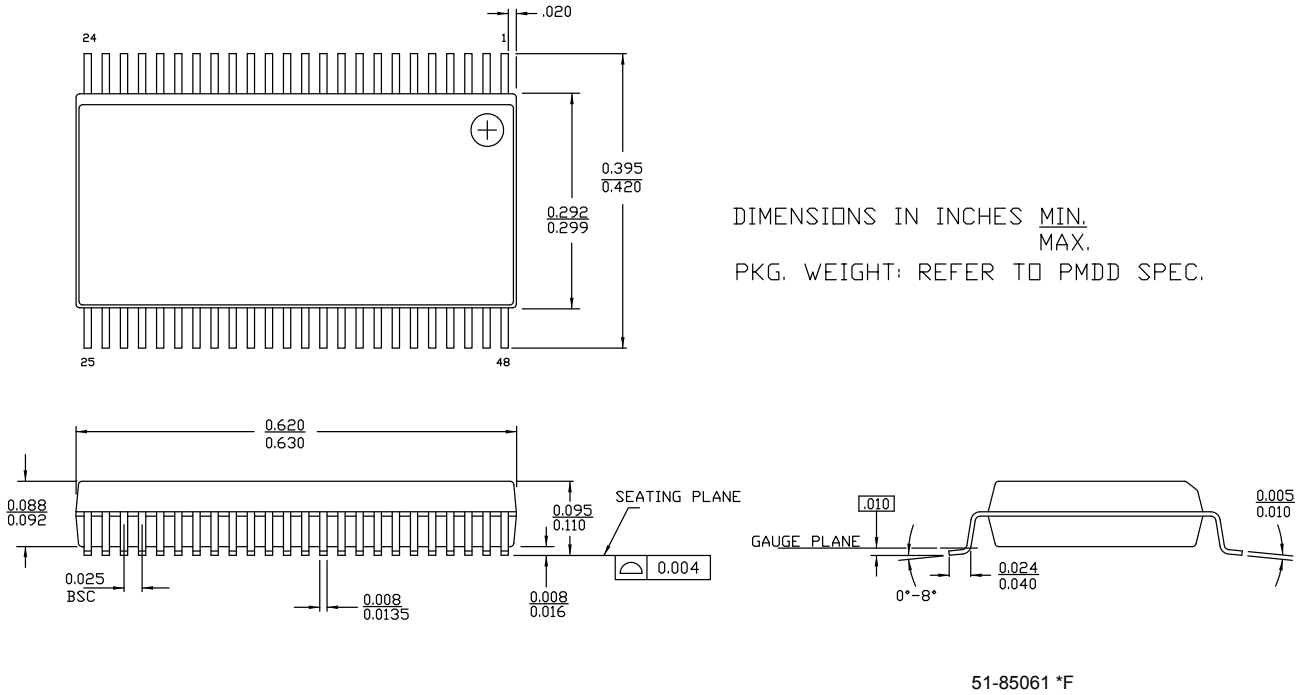
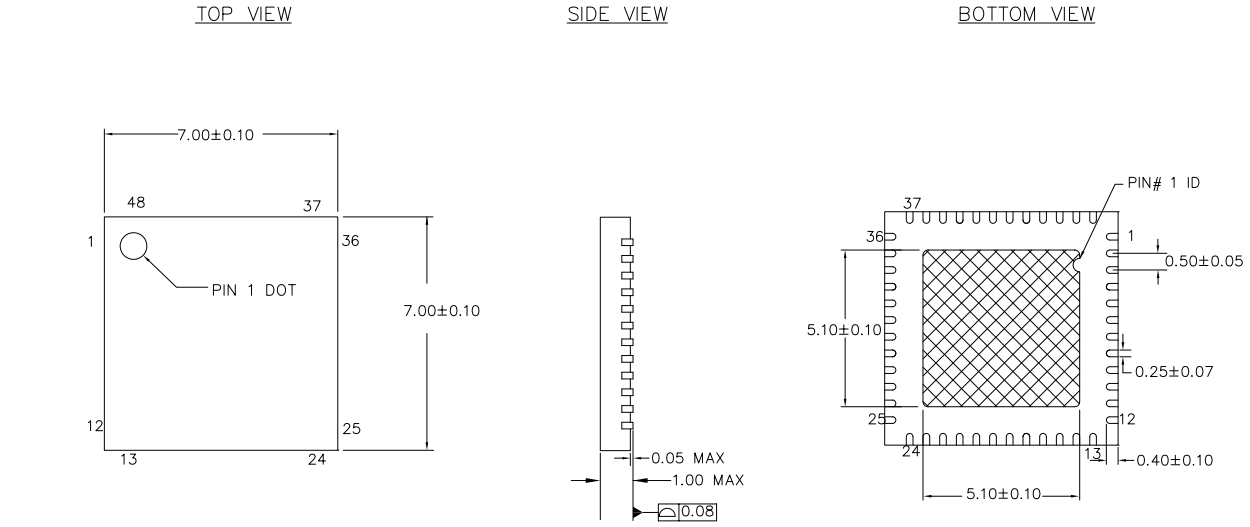


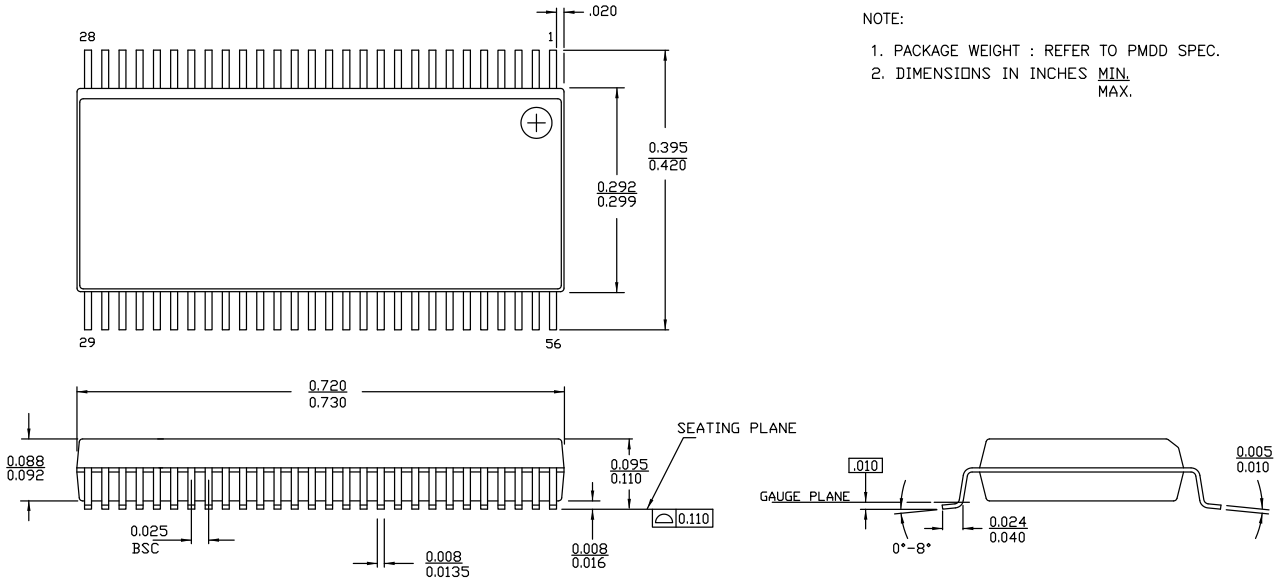
Figure 28. 48-pin QFN 7 × 7 × 1 mm (Sawn Type)



NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *G

Figure 29. 56-pin (300-Mil) SSOP



NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN.
MAX.

51-85062 *F

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Thermal Impedances

Table 40. Thermal Impedances per Package

Package	Typical θ_{JA}[34]
8-pin PDIP	120 °C/W
20-pin SSOP	116 °C/W
20-pin SOIC	79 °C/W
28-pin PDIP	67 °C/W
28-pin SSOP	95 °C/W
28-pin SOIC	68 °C/W
44-pin TQFP	61 °C/W
48-pin SSOP	69 °C/W
48-pin QFN[35]	18 °C/W
56-pin SSOP	47 °C/W

Capacitance on Crystal Pins

Table 41. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8-pin PDIP	2.8 pF
20-pin SSOP	2.6 pF
20-pin SOIC	2.5 pF
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
44-pin TQFP	2.6 pF
48-pin SSOP	3.3 pF
48-pin QFN	2.3 pF
56-pin SSOP	3.3 pF

Solder Reflow Specifications

The following table shows the solder reflow temperature limits that must not be exceeded. Thermap ramp rate should 3 °C or lower.

Table 42. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)[36]	Maximum Time above T_C – 5 °C
8-pin PDIP	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
20-pin SOIC	260 °C	30 seconds
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes
34. $T_J = T_A + POWER \times \theta_{JA}$.
35. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.
36. Refer to Table 44 on page 53.

Document History Page

Document Title: CY8C27143/CY8C27243/CY8C27443/CY8C27543/CY8C27643, PSoC® Programmable System-on-Chip™ Document Number: 38-12012				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
**	127087	New Silicon.	7/01/2003	New document (Revision **).
*A	128780	Engineering and NWJ	7/29/2003	New electrical spec additions, fix of Core Architecture links, corrections to some text, tables, drawings, and format.
*B	128992	NWJ	8/14/2003	Interrupt controller table fixed, refinements to Electrical Spec section and Register chapter.
*C	129283	NWJ	8/28/2003	Significant changes to the Electrical Specifications section.
*D	129442	NWJ	9/09/2003	Changes made to Electrical Spec section. Added 20/28-Lead SOIC packages and pinouts.
*E	130129	NWJ	10/13/2003	Revised document for Silicon Revision A.
*F	130651	NWJ	10/28/2003	Refinements to Electrical Specification section and I2C chapter.
*G	131298	NWJ	11/18/2003	Revisions to GDI, RDI, and Digital Block chapters. Revisions to AC Digital Block Spec and miscellaneous register changes.
*H	229416	SFV	See ECN	New data sheet format and organization. Reference the *PSoC Programmable System-on-Chip Technical Reference Manual* for additional information. Title change.
*I	247529	SFV	See ECN	Added Silicon B information to this data sheet.
*J	355555	HMT	See ECN	Add DS standards, update device table, swap 48-pin SSOP 45 and 46, add Reflow Peak Temp. table. Add new color and logo. Re-add pinout ISSP notation. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications.
*K	523233	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table. Add OCD pinout and package diagram. Add ISSP note to pinout tables. Update package diagram revisions. Update typical and recommended Storage Temperature per industrial specs. Update CY branding and QFN convention. Update copyright and trademarks.
*L	2545030	YARA	07/29/2008	Added note to DC Analog Reference Specification table and Ordering Information.
*M	2696188	DPT / PYRS	04/22/2009	Changed title from “CY8C27143, CY8C27243, CY8C27443, CY8C27543, and CY8C27643 PSoC Mixed Signal Array Final data sheet” to “CY8C27143, CY8C27243, CY8C27443, CY8C27543, CY8C27643 PSoC® Programmable System-on-Chip™”. Updated data sheet template. Added 48-Pin QFN (Sawn) package outline diagram and Ordering information details for CY8C27643-24LTXI and CY8C27643-24LTXIT parts
*N	2762501	MAXK	09/11/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified T_{WRITE} specification. Replaced T_{RAMP} (time) specification with SR_{POWER_UP} (slew rate) specification. Added note [9] to Flash Endurance specification. Added I_{OH}, I_{OL}, DCILO, F32K_U, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications.
*O	2811860	ECU	11/20/2009	Added Contents page. In the Ordering Information table, added 48 Sawn QFN (LTXI) to the Silicon B parts. Updated 28-Pin package drawing (51-85014)

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