Toshiba Semiconductor and Storage - TMP89FS60FG(Z Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TLCS-870
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LED, PWM, WDT
Number of I/O	56
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/toshiba-semiconductor-and-storage/tmp89fs60fg-z

- Trace
- RAM monitor
- Flash memory writing

18. Clock operation mode control circuit : 2 circuit

    Single clock mode / Dual clock mode

19. Low power consumption operation (8 mode)
    - STOP mode:

      Oscillation stops. (Battery/Capacitor back-up.)
    - SLOW1 mode:

      Low power consumption operation using low-frequency clock.(High-frequency clock stop.)
    - SLOW2 mode:

      Low power consumption operation using low-frequency clock.(High-frequency clock oscillate.)
    - IDLE0 mode:

      CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using high frequency clock. Released when the reference time set to TBT has elapsed.
    - IDLE1 mode:

      The CPU stops, and peripherals operate using high frequency clock. Release by interruputs(CPU restarts).
    - IDLE2 mode:

      CPU stops and peripherals operate using high and low frequency clock. Release by interruputs. (CPU restarts).
    - SLEEP0 mode:

      CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using low frequency clock. Released when the reference time set to TBT has elapsed.
    - SLEEP1 mode:

      CPU stops, and peripherals operate using low frequency clock. Release by interruput.(CPU restarts).

20. Wide operation voltage:

    4.3 V to 5.5 V at 8MHz /32.768 kHz
    2.7 V to 5.5 V at 4.2 MHz /32.768 kHz

- When the supply voltage is within the operating voltage range

  When the supply voltage is within the operating voltage range and stable oscillation is achieved, holding the $\overline{\text{RESET}}$ pin Low for 5 [µs] or longer generates a reset. Then, changing the $\overline{\text{RESET}}$ pin level to High starts a warm-up period. Upon completion of the warm-up period, the CPU and peripheral circuits start operating (Figure 2-16).

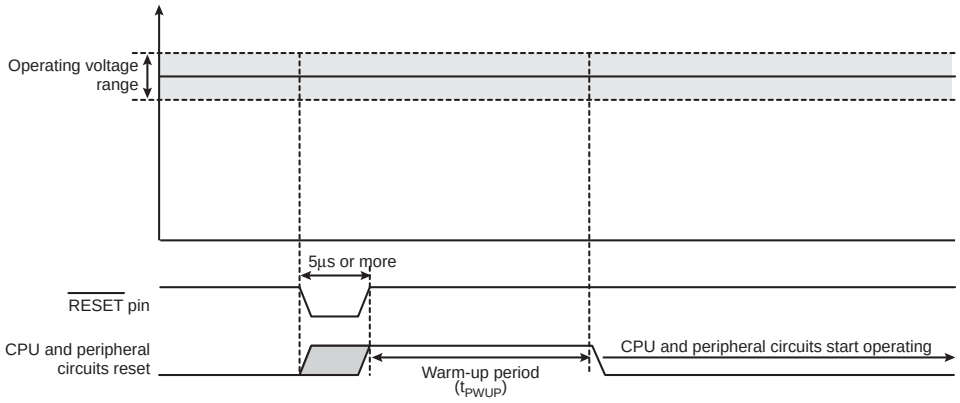


Figure 2-16 External Reset Input (When the Power Supply Is Stable)

2.4.4.3 Voltage detection reset

The voltage detection reset is an internal factor reset that occurs when it is detected that the supply voltage has reached a predetermined detection voltage.

Refer to "Voltage Detection Circuit".

2.4.4.4 Watchdog timer reset

The watchdog timer reset is an internal factor reset that occurs when an overflow of the watchdog timer is detected.

Refer to "Watchdog Timer".

2.4.4.5 System clock reset

The system clock reset is an internal factor reset that occurs when it is detected that the oscillation enable register is set to a combination that puts the CPU into deadlock.

Refer to "Clock Control Circuit".

2.4.4.6 Trimming data reset

The trimming data reset is an internal factor reset that occurs when the trimming data latched in the internal circuit is broken down during operation due to noise or other factors.

The trimming data is a data bit provided for adjustment of the ladder resistor that generates the comparison voltage for the power-on reset and the voltage detection circuits.

This bit is loaded from the non-volatile exclusive use memory during the warm-up time that follows reset release (tPWUP) and latched into the internal circuit.

If the trimming data loaded from the non-volatile exclusive use memory during the warm-up operation that follows reset release is abnormal, IRSTSR<TRMDS> is set to "1".

2. When the watchdog timer reset request signal is selected (when WDCTR<WDTOUT> is "1")

   Setting WDCTR<WDTOUT> to "1" causes a watchdog timer reset request signal to occur when the 8-bit up counter overflows.

   This watchdog timer reset request signal resets the TMP89FS60 and starts the warm-up operation.

5.3.5 Writing the watchdog timer control codes

The watchdog timer control codes are written into WDCDR.

By writing 0x4E (clear code) into WDCDR, the 8-bit up counter is cleared to "0" and continues counting the source clock.

When WDCTR<WDTEN> is "0", writing 0xB1 (disable code) into WDCDR disables the watchdog timer operation.

To prevent the 8-bit up counter from overflowing, clear the 8-bit up counter in a period shorter than the overflow time of the 8-bit up counter and within the clear time.

By designing the program so that no overflow will occur, the program malfunctions and deadlock can be detected through interrupts generated by watchdog timer interrupt request signals.

By applying a reset to the microcomputer using watchdog timer reset request signals, the CPU can be restored from malfunctions and deadlock.

Example: When WDCTR<WDTEN> is "0", set the watchdog timer detection time to 2^{20}/fcgck [s], set the counter clear time to half of the overflow time, and allow a watchdog timer reset request signal to occur if a malfunction is detected.

```
                    LD    (WDCTR), 0y00110011      ;WDTW←10, WDTT←01, WDTOUT←1
Clear the 8-bit up counter at a point after
half of its overflow time and within a period
of the overflow time minus 1 source clock
cycle.
                    LD    (WDCDR), 0x4E            ;Clear the 8-bit up counter
Clear the 8-bit up counter at a point after
half of its overflow time and within a period
of the overflow time minus 1 source clock
cycle.
                    LD    (WDCDR), 0x4E            ;Clear the 8-bit up counter
```

Note: If the overflow of the 8-bit up counter and writing of 0x4E (clear code) into WDCDR occur simultaneously, the 8-bit up counter is cleared preferentially and the overflow detection is not executed.

5.3.6 Reading the 8-bit up counter

The counter value of the 8-bit up counter can be read by reading WDCNT.

The stoppage of the 8-bit up counter can be detected by reading WDCNT at random times and comparing the value to the last read value.

5.3.7 Reading the watchdog timer status

The watchdog timer status can be read at WDST.

WDST<WDTST> is set to "1" when the watchdog timer operation is enabled, and it is cleared to "0" when the watchdog timer operation is disabled.

WDST<WINTST2> is set to "1" when a watchdog timer interrupt request signal occurs due to the overflow of the 8-bit up counter.

7.2 Control

The voltage detection circuit is controlled by voltage detection control registers 1 and 2.

Voltage detection control register 1

VDCR1 (0x0FC6)

	7	6	5	4	3	2	1	0
Bit Symbol	VD2F	VD2SF	VD2LVL		VD1F	VD1SF	VD1LVL	
Read/Write	R/W	Read Only	R/W		R/W	Read Only	R/W	
After reset	0	0	1	0	0	0	0	0

			Read	Write
VD2F	Voltage detection 2 flag (Retains the state when VDD<VD2LVL is detected)	0:	VDD ≥ VD2LVL	Clears VD2F to "0"
		1:	VDD < VD2LVL	-
VD2SF	Voltage detection 2 status flag (Magnitude relation of VDD and VD2LVL when they are read)	0:	VDD ≥ VD2LVL	
		1:	VDD < VD2LVL	
VD2LVL	Selection for detection voltage 2	00:	3.70 +0.2 / -0.2V	
		01:	3.15 +0.15 / -0.15V	
		10:	2.85 +0.15 / -0.15V	
		11:	Reserved	
VD1F	Voltage detection 1 flag (Retains the state when VDD < VD1LVL is detected)		Read	Write
		0:	VDD ≥ VD1LVL	Clears VD1F to "0"
		1:	VDD < VD1LVL	-
VD1SF	Voltage detection 1 status flag (Magnitude relation of VDD and VD1LVL when they are read)	0:	VDD ≥ VD1LVL	
		1:	VDD < VD1LVL	
VD1LVL	Selection for detection voltage 1	00:	4.50 +0.2 / -0.2V	
		01:	4.20 +0.2 / -0.2V	
		10:	3.70 +0.2 / -0.2V	
		11:	3.15 +0.15 / -0.15V	

Note 1: VDCR1 is initialized by a power-on reset or an external reset input.

Note 2: When VD2F or VD1F is cleared by the software and is set due to voltage detection at the same time, the setting due to voltage detection is given priority.

Note 3: VD2F and VD1F cannot be programmed to "1" by the software.

Voltage detection control register 2

VDCR2 (0x0FC7)

	7	6	5	4	3	2	1	0
Bit Symbol	-	-	"0"	"0"	VD2MOD	VD2EN	VD1MOD	VD1EN
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

VD2MOD	Selects the operation mode of voltage detection 2	0:	Generate an INTVLTD interrupt request signal
		1:	Generate a voltage detection reset 2 signal
VD2EN	Enables/disables the operation of voltage detection 2	0:	Disables the operation of voltage detection 2
		1:	Enables the operation of voltage detection 2
VD1MOD	Selects the operation mode of voltage detection 1	0:	Generates an INTVLTD interrupt request signal
		1:	Generates a voltage detection reset signal
VD1EN	Enables/disables the operation of voltage detection 1	0:	Disables the operation of voltage detection 1
		1:	Enables the operation of voltage detection 1

Note 1: VDCR2 is initialized by a power-on reset or an external reset input.

Note 2: Bits 7 and 6 of VDCR2 are read as "0".

Note 3: Bit 5 and 4 of VDCR2 should be cleared to "0".

8.3.3 Port P2 (P27 to P20)

Port P2 is an 8-bit input/output port that can be set to input or output for each bit individually, and it is also used as the serial bus interface input/output, the serial interface input/output, the UART input/output and the on-chip debug function.

The output circuit has the P-channel output control function and either the sink open drain output or the C-MOS output can be selected. Port P2 contains a programmable pull-up resistor on the VDD side. This pull-up resistor can be used when the port is used in the input mode or as a sink open drain output.

When this port is used as the serial bus interface, the serial interface or the UART, setting for serial interface selecting function is also needed. For details, refer to "8.4 Serial Interface Selecting Function".

For the on-chip debug function, refer to the chapter of "On-chip Debug Function (OCD)".

Table 8-8 Port P2

	P27	P26	P25	P24	P23	P22	P21	P20
Secondary function	-	-	SCLK0	SI0 SCL0	SO0 SDA0	SCLK0	SI0 RXD0 OCDIO	SO0 TXD0 OCDCK

10.1 Control

The low power consumption function is controlled by the low power consumption registers (POFFCRn). (n = 0, 1, 2, 3)

Low power consumption register 0

POFFCR0		7	6	5	4	3	2	1	0
(0x0F74)	Bit Symbol	-	-	TC023EN	TC001EN	-	-	TCA1EN	TCA0EN
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0

TC023EN	TC02, 03 control	0 1	Disable Enable
TC001EN	TC00, 01 control	0 1	Disable Enable
TCA1EN	TCA1 control	0 1	Disable Enable
TCA0EN	TCA0 control	0 1	Disable Enable

Low power consumption register 1

POFFCR1		7	6	5	4	3	2	1	0
(0x0F75)	Bit Symbol	-	-	-	SBI0EN	-	UART2EN	UART1EN	UART0EN
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0

SBI0EN	I2C0 control	0 1	Disable Enable
UART2EN	UART2 control	0 1	Disable Enable
UART1EN	UART1 control	0 1	Disable Enable
UART0EN	UART0 control	0 1	Disable Enable

Low power consumption register 2

POFFCR2		7	6	5	4	3	2	1	0
(0x0F76)	Bit Symbol	-	-	RTCEN	-	-	-	SIO1EN	SIO0EN
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0

RTCEN	RTC control	0 1	Disable Enable
SIO1EN	SIO1 control	0 1	Disable Enable
SIO0EN	SIO0 control	0 1	Disable Enable

13.4.6.3 Register buffer configuration

(1) Temporary buffer

The TMP89FS60 contains an 8-bit temporary buffer. When a write instruction is executed on TA0DRAL (TA0DRBL), the data is first stored into this temporary buffer, whether the double buffer is enabled or disabled. Subsequently, when a write instruction is executed on TA0DRAH (TA0DRBH), the set value is stored into the double buffer or TA0DRAH (TA0DRBH). At the same time, the set value in the temporary buffer is stored into the double buffer or TA0DRAL (TA0DRBL). (This structure is designed to enable the set values of the lower-level register and the higher-level register simultaneously.) Therefore, when setting data to TA0DRA (TA0DRB), be sure to write the data into TA0DRAL and TA0DRAH (TA0DRBL and TA0DRBH) in this order.

See Figure 13-1 for the temporary buffer configuration.

(2) Double buffer

In the TMP89FS60, the double buffer can be used by setting TA0CR<TA0DBF>. Setting TA0CR<TA0DBF> to "0" disables the double buffer. Setting TA0CR<TA0DBF> to "1" enables the double buffer.

See Figure 13-1 for the double buffer configuration.

- When the double buffer is enabled

  When a write instruction is executed on TA0DRAH (TA0DRBH) during the timer operation, the set value is first stored into the double buffer, and TA0DRAH/L are not updated immediately. TA0DRAH/L (TA0DRBH/L) compare the last set values to the counter value. If a match is detected, an INTTCA0 interrupt request is generated and the double buffer set value is stored into TA0DRAH/L (TA0DRBH/L). Subsequently, the match detection is executed using a new set value.

  When a read instruction is executed on TA0DRAH/L (TA0DRBH/L), the double buffer value (the last set value) is read, not the TA0DRAH/L (TA0DRBH/L) values (the current effective values).

  When a write instruction is executed on TA0DRAH/L (TA0DRBH/L) while the timer is stopped, the set value is immediately stored into both the double buffer and TA0DRAH/L (TA0DRBH/L).

- When the double buffer is disabled

  When a write instruction is executed on TA0DRAH (TA0DRBH) during the timer operation, the set value is immediately stored in TA0DRAH/L (TA0DRBH/L). Subsequently, the match detection is executed using a new set value.

  If the values set to TA0DRAH/L (TA0DRBH/L) are smaller than the up counter value, the up counter overflows and the match detection is executed using a new set value. As a result, the output pulse width may be longer than the set time. If that is a problem, enable the double buffer.

  When a write instruction is executed on TA0DRAH/L (TA0DRBH/L) while the timer is stopped, the set value is immediately stored into TA0DRAH/L (TA0DRBH/L).

14.4.4.2 Operation

Setting T001CR<T00RUN> to "1" allows the up counter to increment based on the selected source clock. When a match between the internal up counter value and the value set to T00PWM is detected, the output of the $\overline{\text{PPG0}}$ pin is reversed. When T00MOD<TFF0> is "0", the $\overline{\text{PPG0}}$ pin changes from the "L" to "H" level. When T00MOD<TFF0> is "1", the $\overline{\text{PPG0}}$ pin changes from the "H" to "L" level.

Subsequently, the up counter continues counting up. When a match between the up counter value and T00REG is detected, the output of the $\overline{\text{PPG0}}$ pin is reversed again. When T00MOD<TFF0> is "0", the $\overline{\text{PPG0}}$ pin changes from the "H" to "L" level. When T00MOD<TFF0> is "1", the $\overline{\text{PPG0}}$ pin changes from the "L" to "H" level. At this time, an INTTC00 interrupt request is generated.

When T001CR<T00RUN> is set to "0" during the operation, the up counter is stopped and cleared to "0x00". The $\overline{\text{PPG0}}$ pin returns to the level selected at T00MOD<TFF0>.

14.4.4.3 Double buffer

The double buffer can be used for T00PWM and T00REG by setting T00MOD<DBE0>. The double buffer is disabled by setting T00MOD<DBE0> to "0" or enabled by setting T00MOD<DBE0> to "1".

- When the double buffer is enabled

  When a write instruction is executed on T00PWM (T00REG) during the timer operation, the set value is first stored in the double buffer, and T00PWM (T00REG) is not updated immediately. T00PWM (T00REG) compares the previous set value with the up counter value. When an INTTC00 interrupt request is generated, the double buffer set value is stored in T00PWM (T00REG). Subsequently, the match detection is executed using a new set value.

  When a read instruction is executed on T00PWM (T00REG), the value in the double buffer (the last set value) is read out, not the T00PWM (T00REG) value (the currently effective value).

  When a write instruction is executed on T00PWM (T00REG) while the timer is stopped, the set value is immediately stored in both the double buffer and T00PWM (T00REG).

- When the double buffer is disabled

  When a write instruction is executed on T00PWM (T00REG) during the timer operation, the set value is immediately stored in T00PWM (T00REG). Subsequently, the match detection is executed using a new set value. If the value set to T00PWM (T00REG) is smaller than the up counter value, the $\overline{\text{PPG0}}$ pin is not reversed until the up counter overflows and a match detection is executed using a new set value. If the value set to T00PWM (T00REG) is equal to the up counter value, the match detection is executed immediately after data is written into T00PWM (T00REG). Therefore, the timing of changing the $\overline{\text{PPG0}}$ pin may not be an integral multiple of the source clock (Figure 14-10). If these are problems, enable the double buffer.

  When a write instruction is executed on T00PWM (T00REG) while the timer is stopped, the set value is immediately stored in T00PWM (T00REG).

interval may be longer than the selected time. If the value set to T01+00REG is equal to the up counter value, the match detection is executed immediately after data is written into T01+00REG. Therefore, the interrupt request interval may not be an integral multiple of the source clock. If these are problems, enable the double buffer.

When write instructions are executed on T00REG and T01REG in this order while the timer is stopped, the set value is immediately stored in T01+00REG.

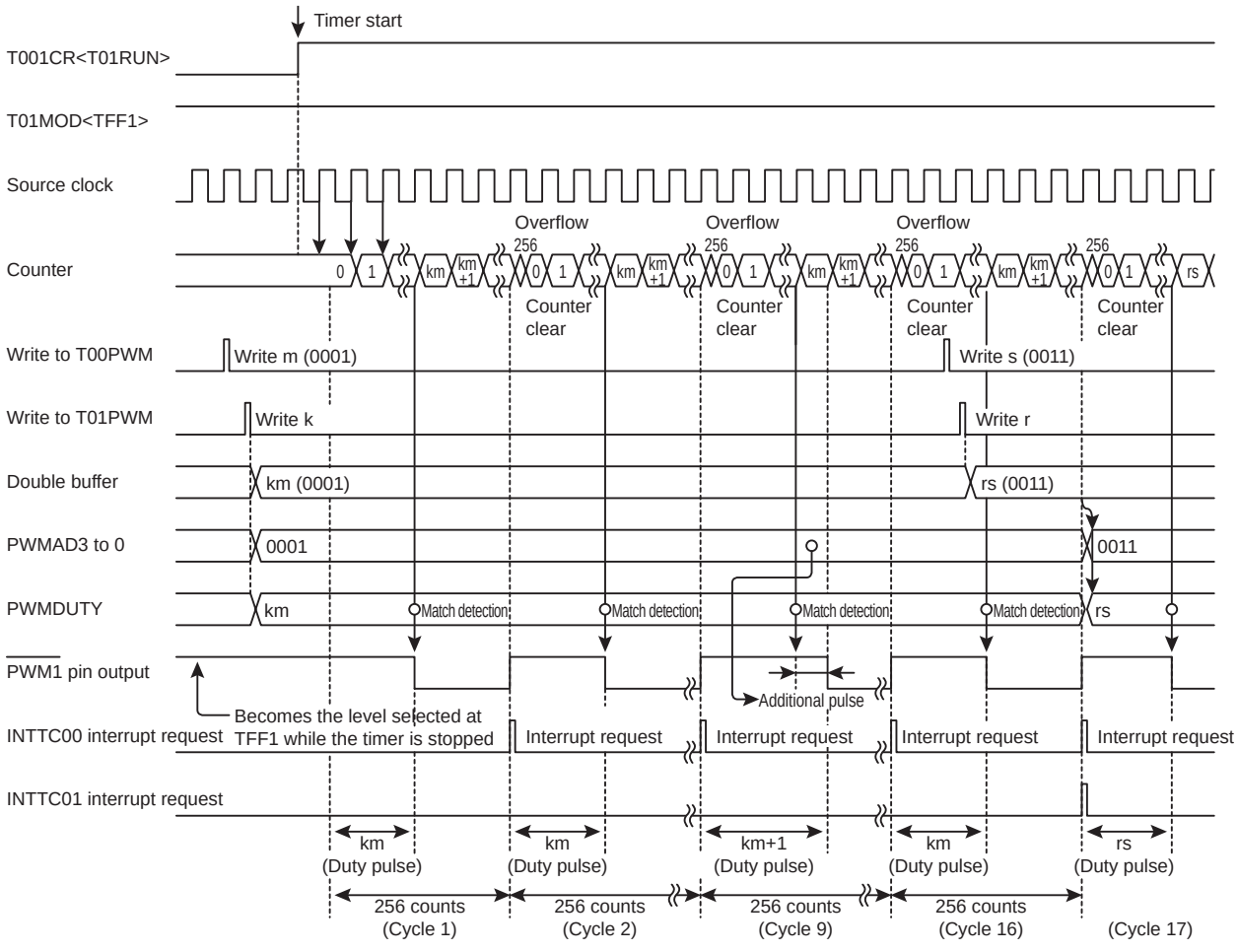
When a read instruction is executed on T01+00REG, the last value written into T01+00REG is read out, regardless of the T00MOD<DBE1> setting.

(Example) Operate TC00 and TC01 in the 16-bit timer mode with the operation clock of fcgck/2 [Hz] and generate interrupts at 96 μs intervals (fcgck = 8 MHz)

```
LD      (POFFCR0),0x10      ; Sets TC001EN to "1"
DI                          ; Sets the interrupt master enable flag to "disable"
SET     (EIRH).4            ; Sets the INTTC00 interrupt enable register to "1"
EI                          ; Sets the interrupt master enable flag to "enable"
LD      (T01MOD),0xF0       ; Selects the 16-bit timer mode and fcgck/2
LD      (T00REG),0x80       ; Sets the timer register (96μs / (2/fcgck) = 0x180)
LD      (T01REG),0x01       ; Sets the timer register
LD      (T001CR),0x06       ; Starts TC00 and TC001 (16-bit mode)
```

(Example) Operate TC00 and TC01 in the 12-bit PWM mode with the operation clock of fcgck/2 and output a duty pulse nearly equivalent to 14.0625 µs in 64µs cycles (fcgck = 8 MHz)
(Actually, output a duty pulse of 225 µs in total in 16 cycles (1024 µs))

```
SET     (P7FC).1          ; Sets P7FC1 to "1"
SET     (P7CR).1          ; Sets P7CR1 to "1"
LD      (POFFCR0),0x10    ; Sets TC001EN to "1"
DI                        ; Sets the interrupt master enable flag to "disable"
SET     (EIRH).4          ; Sets the INTTC00 interrupt enable register to "1"
EI                        ; Sets the interrupt master enable flag to "enable"
LD      (T01MOD),0xF2     ; Selects the 12-bit PWM mode and fcgck/2
LD      (T00PWM),0x84     ; Sets the timer register (duty pulse)
                          ; (14.0625µs × 16) / (2/fcgck) = 0x384
LD      (T01PWM),0x03     ; Sets the timer register (duty pulse)
LD      (T001CR),0x06     ; Starts TC00 and TC01
```



When the double buffer is enabled (T01MOD<DBE1>="1")

Figure 14-15 12-bit PWM Mode Timing Chart

14.5 Revision History

Rev	Description
RA003	Revised interrupt name from "INTT00" and "INTT01" to "INTTC00" and "INTTC01". Added upper bar to PWM and PPG label.
RA004	"14.4.3 8-bit pulse width modulation (PWM) output mode" Revised Exsample program.
	"Figure 14-15 12-bit PWM Mode Timing Chart" Revised each item name.
RA005	"Figure 14-1 8-bit Timer Counters 00 and 01" Revised source clock from "fc" to "fcgck". "14.4.7 12-bit pulse width modulation (PWM) output mode" Revised Example program.

When the subsequent data is written into SIO0BUF, SIO0SR<SEF> is set to "1", the SCLK0 pin outputs the serial clock, and the transmit operation is restarted. An INTSIO0 interrupt request is generated at the restart of the transmit operation.

(2) When an external clock is used and SIO0SR<TBFL> is "0"

When the data transmission is completed, the SO pin keeps last output value. When an external serial clock is input to the SCLK0 pin after completion of the data transmission, an undefined value is transmitted and the transmit underrun error flag SIO0SR<UERR> is set to "1".

If a transmit underrun error occurs, data must not be written to SIO0BUF during the transmission of an undefined value. (It is recommended to finish the transmit operation by setting SIO0CR<SIOS> to "0" or force the transmit operation to stop by setting SIO0CR<SIOM> to "00".)

The transmit underrun error flag SIO0SR<UERR> is cleared by reading SIO0SR.

(3) When an internal or external clock is used and SIO0SR<TBFL> is "1"

When the data transmission is completed, SIO0SR<TBFL> is cleared to "0". The data in SIO0BUF is transferred to the shift register and the transmission of subsequent data is started. At this time, SIO0SR<SEF> is set to "1" and an INTSIO0 interrupt request is generated.

17.5.1.5 Stopping the transmit operation

Set SIO0CR<SIOS> to "0" to stop the transmit operation. When SIO0SR<SEF> is "0", or when the shift operation is not in progress, the transmit operation is stopped immediately and an INTSIO0 interrupt request is generated. When SIO0SR<SEF> is "1", the transmit operation is stopped after all the data in the shift register is transmitted (reserved stop). At this time, an INTSIO0 interrupt request is generated again.

When the transmit operation is completed, SIO0SR<SIOF, SEF and TBFL> are cleared to "0". Other SIO0SR registers keep their values.

If the internal clock has been used, the SO0 pin automatically returns to the "H" level. If an external clock has been used, the SO0 pin keeps the last output value. To return the SO0 pin to the "H" level, write "00" to SIO0CR<SIOM> when the operation is stopped.

The transmit operation can be forced to stop by setting SIO0CR<SIOM> to "00" during the operation. By setting SIO0CR<SIOM> to "00", SIO0CR<SIOS> and SIO0SR are cleared to "0" and the SIO stops the operation, regardless of the SIO0SR<SEF> value. The SO0 pin becomes the "H" level. If the internal clock is selected, the SCLK0 pin returns to the initial level.

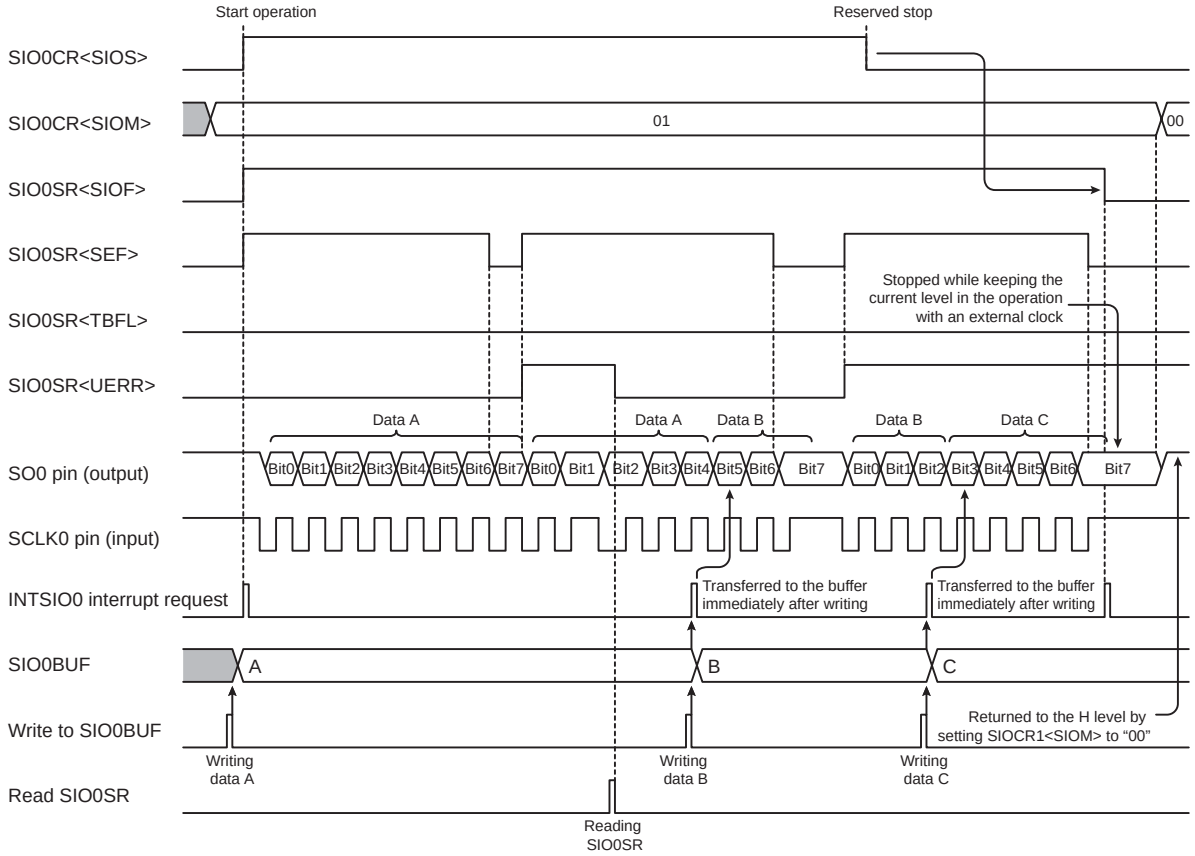


Figure 17-8 8-bit Transmit Mode (External Clock and Occurrence of Transmit Underrun Error)

In the acknowledgment mode, the master device generates the clocks that correspond to the number of data bits, generates the clocks for an acknowledge signal, and generates an interrupt request.

The slave device counts the clocks that correspond to the data bits, counts the clocks for an acknowledge signal, and generates an interrupt request.

The non-acknowledgment mode is activated by setting SBI0CR1<ACK> to "0".

In the non-acknowledgment mode, the master device generates the clocks that correspond to the number of data bits, and generates an interrupt request.

The slave device counts the clocks that correspond to the data bits, and generates an interrupt request.

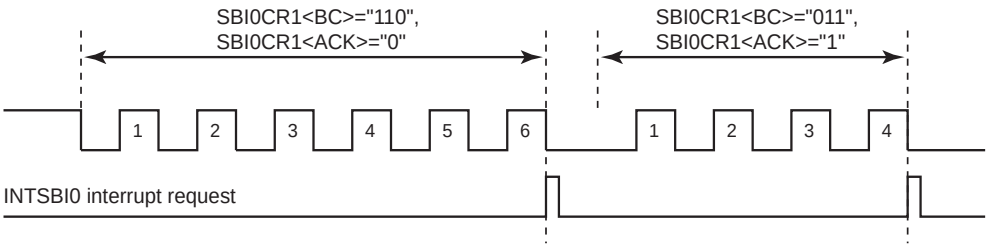


Figure 18-5 Number of Clocks for Data Transfer and SBI0CR1<BC> and SBI0CR1<ACK>

The relationship between the number of clocks for data transfer and SBI0CR1<BC> and SBI0CR1<ACK> is shown in Table 18-1.

Table 18-1 Relationship between the Number of Clocks for Data Transfer and SBI0CR1<BC> and SBI0CR1<ACK>

BC	ACK=0 (Non-acknowledgment mode)		ACK=1 (Acknowledgment mode)	
	Number of clocks for data transfer	Number of data bits	Number of clocks for data transfer	Number of data bits
000	8	8	9	8
001	1	1	2	1
010	2	2	3	2
011	3	3	4	3
100	4	4	5	4
101	5	5	6	5
110	6	6	7	6
111	7	7	8	7

BC is cleared to "000" by the start condition.

Therefore, the slave address and the direction bit are always transferred in 8-bit units. In other cases, BC keeps the set value.

Note: SBI0CR1<ACK> must be set before transmitting or receiving a slave address. When SBI0CR1<ACK> is cleared, the slave address match detection and the direction bit detection are not executed properly.

18.4.3.2 Output of an acknowledge signal

In the acknowledgment mode, the SDA0 pin changes as follows during the period of the clocks for an acknowledge signal.

- In the master mode

21.5 Access to the Flash Memory Area

A read or a program fetch cannot be performed on the whole of the flash memory area if data is being written to the flash memory, if data in flash memory is being erased or if a security setting is being made in the flash memory. When performing these operation on the flash memory area, the flash memory cannot be directly accessed by using a program in the flash memory; the flash memory must be accessed using a program in the BOOTROM area or the RAM area.

Data can be written to and read from the flash memory area in units of one byte. Data in the flash memory can be erased in units of 4 kbytes, and all data in the flash memory can be erased at one stroke. A read can be performed using one memory transfer instruction. A write or erase, however, must be performed using more than one memory transfer instruction because the command sequence method is used. For information on the command sequence, refer to Table 21-1.

Note 1: To allow a program to resume control on the flash memory area that is rewritten, it is recommended that you let the program jump (return) after verifying that the program has been written properly.

Note 2: Do not reset the MCU (including a reset generated due to internal factors) when data is being written to the flash memory, data is being erased from the flash memory or the security command is being executed. If a reset occurs, there is the possibility that data in the flash memory may be rewritten to an unexpected value.

21.5.1 Flash memory control in serial PROM mode

The serial PROM mode is used to access the flash memory by using a control program provided in the BOOT-ROM area. Since almost all operations relating to access to the flash memory can be controlled simply using data supplied through the serial interface (UART or SIO), it is not necessary to operate the control register for the user. For details of the serial PROM mode, see "Serial PROM Mode".

To access the flash memory in serial PROM mode by using a user-specific program or peripheral functions other than UART and SIO, it is necessary to execute a control program in the RAM area by using the RAM loader command of the serial PROM mode. How to execute this control program is described in "21.5.1.1 How to transfer and write a control program to the RAM area in RAM loader mode of the serial PROM mode".

21.5.1.1 How to transfer and write a control program to the RAM area in RAM loader mode of the serial PROM mode

How to execute a control program in the RAM area in serial PROM mode is described below. A control program to be executed in the RAM area must be generated in the Intel-Hex format and be transferred using the RAM loader of the serial PROM mode.

Steps 1 and 2 shown below are controlled by a program in the BOOTROM, and other steps are controlled by a program transferred to the RAM area. The following procedure is linked with a program example to be explained later.

1. Transfer the write control program to the RAM area in RAM loader mode.
2. Jump to the RAM area.
3. Set a nonmaskable interrupt vector in the RAM area.
4. Set FLSCR1<FLSMD> to "0y101", and specify the area to be erased by making the appropriate FLSCR1<FAREA> setting. (Make the appropriate FLSCR1<ROMSEL> setting as required.) Then set "0xD5" on FLSCR2<CR1EN>.
5. Execute the erase command sequence.
6. Read the same flash memory address twice consecutively.
   (Repeat step 6 until the read values become the same.)
7. Specify the area (area erased in step 5 above) to which data is written by making the appropriate FLSCR1<FAREA> setting. (Make the appropriate FLSCR1<ROMSEL> setting as required.) Then set "0xD5" on FLSCR2<CR1EN>.
8. Execute the write command sequence.
9. Read the same flash memory address twice consecutively.
   (Repeat step 9 until the read values become the same.)

22.4 Example Connection for On-board Writing

Figure 22-2 shows example connections to perform on-board writing.

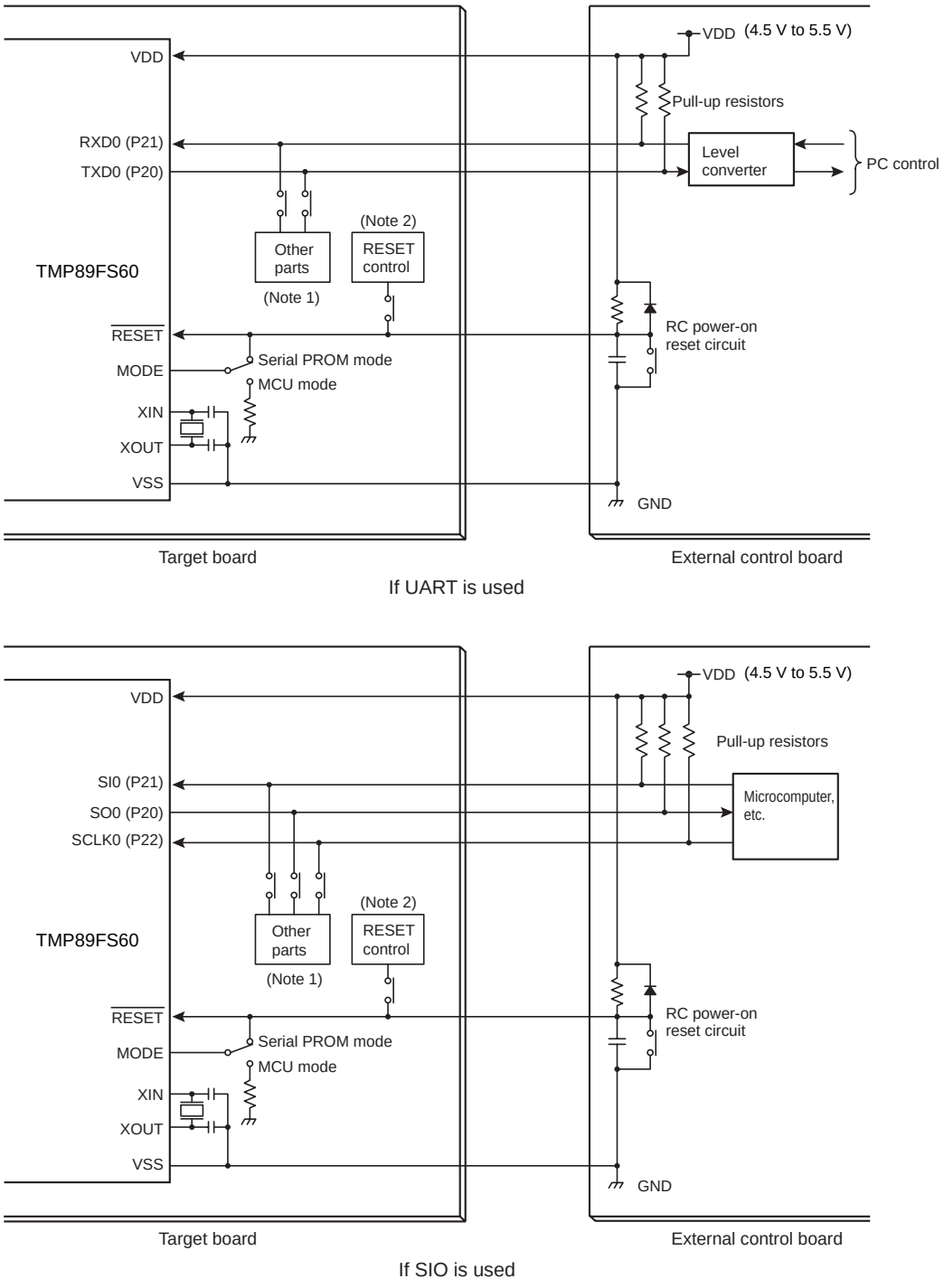


Figure 22-2 Example Connections for On-board Writing

Note 1: If other parts on a target board interfere with the UART communication in serial PROM mode, disconnect these pins by using a jumper or switch.

Note 2: If the reset control circuit on a target board interferes with the startup of serial PROM mode, disconnect the circuit by using a jumper, etc.

Note 3: For information on other pin settings, refer to "Table 22-3 Pin Functions in Serial PROM Mode".

Table 22-9 Transfer Formats of the Flash Memory Read Command

	Transfer byte	Transfer data from the external controller to TMP89FS60	Baud rate	Transfer data from TMP89FS60 to the external controller
BOOT ROM	m-th + 11 byte m-th + 12 byte	Number of bytes to read 07 to 00	Baud rate after adjustment Baud rate after adjustment	- OK: No data transmitted Error: No data transmitted
	m-th + 13 byte : n-th - 2 byte		Baud rate after adjustment Baud rate after adjustment	Memory data Memory data
	n-th - 1 byte	-	Baud rate after adjustment	OK: Checksum (high) Error: No data transmitted
	n-th byte	-	Baud rate after adjustment	OK: Checksum (low) Error: No data transmitted
	n-th + 1 byte	(Wait for the next operation command data)	Baud rate after adjustment	-

Note 1: "0x** × 3" means that the device goes into an idle state after transmitting 3 bytes of 0x**. For further information, refer to Table 22-18.

Note 2: For information on checksums, refer to "22.10 Checksum (SUM)". For information on passwords, refer to "22.12.1 Passwords".

Note 3: If the area 0xFFE0 through 0xFFFF is all 0xFF, password authentication is not performed and, therefore, the password string need not be transmitted. The password count storage address and password comparison start address, however, must be specified, even for a blank product. If the password count storage address and/or password comparison start address are/is incorrect, a password error occurs; the TMP89FS60 stops communication and goes into an idle state. Therefore, if a password error occurs, initialize the TMP89FS60 by using the $\overline{\text{RESET}}$ pin, and restart the serial PROM mode.

Note 4: If the security program is enabled in flash memory or if a password error occurs, the TMP89FS60 stops communication, and goes into an idle state. Therefore, if a password error occurs, initialize the TMP89FS60 by using the $\overline{\text{RESET}}$ pin, and restart the serial PROM mode.

Note 5: If a communication error occurs during the transfer of a password address or a password string, the TMP89FS60 stops communication and goes into an idle state. Therefore, when a password error occurs, initialize the TMP89FS60 by using the $\overline{\text{RESET}}$ pin, and restart the serial PROM mode.

Note 6: If the number of bytes received at the m-th + 7 byte, m-th + 9 byte or m-th + 11 byte is more than 0x000000 or the size of internal memory, the TMP89FS60 stops communication and goes into an idle state.

22.14 AC Characteristics (UART)

Table 22-24 UART Timing-1

Parameter	Symbol	Clock frequency (fcgck)	Minimum required time	
			At fcgck = 1 MHz	At fcgck = 8 MHz
Time from when MCU receives 0x86 to when it echoes back	CMeb1	Approx. 660	660 µs	82.5 µs
Time from when MCU receives 0x79 to when it echoes back	CMeb2	Approx. 540	540 µs	67.5 µs
Time from when MCU receives an operation command to when it echoes back	CMeb3	Approx. 300	300 µs	37.5 µs
Time required to calculate the checksum (flash memory)	CMfsm	Approx. 2800000 (60KB)	2.8 s	350 ms
Time required to calculate the checksum (RAM)	CMrsm	Approx. 160	160 µs	20 µs
Time when MCU receives Intel Hex data to when it transmits over-write detection data	CMwr	Approx. 200	200 µs	25 µs
Time from when MCU receives data (number of read bytes) to when it transmits memory data	CMrd	Approx. 430	430 µs	54 µs
Time from when MCU receives data (mask ROM emulation setting data) to when it echoes back	CMem2	Approx. 420	420 µs	52.5 µs
Time required to enable the security program	CMrp	Approx. 1080	1.08 ms	135 µs

Table 22-25 UART Timing-2

Parameter	Symbol	Clock frequency (fcgck)	Minimum required time	
			At fcgck = 1 MHz	At fcgck = 8 MHz
Time required to keep MODE and RESET pins at L after power-on	RSsup	-	10 ms	
Time from when MODE and RESET pins are set to H to the acceptance of RXD	RXsup	-	20 ms	
Time from when MCU echoes back 0x86 to the acceptance of RXD	CMtr1	Approx. 140	140 µs	18 µs
Time from when MCU echoes back 0x79 to the acceptance of RXD	CMtr2	Approx. 90	90 µs	11 µs
Time from when MCU echoes back an operation command to the acceptance of RXD	CMtr3	Approx. 270	270 µs	34 µs
Time from when the execution of a current command is completed to the acceptance of the next operation command	CMnx	Approx. 1100	1.1 ms	138 µs

25. Electrical Characteristics

25.1 Absolute Maximum Ratings

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply voltage	V_{DD}		−0.3 to 6.0	V
Input voltage	V_{IN1}	P0, P1, P2 (excluding P23 and P24), P4, P5, P7, P8, P9, PB (tri-state port)	−0.3 to V_{DD} + 0.3	V
	V_{IN2}	P23, P24 (sink open drain port)	−0.3 to V_{DD} + 0.3	
	V_{IN3}	AIN0 to AIN15 (analog input voltage)	−0.3 to A_{VDD} + 0.3	
Output voltage	V_{OUT1}		−0.3 to V_{DD} + 0.3	V
Output current (per pin)	I_{OUT1}	P0, P1, P2 (excluding P23 and P24), P4, P5, P7, P8, P9, PB (tri-state port)	−1.8	mA
	I_{OUT2}	P0, P1, P2, P4, P9 (pull-up resistor)	−0.4	
	I_{OUT3}	P0, P1, P2, P4, P7, P8, P9 (tri-state port)	3.2	
	I_{OUT4}	PB (large current port)	30	
Output current (total)	ΣI_{OUT1}	P0, P1, P2 (excluding P23 and P24), P4, P5, P7, P8, P9, PB (tri-state port)	−30	
	ΣI_{OUT2}	P0, P1, P2, P4, P9 (pull-up resistor)	−4	
	ΣI_{OUT3}	P0, P1, P2, P4, P5, P7, P8, P9 (tri-state port)	60	
	ΣI_{OUT4}	PB (large current port)	120	
Power dissipation (Topr = 85°C)	P_D		250	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		−55 to 125	
Operating temperature	Topr		−40 to 85	