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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128d4-anr

Table 7-3. Number of Bytes and Pages in the EEPROM

Devices	EEPROM	Page Size	E2BYTE	E2PAGE	No of Pages
	Size	bytes			
ATxmega16D4	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega32D4	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega64D4	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128D4	2K	32	ADDR[4:0]	ADDR[10:5]	64

14. I/O Ports

14.1 Features

- 34 general purpose input and output pins with individual configuration
- Output driver with configurable driver and pull settings:
  - Totem-pole
  - Wired-AND
  - Wired-OR
  - Bus-keeper
  - Inverted I/O
- Input with synchronous and/or asynchronous sensing with interrupts and events
  - Sense both edges
  - Sense rising edges
  - Sense falling edges
  - Sense low level
- Optional pull-up and pull-down resistor on input and Wired-OR/AND configurations
- Asynchronous pin change sensing that can wake the device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins
  - Hardware read-modify-write through dedicated toggle/clear/set registers
  - Configuration of multiple pins in a single operation
  - Mapping of port registers into bit-accessible I/O memory space
- Peripheral clocks output on port pin
- Real-time counter clock output to port pin
- Event channels can be output on port pin
- Remapping of digital peripheral pin functions
  - Selectable USART, SPI, and timer/counter input/output pin locations

14.2 Overview

One port consists of up to eight port pins: pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, SPI, and timer/counters, can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

The notation of the ports are PORTA, PORTB, PORTC, PORTD, PORTE, and PORTR.

20. TWI – Two-Wire Interface

20.1 Features

- Two identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
  - Phillips I^{2}C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

20.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I^{2}C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V$_{CC}$ voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

28. Pinout and Pin Functions

The device pinout is shown in "Pinout/Block Diagram" on page 3. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

28.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

28.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

28.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

28.1.3 Analog Functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
A_{REF}	Analog reference input pin

28.1.4 Timer/Counter and AWEX Functions

OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

28.1.5 Communication Functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

PORT E	PIN #	INTERRUPT	TCE0	TWIE
VCC	31			
PE2	32	SYNC/ASYNC	OC0C	
PE3	33	SYNC	OC0D	

Table 28-6. Port F - Alternate Functions

PORT R	PIN #	INTERRUPT	PDI	XTAL	TOSC[1]
PDI	34		PDI_DATA		
$\overline{RESET}$	35		PDI_CLOCK		
PRO	36	SYNC		XTAL2	TOSC2
PR1	37	SYNC		XTAL1	TOSC1

Note: 1. TOSC pins can optionally be moved to PE2/PE3

Mnemonics	Operands	Description	Operation		Flags	#Clocks
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0		None	2 / 3[1]
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND		None	3[1]
CALL	k	call Subroutine	PC ← k		None	3 / 4[1]
RET		Subroutine Return	PC ← STACK		None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK		I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3		None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr		Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C		Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K		Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3		None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3		None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3		None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3		None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1		None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1		None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1		None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1		None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1		None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1		None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1		None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1		None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1		None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1		None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N $\oplus$ V= 0) then PC ← PC + k + 1		None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N $\oplus$ V= 1) then PC ← PC + k + 1		None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1		None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1		None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1		None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1		None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1		None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1		None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1		None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1		None	1 / 2
Data transfer instructions						
MOV	Rd, Rr	Copy Register	Rd ← Rr		None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr		None	1
LDI	Rd, K	Load Immediate	Rd ← K		None	1

Mnemonics	Operands	Description	Operation			Flags	#Clocks
LDS	Rd, k	Load Direct from data space	Rd	←	(k)	None	$2^{(1)(2)}$
LD	Rd, X	Load Indirect	Rd	←	(X)	None	$1^{(1)(2)}$
LD	Rd, X+	Load Indirect and Post-Increment	Rd X	← ←	(X) X + 1	None	$1^{(1)(2)}$
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, Rd ← (X)	← ←	X - 1 (X)	None	$2^{(1)(2)}$
LD	Rd, Y	Load Indirect	Rd ← (Y)	←	(Y)	None	$1^{(1)(2)}$
LD	Rd, Y+	Load Indirect and Post-Increment	Rd Y	← ←	(Y) Y + 1	None	$1^{(1)(2)}$
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y Rd	← ←	Y - 1 (Y)	None	$2^{(1)(2)}$
LDD	Rd, Y+q	Load Indirect with Displacement	Rd	←	(Y + q)	None	$2^{(1)(2)}$
LD	Rd, Z	Load Indirect	Rd	←	(Z)	None	$1^{(1)(2)}$
LD	Rd, Z+	Load Indirect and Post-Increment	Rd Z	← ←	(Z), Z+1	None	$1^{(1)(2)}$
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z Rd	← ←	Z - 1, (Z)	None	$2^{(1)(2)}$
LDD	Rd, Z+q	Load Indirect with Displacement	Rd	←	(Z + q)	None	$2^{(1)(2)}$
STS	k, Rr	Store Direct to Data Space	(k)	←	Rd	None	$2^{(1)}$
ST	X, Rr	Store Indirect	(X)	←	Rr	None	$1^{(1)}$
ST	X+, Rr	Store Indirect and Post-Increment	(X) X	← ←	Rr, X + 1	None	$1^{(1)}$
ST	-X, Rr	Store Indirect and Pre-Decrement	X (X)	← ←	X - 1, Rr	None	$2^{(1)}$
ST	Y, Rr	Store Indirect	(Y)	←	Rr	None	$1^{(1)}$
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) Y	← ←	Rr, Y + 1	None	$1^{(1)}$
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y (Y)	← ←	Y - 1, Rr	None	$2^{(1)}$
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q)	←	Rr	None	$2^{(1)}$
ST	Z, Rr	Store Indirect	(Z)	←	Rr	None	$1^{(1)}$
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) Z	← ←	Rr Z + 1	None	$1^{(1)}$
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z	←	Z - 1	None	$2^{(1)}$
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q)	←	Rr	None	$2^{(1)}$
LPM		Load Program Memory	R0	←	(Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd	←	(Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd Z	← ←	(Z), Z + 1	None	3
ELPM		Extended Load Program Memory	R0	←	(RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd	←	(RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd Z	← ←	(RAMPZ:Z), Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z)	←	R1:R0	None	-

31.3 49C2

A1 BALL ID

E

D

TOP VIEW

0.10

A1

A

A2

SIDE VIEW

E1

G
F
E
D
C
B
A

e

D1

1 2 3 4 5 6 7

A1 BALL CORNER

b

e

49 - ø0.35 ±0.05

BOTTOM VIEW
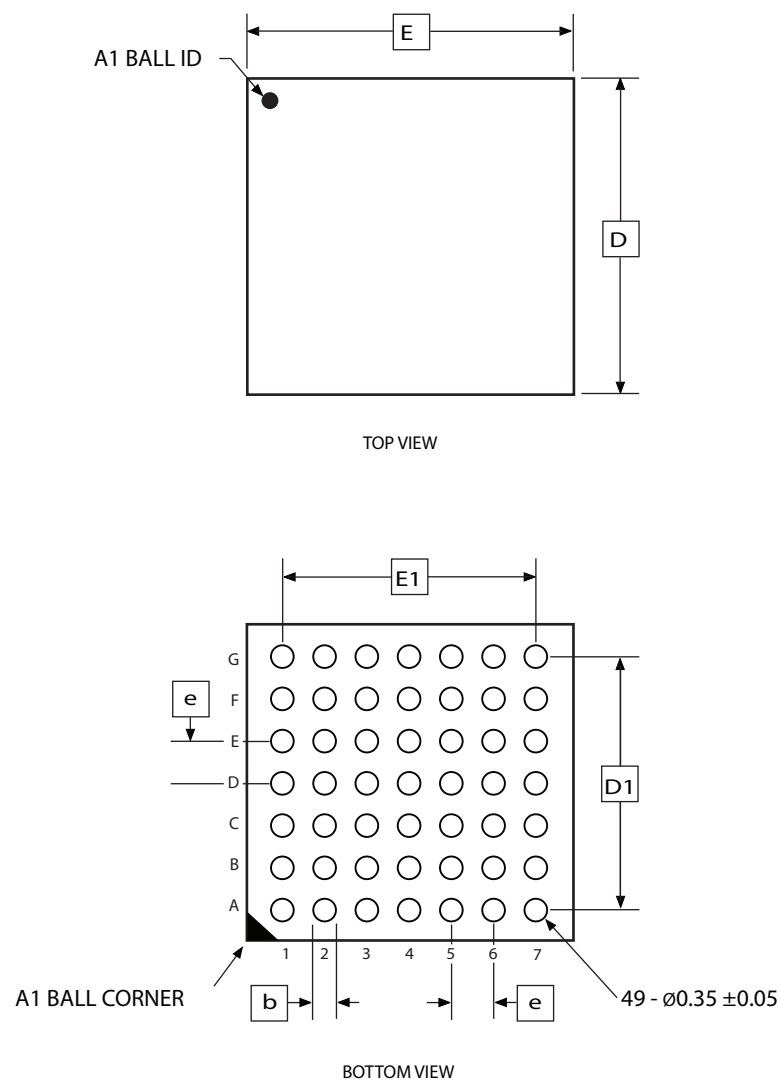
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.20	–	–	
A2	0.65	–	–	
D	4.90	5.00	5.10	
D1	3.90 BSC			
E	4.90	5.00	5.10	
E1	3.90 BSC			
b	0.30	0.35	0.40	
e	0.65 BSC			

3/14/08

| Atmel® Package Drawing Contact: packagedrawings@atmel.com | TITLE 49C2, 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA) | GPC CBD | DRAWING NO. 49C2 | REV. A |

32.1.4 Wake-up Time from Sleep Modes

Table 32-6. **Device Wake-up Time from Sleep Modes with Various System Clock Sources**

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		μs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		5.0		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-2. Wake-up Time Definition
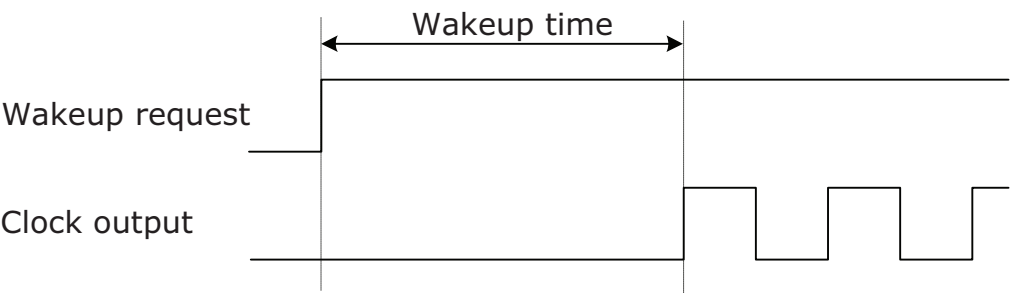
32.3.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-63. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$I_{OH}^{(1)}$/ $I_{OL}^{(2)}$	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.7 - 3.6V		2		V_{CC}+0.3	V
		V_{CC} = 2.0 - 2.7V		$0.7*V_{CC}$		V_{CC}+0.3	
		V_{CC} = 1.6 - 2.0V		$0.7*V_{CC}$		V_{CC}+0.3	
V_{IL}	Low level input voltage	V_{CC} = 2.7- 3.6V		-0.3		$0.3*V_{CC}$	
		V_{CC} = 2.0 - 2.7V		-0.3		$0.3*V_{CC}$	
		V_{CC} = 1.6 - 2.0V		-0.3		$0.3*V_{CC}$	
V_{OH}	High level output voltage	V_{CC} = 3.0 - 3.6V	I_{OH} = -2mA	2.4	$0.94*V_{CC}$		
		V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.0 - 3.6V	I_{OL} = 2mA		$0.05*V_{CC}$	0.4	
		V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current	T = 25°C			<0.001	0.1	µA
R_P	Pull/Buss keeper resistor				24		kΩ
t_r	Rise time	No load			4		ns

Notes: 1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OH} for PORTC must not exceed 200mA.
The sum of all I_{OH} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all I_{OH} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OL} for PORTC must not exceed 200mA.
The sum of all I_{OL} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all I_{OL} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

Table 32-74. Programming Time

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
	Chip erase	64KB Flash, EEPROM[2] and SRAM erase		55		ms
	Flash	Page erase		4		
		Page write		4		
		Atomic Page Erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic Page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.3.13 Clock and Oscillator Characteristics

32.3.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 32-75.   32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.3.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 32-76.   2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.21		

32.4.15 Two-Wire Interface Characteristics

Table 32-114 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-28.

Figure 32-28.Two-wire Interface Bus Timing
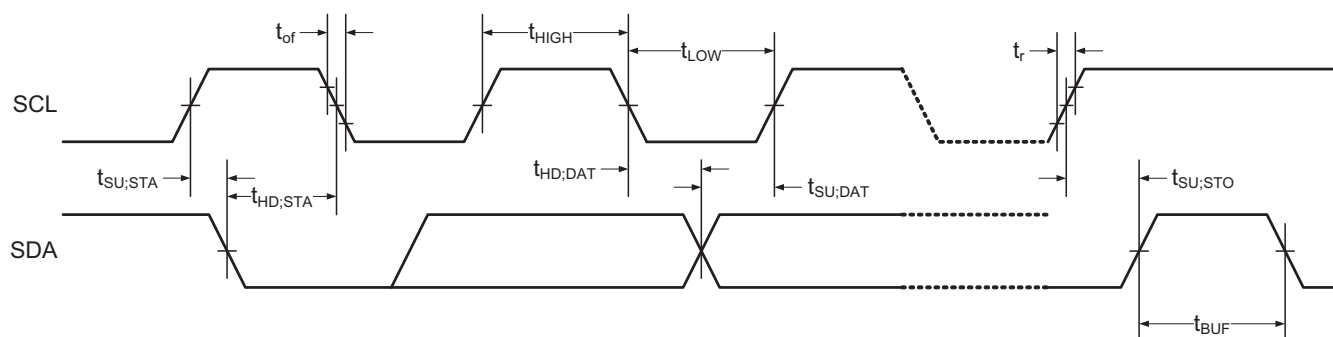
Table 32-114. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7 * V_{CC}$		$V_{CC} + 0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3 * V_{CC}$	
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05 * V_{CC}$[1]			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1 C_b$[1][2]		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$[2]	$20 + 0.1 C_b$[1][2]		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER}[3]$>max(10f_{SCL}, 250kHz)$	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\dfrac{V_{CC} - 0.4V}{3mA}$		$\dfrac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\dfrac{300ns}{C_b}$	

Figure 33-27. I/O Pin Output Voltage vs. Source Current
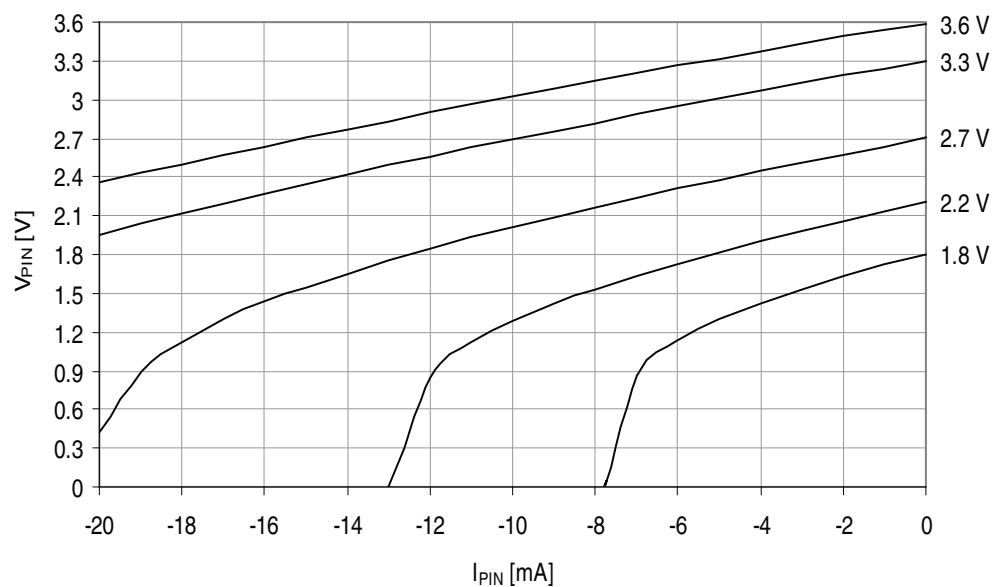
Figure 33-28. I/O Pin Output Voltage vs. Sink Current
$V_{CC} = 1.8V$
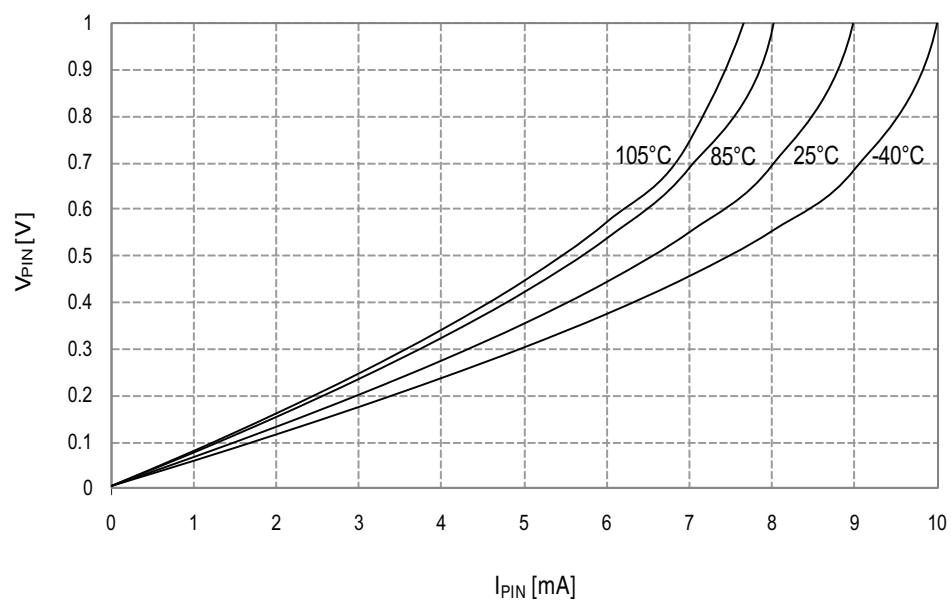
33.1.9.4 32MHz Internal Oscillator

Figure 33-71. 32MHz Internal Oscillator Frequency vs. Temperature
   DFLL disabled
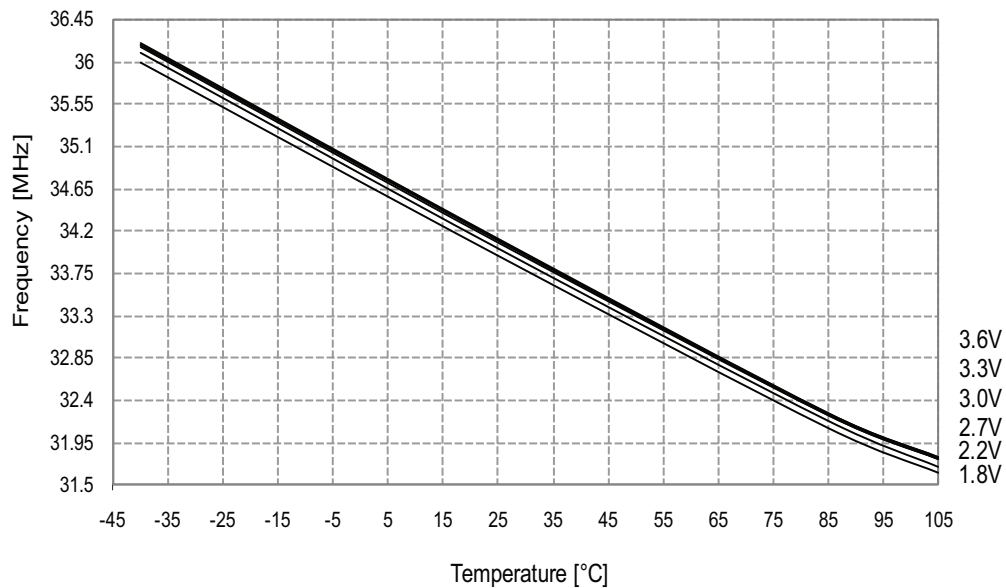
Figure 33-72. 32MHz Internal Oscillator Frequency vs. Temperature
   DFLL enabled, from the 32.768kHz internal oscillator
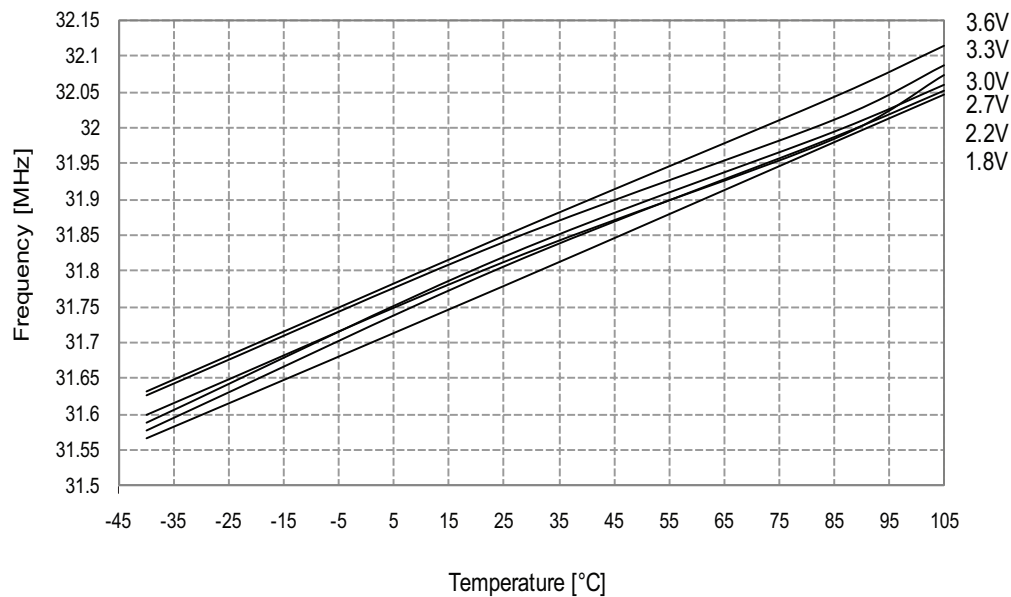
Figure 33-82. Active Mode Supply Current vs. V$_{CC}$
    f$_{SYS}$ = 32.768kHz internal oscillator
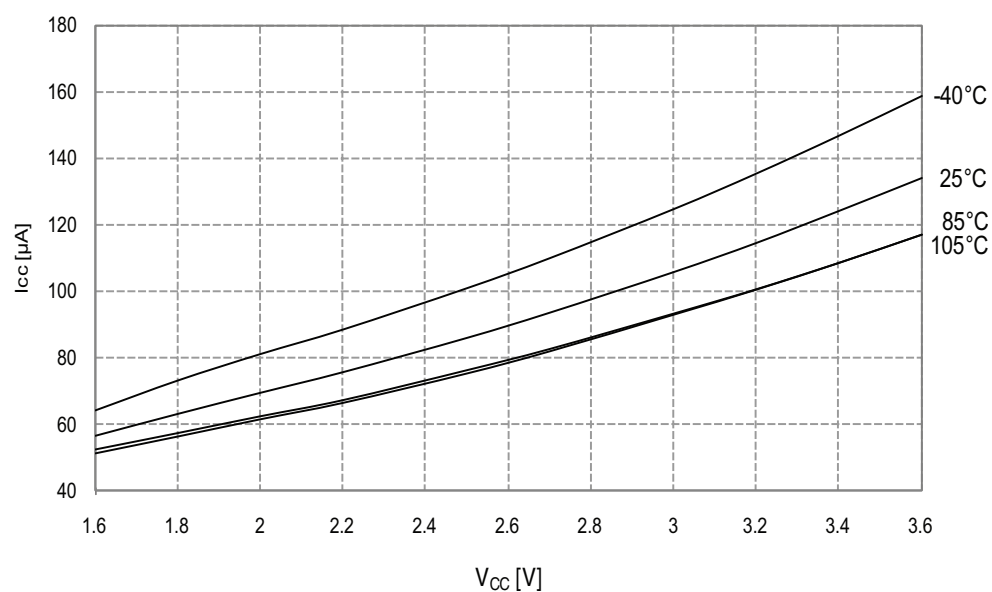
Figure 33-83. Active Mode Supply Current vs. V$_{CC}$
    f$_{SYS}$ = 1MHz external clock
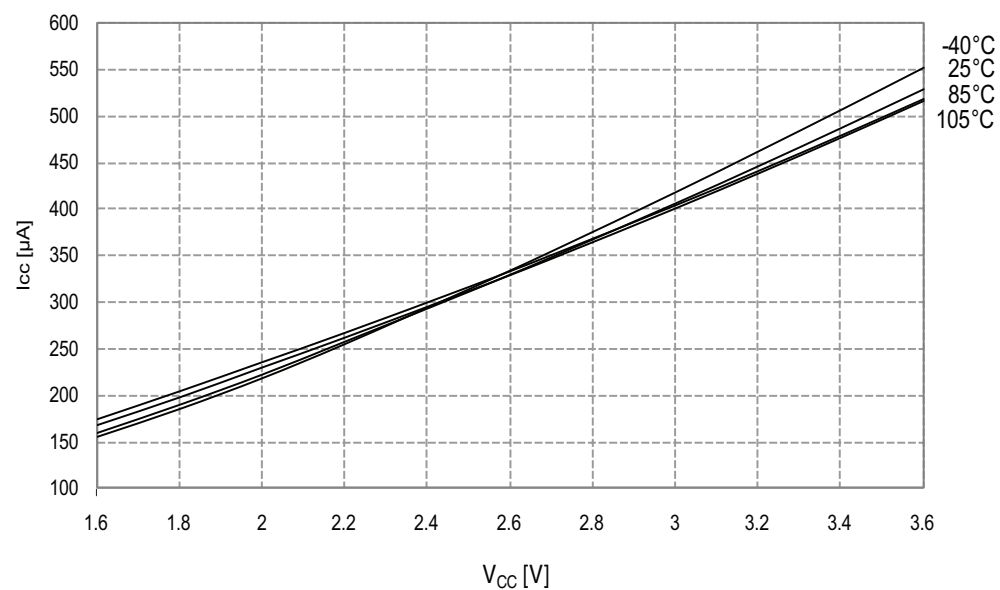
Figure 33-138. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage
  $V_{CC} = 3.0V$
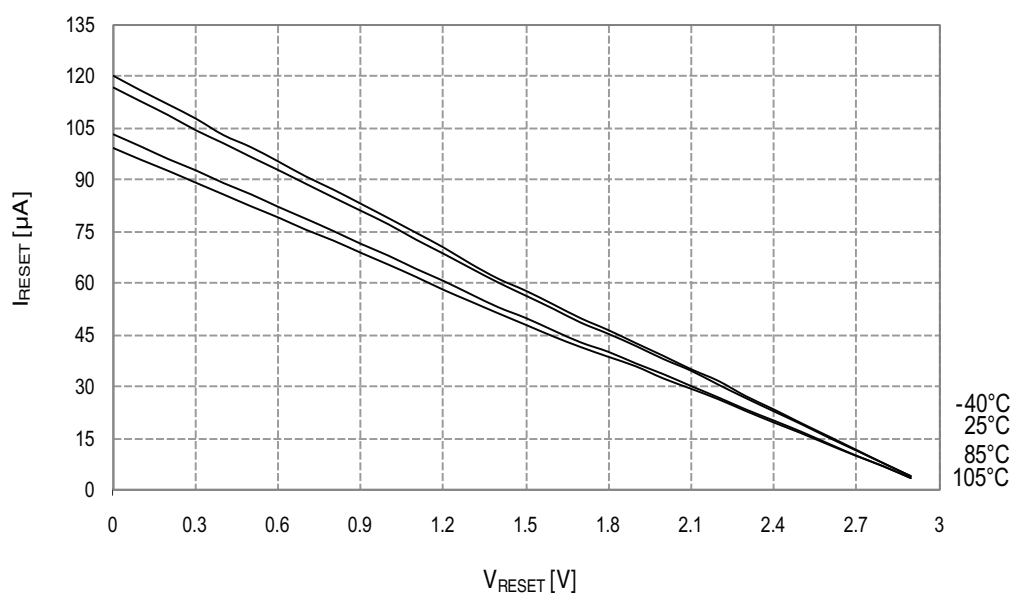
Figure 33-139. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage
  $V_{CC} = 3.3V$
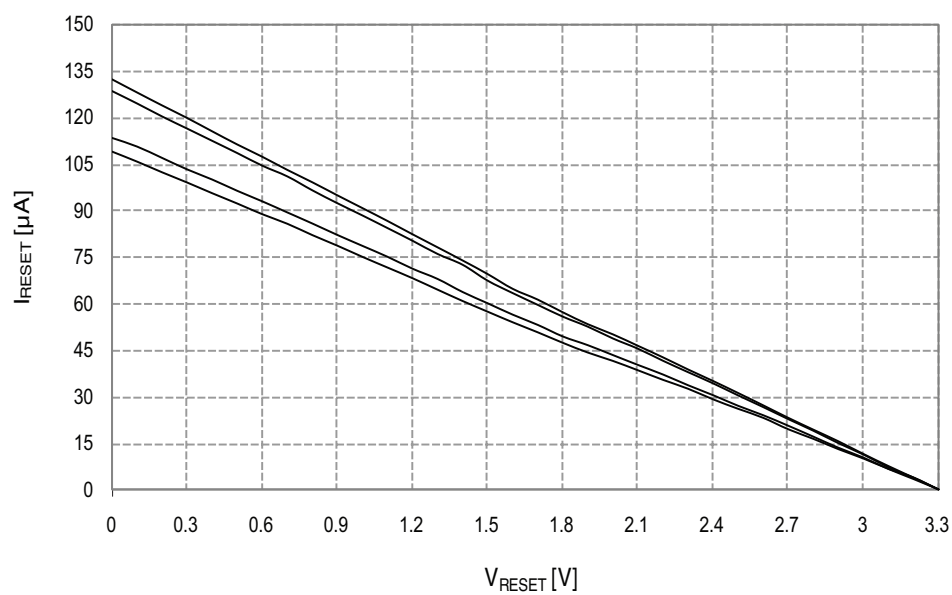
33.2.10 Two-Wire Interface Characteristics

Figure 33-156. SDA Hold Time vs. Temperature
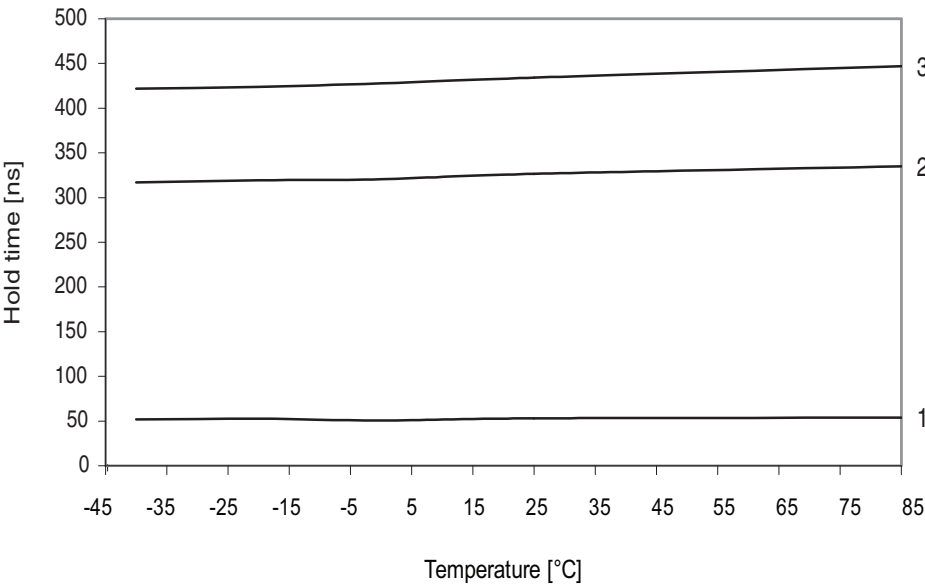
Figure 33-157. SDA Hold Time vs. Supply Voltage
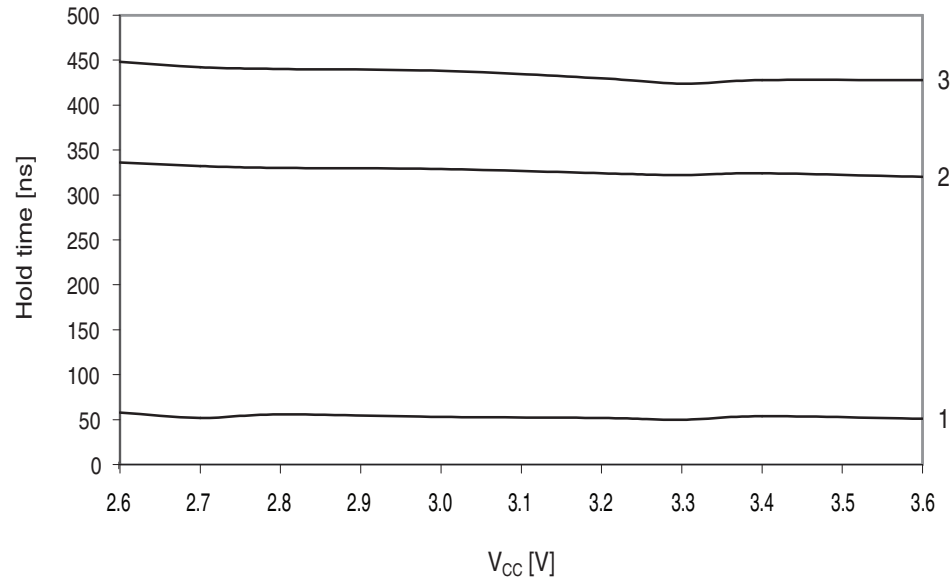
33.3.1.3 Power-down Mode Supply Current

Figure 33-173. Power-down Mode Supply Current vs. Temperature
All functions disabled
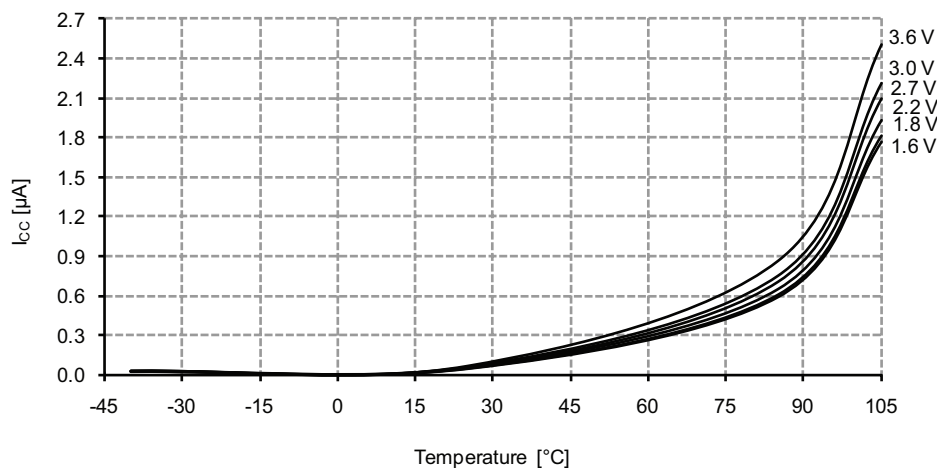
Figure 33-174. Power-down Mode Supply Current vs. V$_{CC}$
All functions disabled
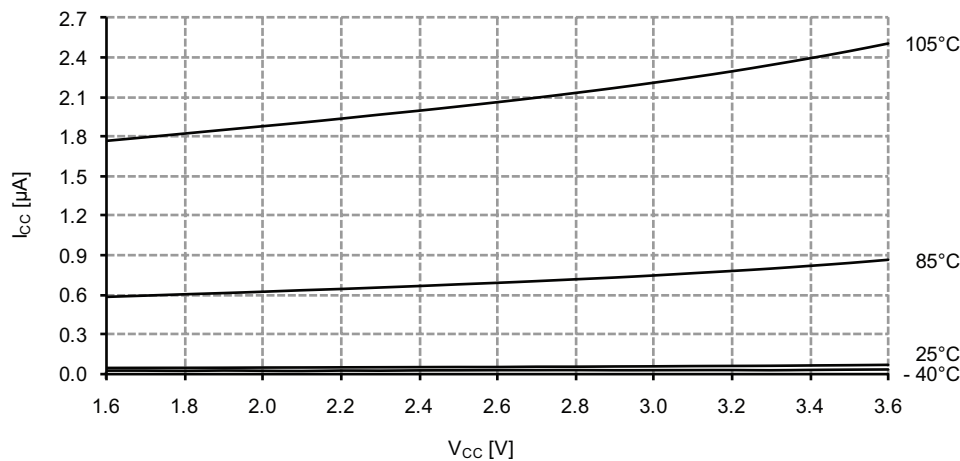
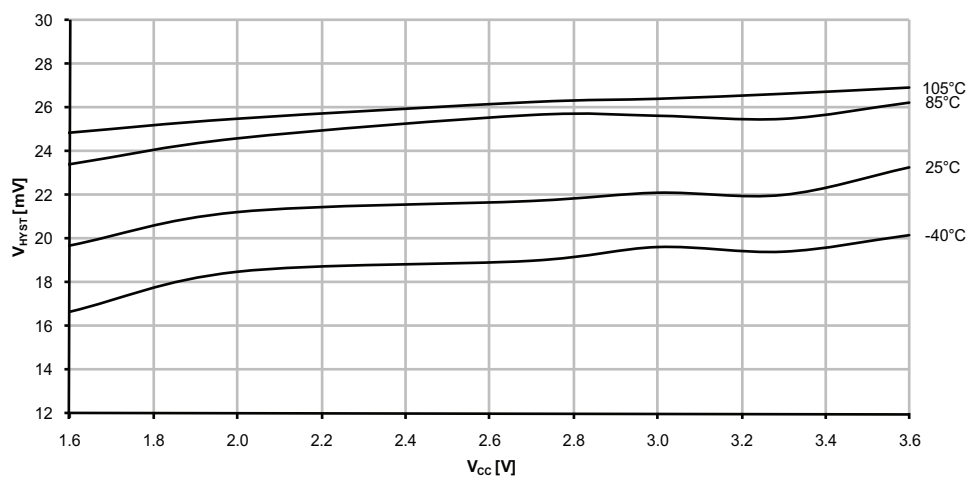**Figure 33-295. Analog Comparator Hysteresis vs. V$_{CC}$**
   Low power, small hysteresis

Figure 33-296. Analog Comparator Hysteresis vs. V$_{CC}$
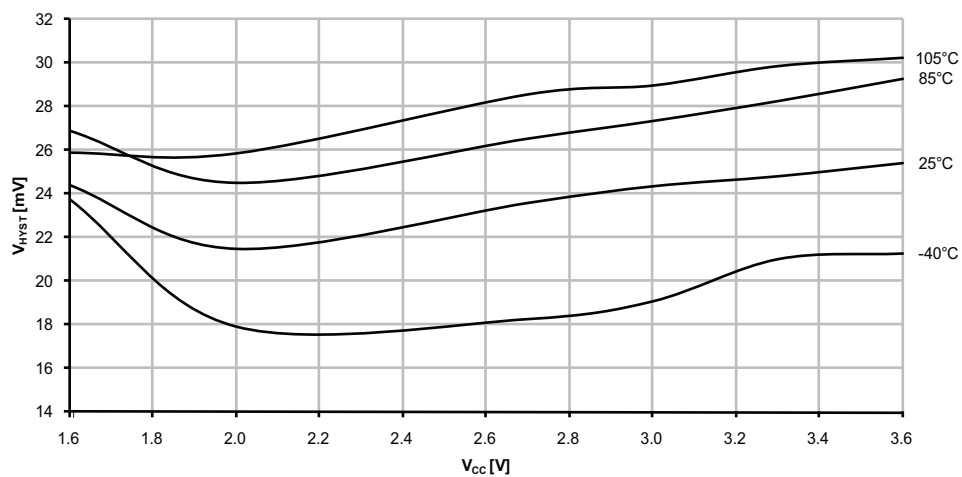   *High-speed mode, large hysteresis*

Figure 33-319. 32MHz Internal Oscillator Frequency vs. Temperature
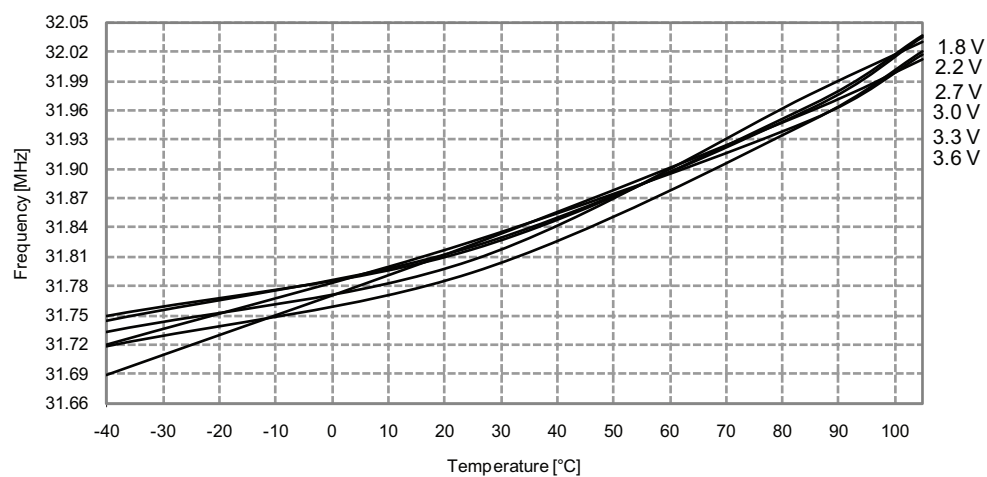 *DFLL enabled, from the 32.768kHz internal oscillator*

Figure 33-320. 32MHz Internal Oscillator CALA Calibration Step Size
  $V_{CC} = 3.0V$