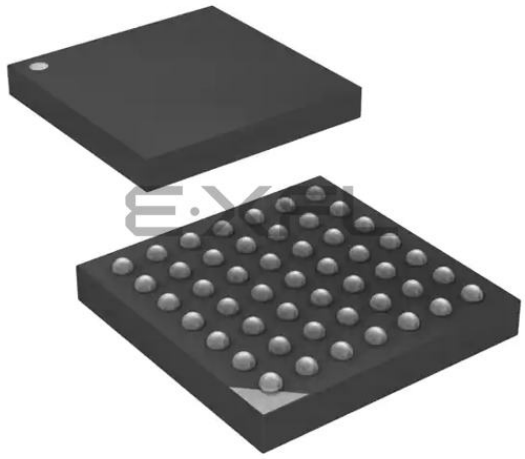

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128d4-cu

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to "Electrical Characteristics" on page 64.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 14.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes for Atmel AVR XMEGA D4 Devices

Device	Device ID bytes		
	Byte 2	**Byte 1**	**Byte 0**
ATxmega16D4	42	94	1E
ATxmega32D4	42	95	1E
ATxmega64D4	47	96	1E
ATxmega128D4	47	97	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

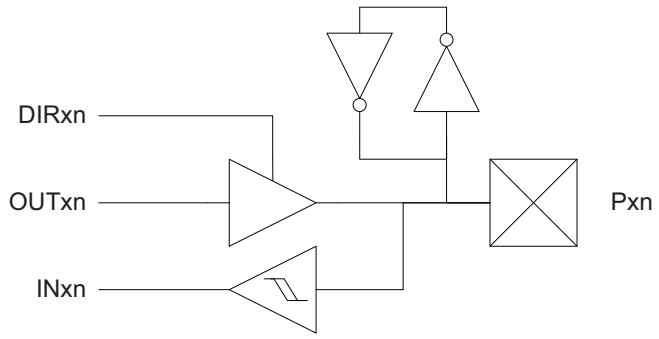
An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

Figure 14-4. I/O Configuration - Totem-pole with Bus-keeper



14.3.5 Others

Figure 14-5. Output Configuration - Wired-OR with Optional Pull-down

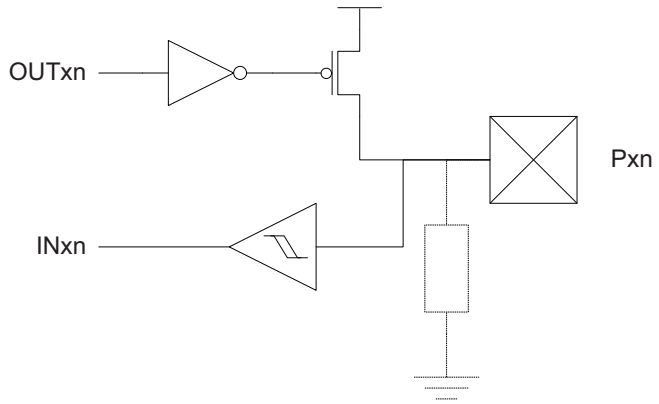
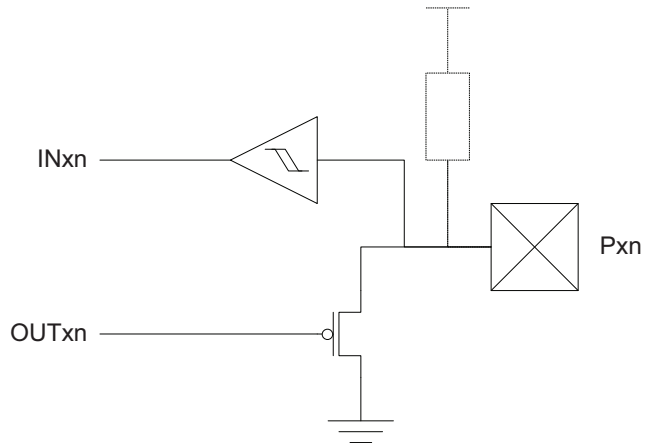


Figure 14-6. I/O Configuration - Wired-AND with Optional Pull-up



14.4 Input Sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 14-7.

25. ADC – 12-bit Analog to Digital Converter

25.1 Features

- One Analog to Digital Converters (ADC)
- 12-bit resolution
- Up to 200 thousand samples per second
  - Down to 3.6µs conversion time with 8-bit resolution
  - Down to 5.0µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 12 single-ended inputs
  - 12x4 differential inputs without gain
  - 12x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Three internal inputs
  - Internal temperature sensor
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional interrupt/event on compare result

25.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to 200 thousand samples per second (ksps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

The ADC measurements can either be started by application software or an incoming event from another peripheral in the device. The ADC measurements can be started with predictable timing, and without software intervention.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The AV_{CC}/10 and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

Table 32-10. Accuracy Characteristics

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL[1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			200ksps, V_{REF} = 3V		0.6	1	
			200ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL[1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			200ksps, V_{REF} = 3V		0.35	1	
			200ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset Error	Differential mode			8		mV
			Temperature drift		0.01		mV/K
			Operating voltage drift		0.25		mV/V
	Gain Error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
		Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

32.2.11 Power-on Reset Characteristics

Table 32-44. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} [1]	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.2.12 Flash and EEPROM Memory Characteristics

Table 32-45. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 32-46. Programming Time

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
	Chip erase[2]	32KB Flash, EEPROM		50		ms
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 32-51. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency[1]	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.2.13.6External Clock Characteristics

Figure 32-10.External Clock Drive Waveform

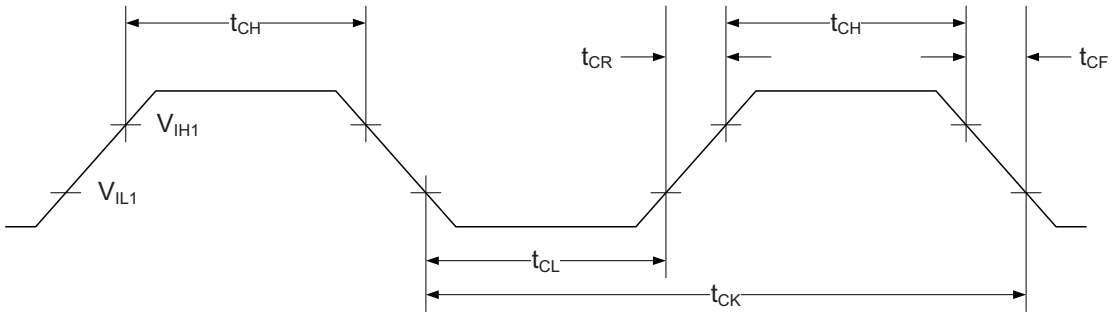


Table 32-52. External Clock[1]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency[2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7.0			
$t_{CH/CL}$	Clock high/low time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
$V_{IL/IH}$	Low/high level input voltage		See Table 32-7 on page 69			V
Δt_{CK}	Reduction in period time from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.3.14 SPI Characteristics

Figure 32-19.SPI Timing Requirements in Master Mode

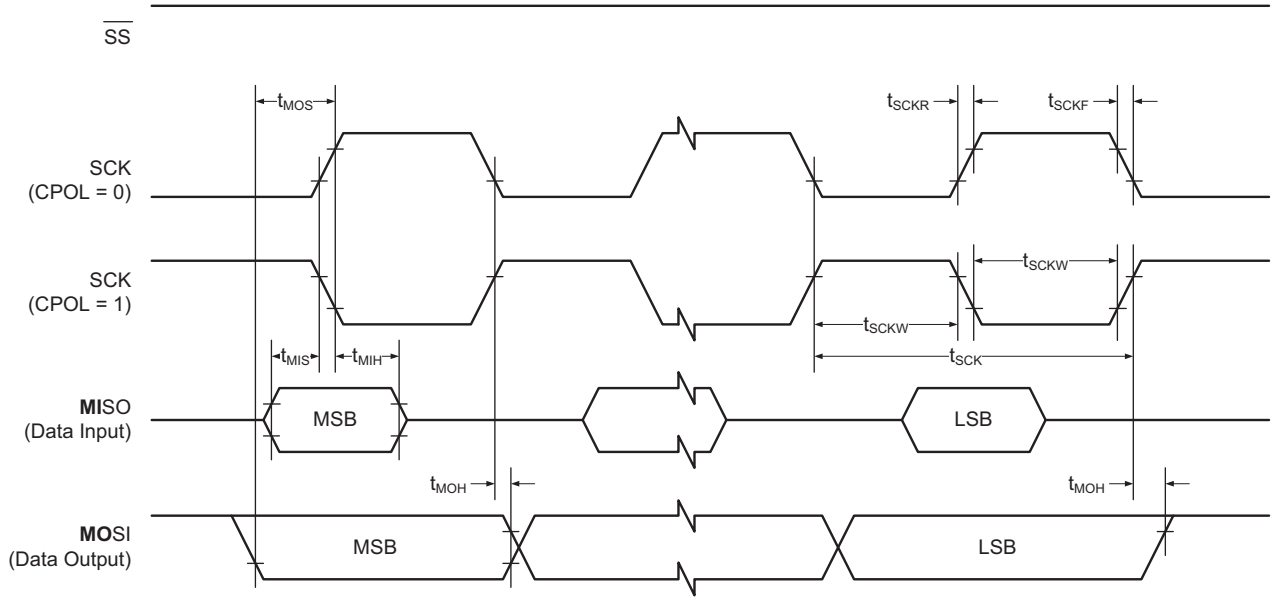
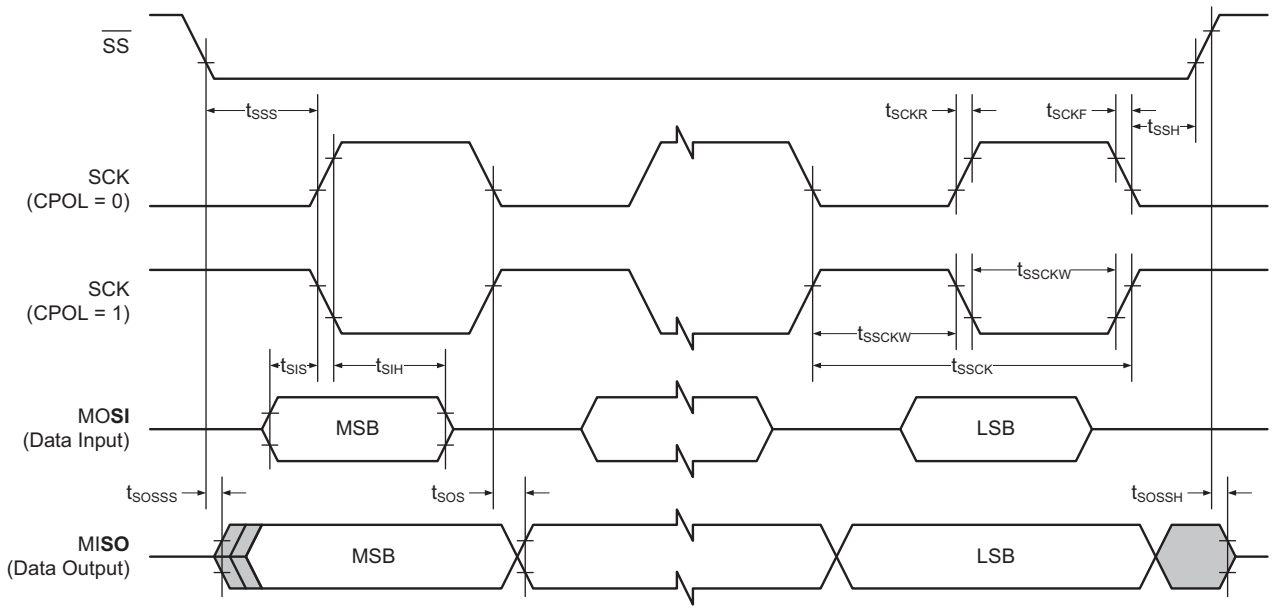


Figure 32-20.SPI Timing Requirements in Slave Mode



32.4.14 SPI Characteristics

Figure 32-26.SPI Timing Requirements in Master Mode

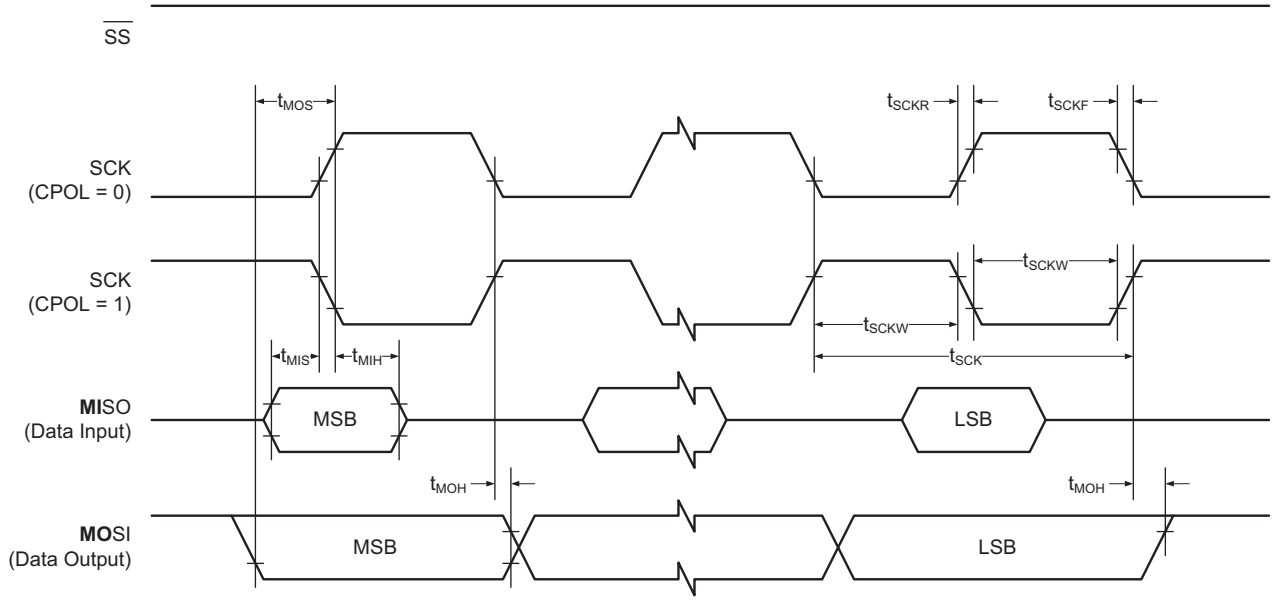
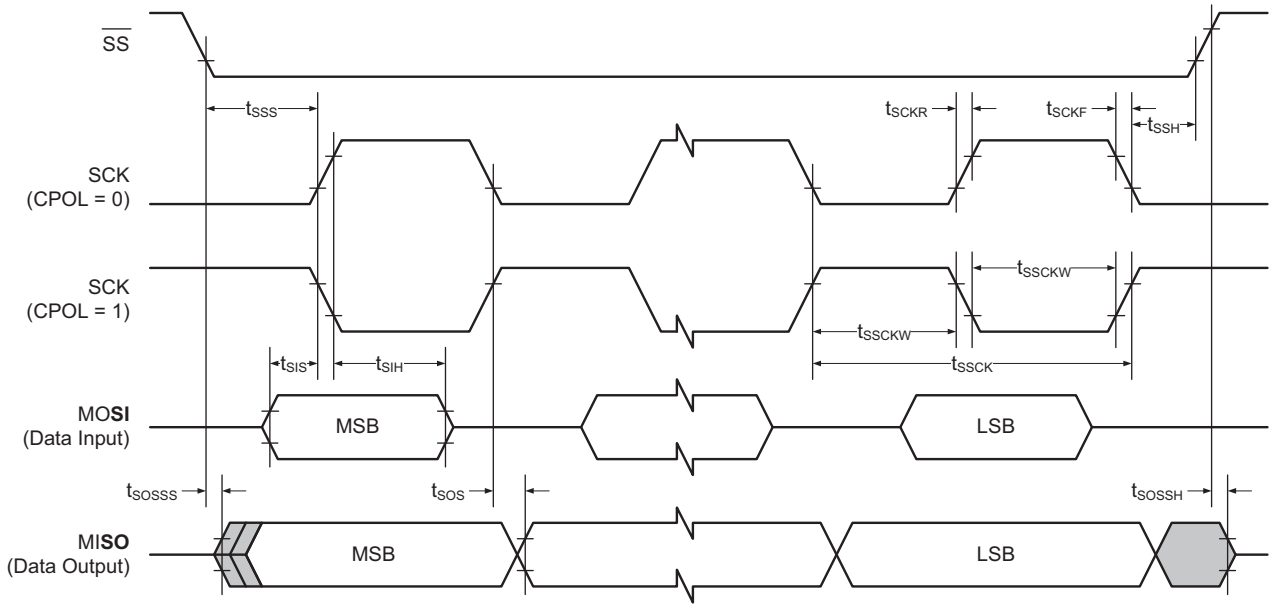


Figure 32-27.SPI Timing Requirements in Slave Mode



32.4.15 Two-Wire Interface Characteristics

Table 32-114 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-28.

Figure 32-28.Two-wire Interface Bus Timing

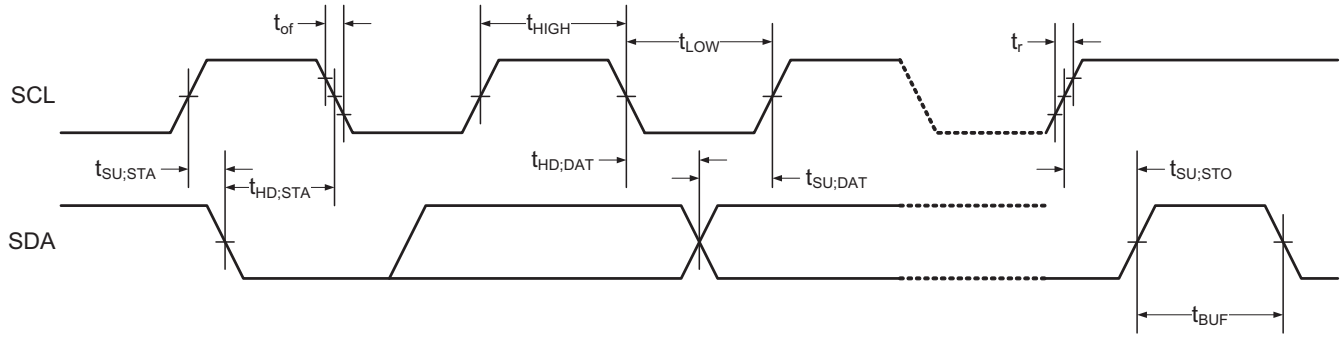


Table 32-114. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3*V_{CC}$	
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05*V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	

Figure 33-49. Analog Comparator Hysteresis vs. V_{CC}

Low power, small hysteresis

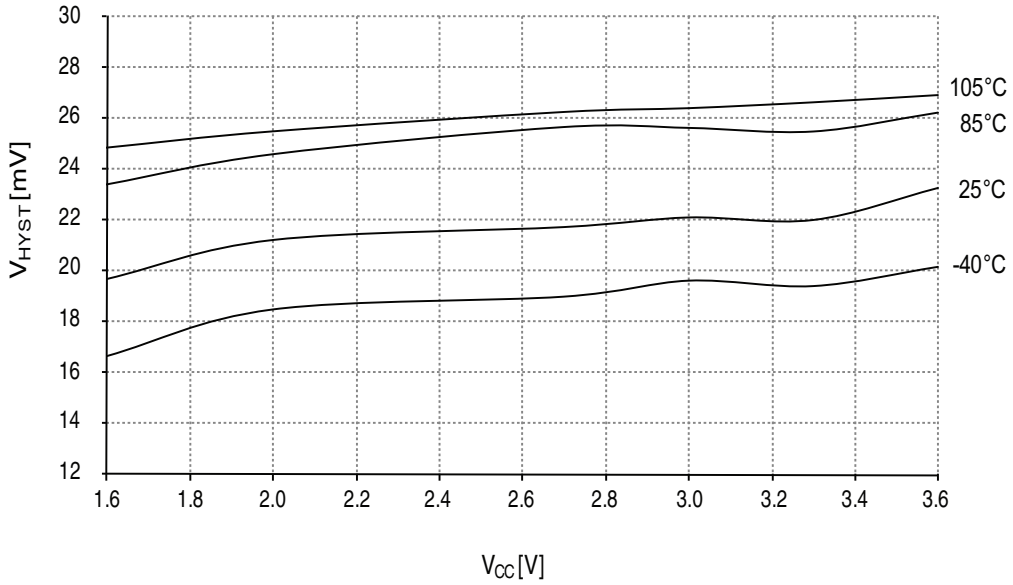


Figure 33-50. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis

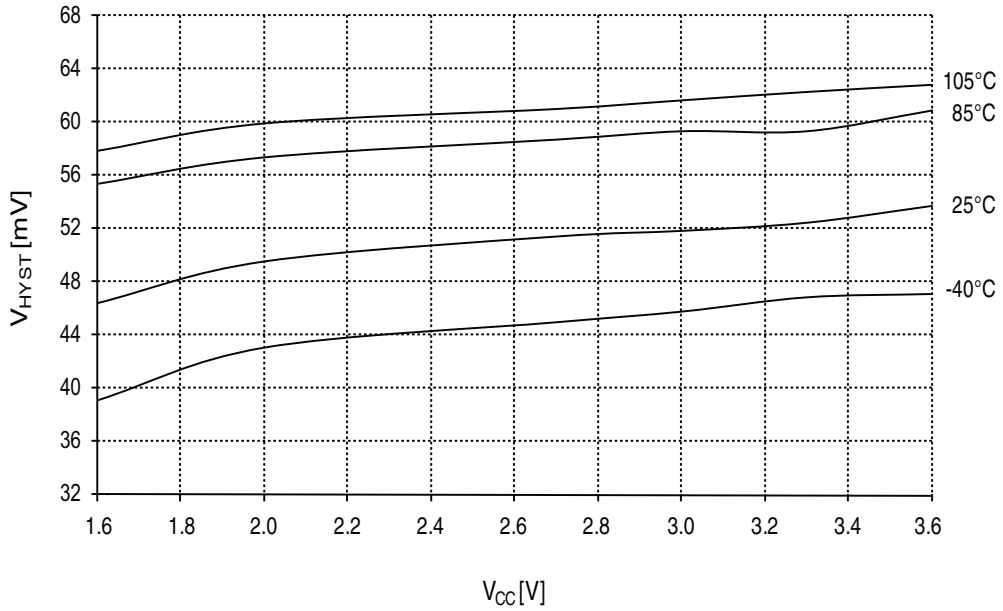


Figure 33-90. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

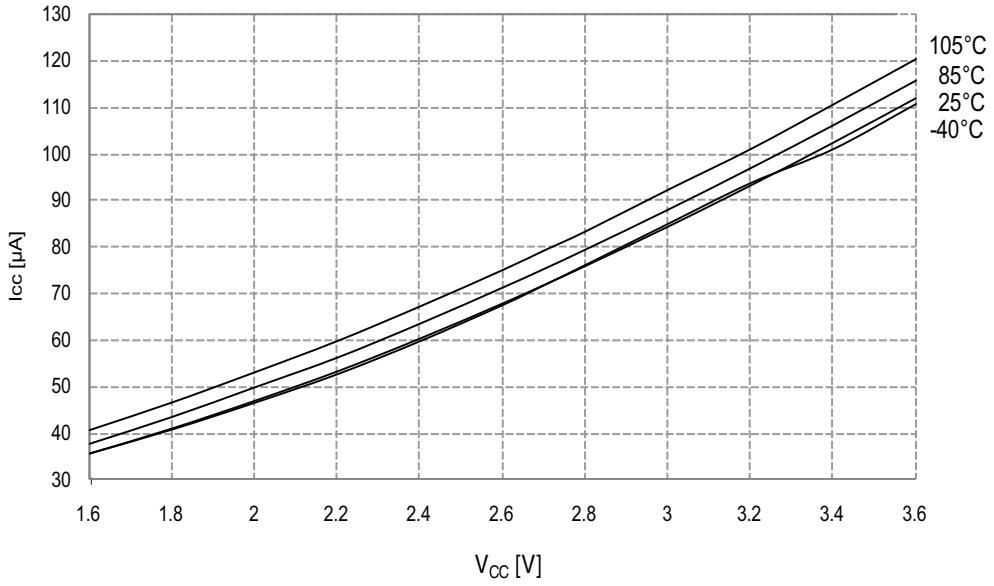
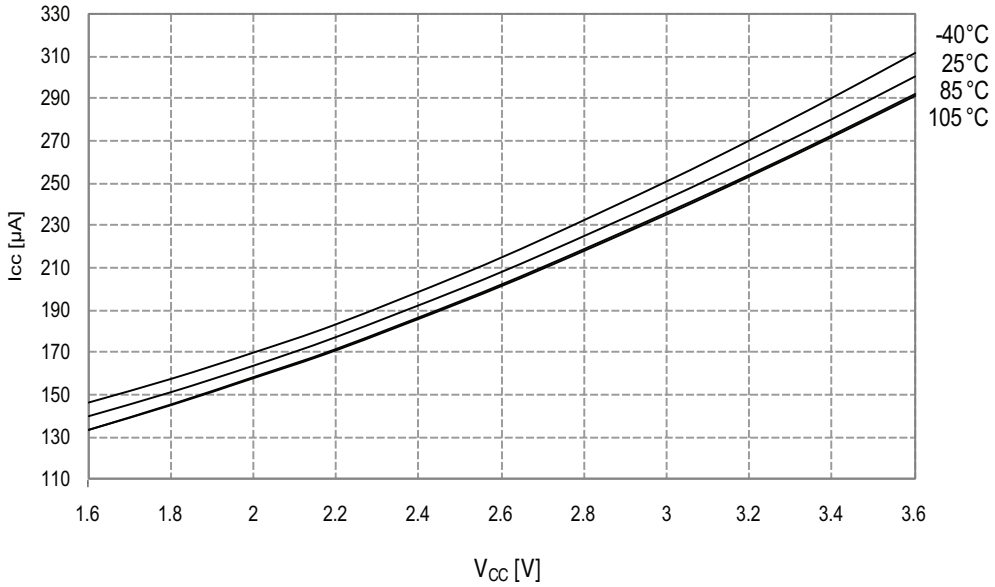


Figure 33-91. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator



33.2.2 I/O Pin Characteristics

33.2.2.1 Pull-up

Figure 33-100. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 1.8V

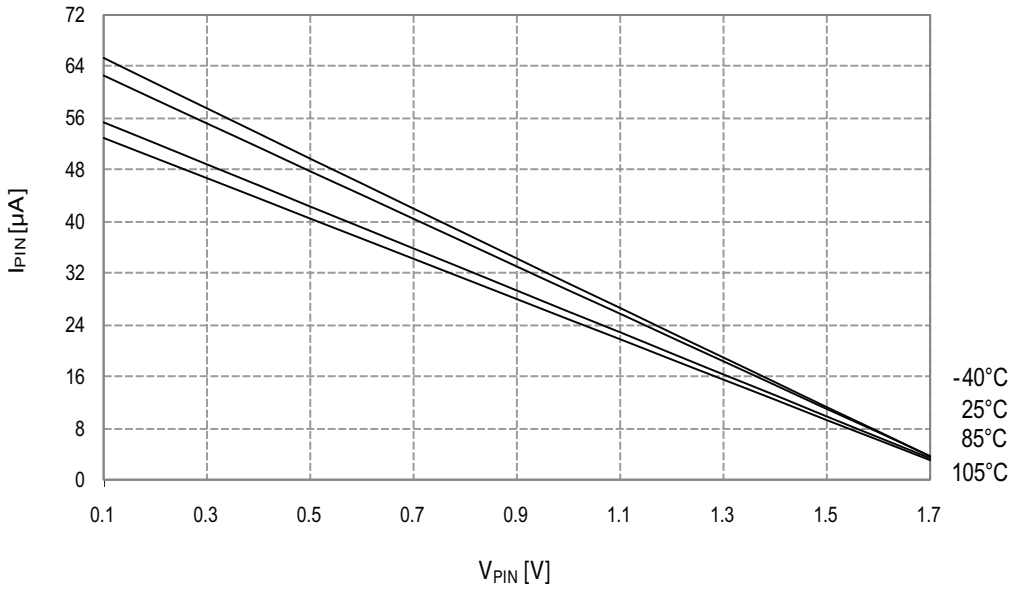


Figure 33-101. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.0V

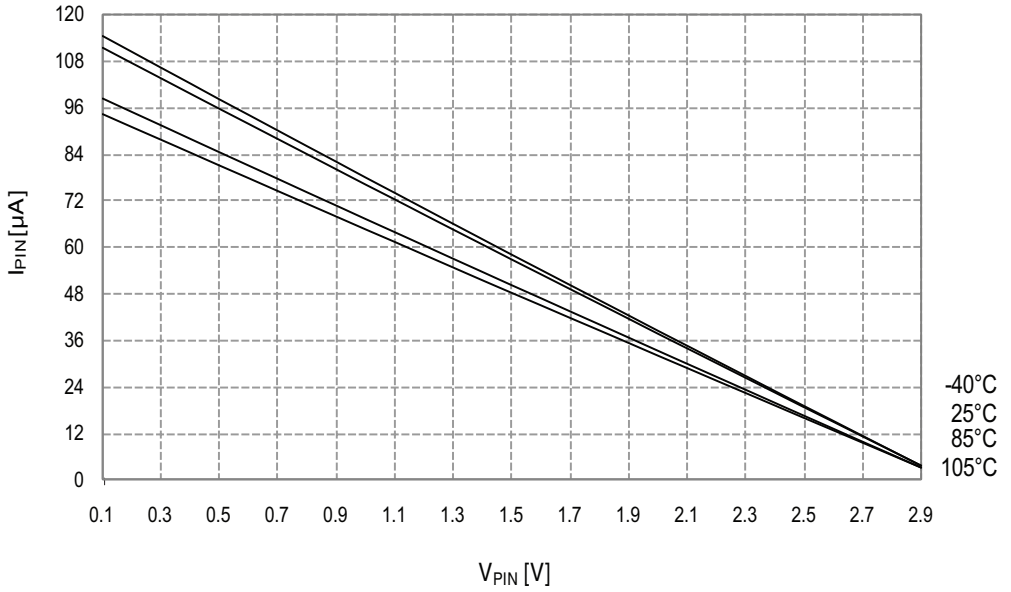


Figure 33-161. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

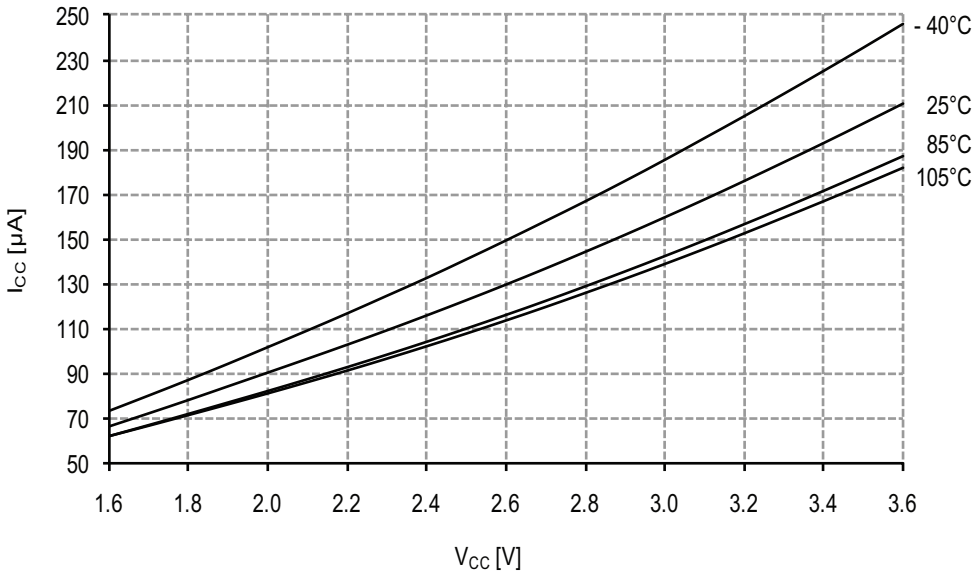


Figure 33-162. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

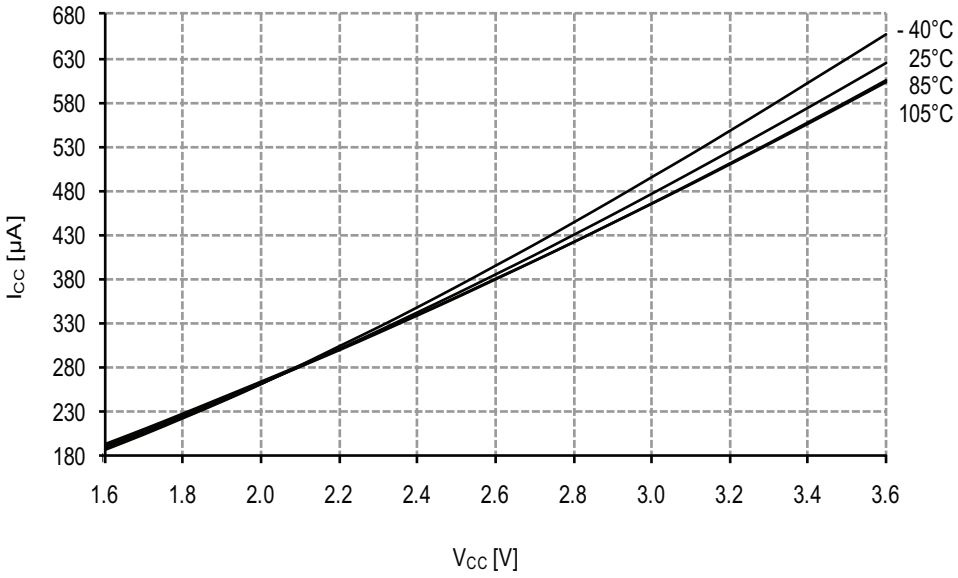


Figure 33-195. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external

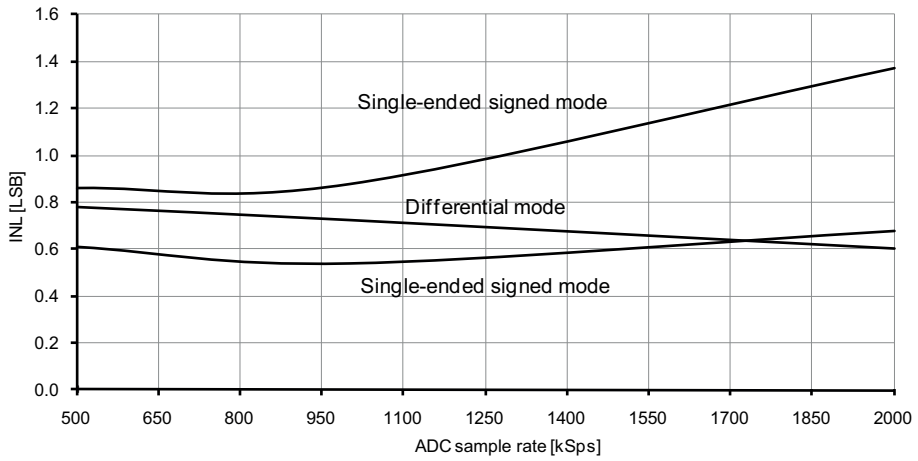


Figure 33-196. INL Error vs. Input Code

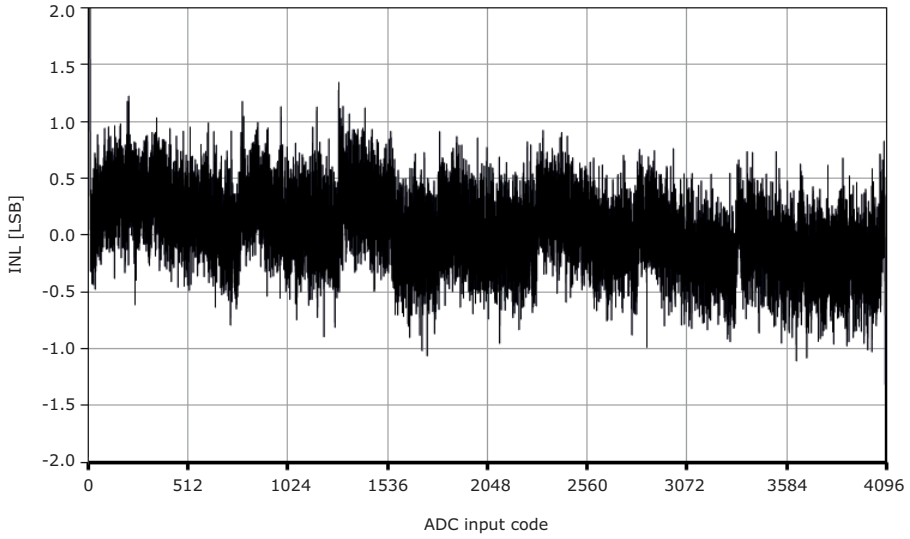


Figure 33-197. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

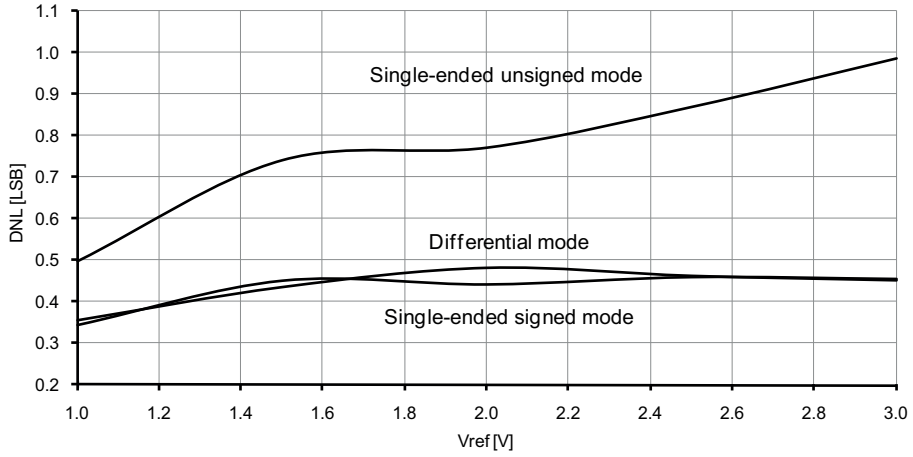


Figure 33-198. DNL Error vs. Sample rate

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external

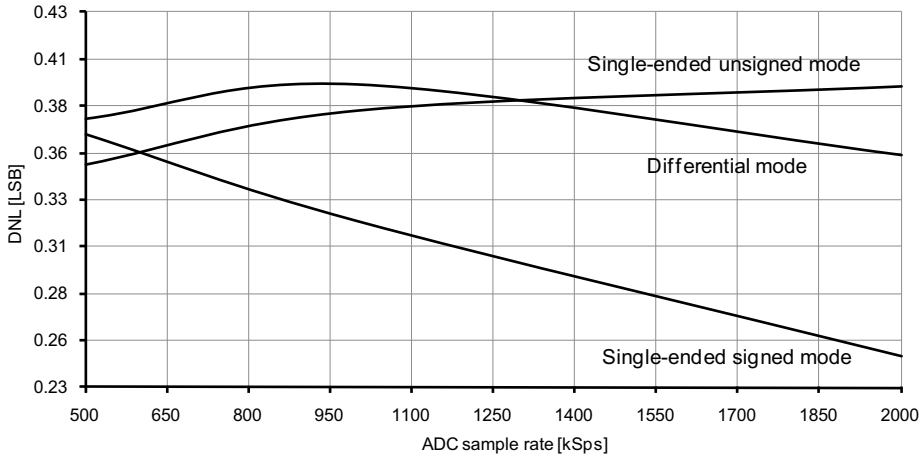


Figure 33-221. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V

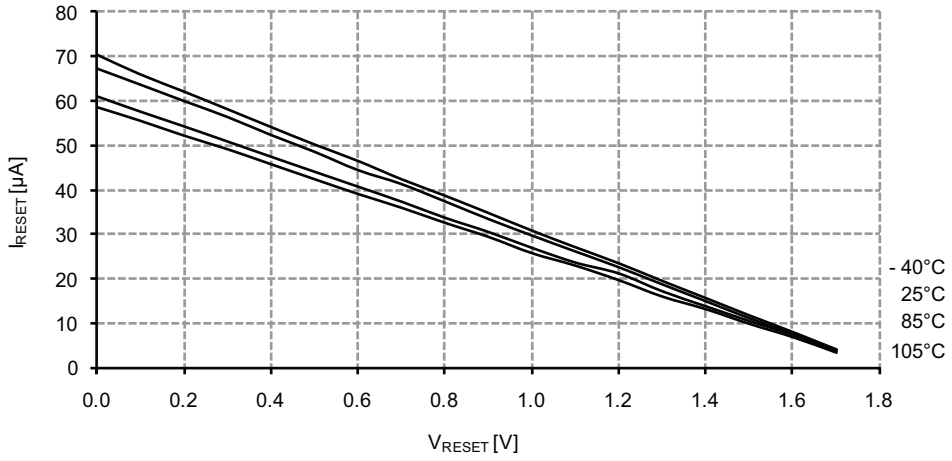
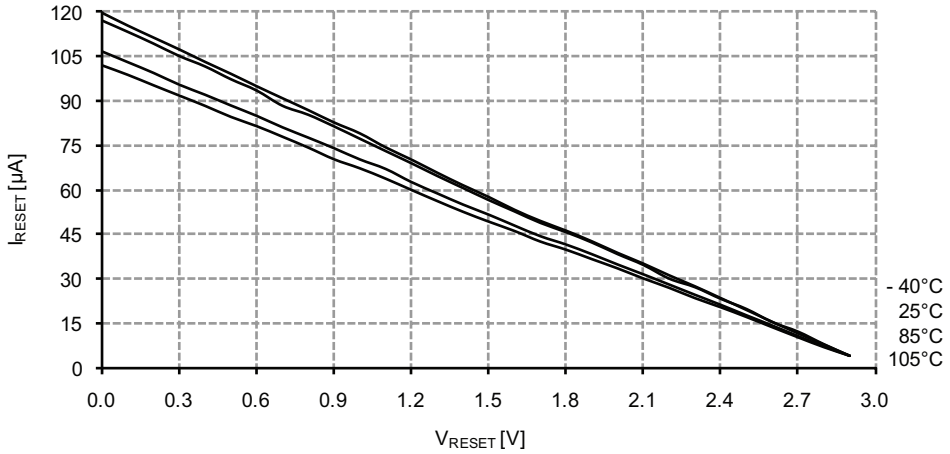


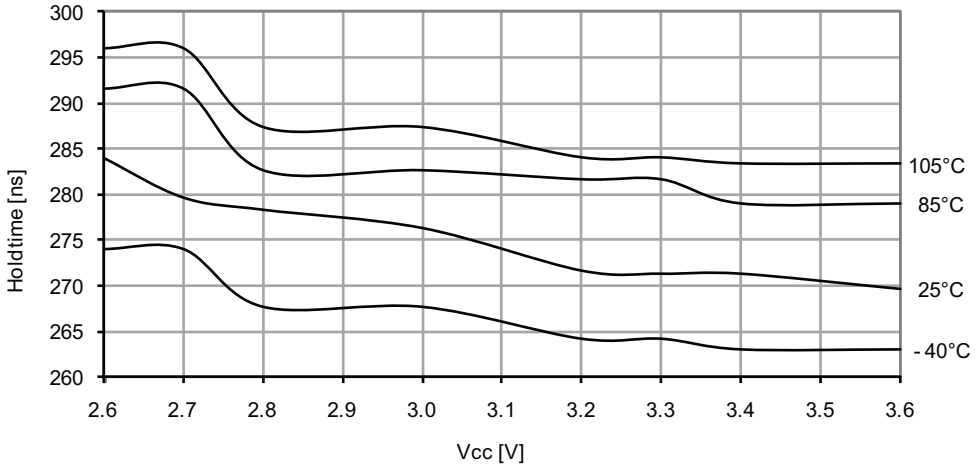
Figure 33-222. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.0V



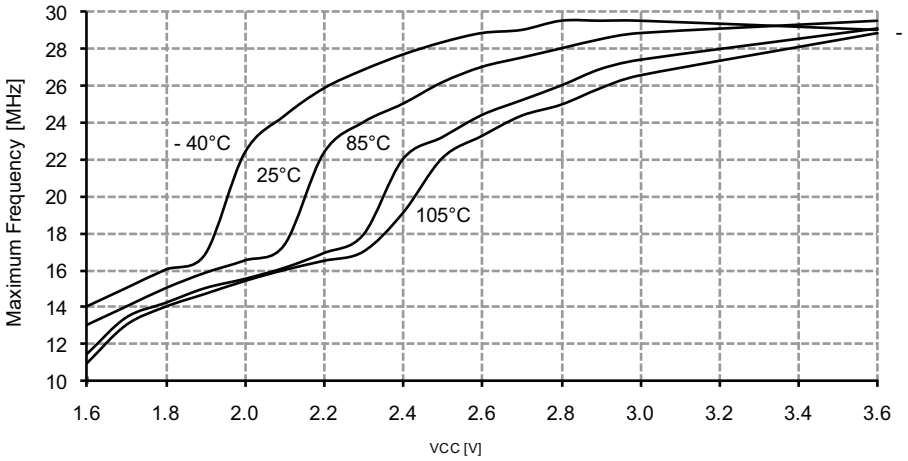
33.3.11 Two-Wire Interface Characteristics

Figure 33-241. SDA Hold Time vs. Supply Voltage



33.3.12 PDI Characteristics

Figure 33-242. Maximum PDI Frequency vs. V_{CC}



35. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

35.1 8135S – 09/2016

1.	Updated "Instruction Set Summary" on page 56. Removed "DES" instruction.
2.	Updated "Gain Stage Characteristics" : Table 32-11 on page 72, Table 32-39 on page 91Table 32-67 on page 110 and Table 32-96 on page 131. "Offset Error, input referred" is changed to "Offset Error, output referred.

35.2 8135R – 02/2015

1.	Updated Figure 25-1 on page 45
2.	Updated the "Packaging information" on page 61. Replaced "44M1" on page 62 by a correct package.
3.	Updated tables Table 32-8 on page 70and Table 32-36 on page 89 with information on fixed voltage offset.
4.	Updated use of capitals in heading, table headings and figure titles.

35.3 8135Q – 09/2014

1.	Updated the "Ordering Information" on page 2. Added ordering information for ATxmega16D4/32D4/64D4/128D4 @ 105°C.
2.	Updated the Application table section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 13
3.	Updated Table 32-4 on page 66, Table 32-33 on page 86, Table 32-60 on page 104 and Table 32-89 on page 125. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
4.	Updated Table 32-17 on page 74, Table 32-45 on page 93, Table 32-73 on page 112 and Table 32-102 on page 133. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
5.	Changed Vcc to AVcc in Figure 25-1 on page 45 and in the text in Section 25. "ADC – 12-bit Analog to Digital Converter" on page 44 and in Section 26. "AC – Analog Comparator" on page 46
6.	Changed unit parameter for $t_{SU;DAT}$ to ns in Table 32-28 on page 82, Table 32-56 on page 101, Table 32-85 on page 121 and Table 32-114 on page 142.
7.	Added ERRATA information on disabling of USART transmitter to Section 34.1 "ATxmega16D4 / ATxmega32D4" on page 308.
8.	Updated the typical characteristics of "ATxmega64D4" and "ATxmega128D4" with characterizations @105°C

35.4 8135P – 01/2014

1.	Updated the typical characteristics of "ATxmega16D4" and "ATxmega32D4" with characterizations @ 105°C

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