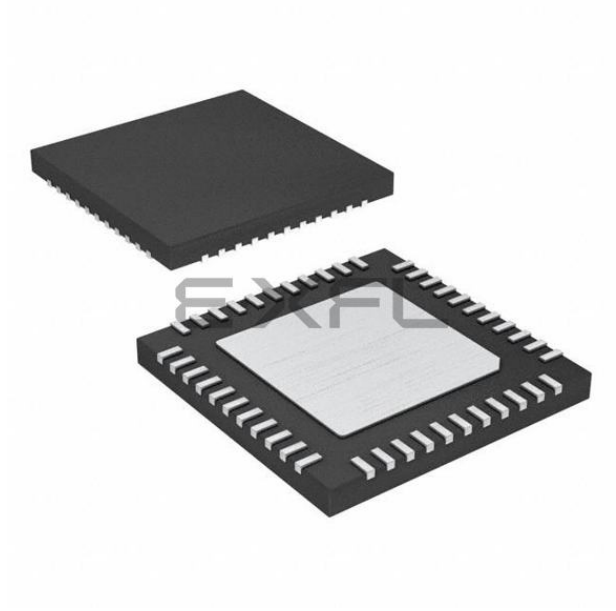


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8/16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 128KB (64K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VFQFN Exposed Pad |
| Supplier Device Package | 44-VQFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atxmega128d4-mh |

| Ordering Code | Flash (Bytes) | EEPROM (Bytes) | SRAM (Bytes) | Speed (MHz) | Power Supply | Package[1][2][3] | Temp |
|---|---|---|---|---|---|---|---|
| ATxmega128D4-AN | 128K + 8K | 2K | 8K | 32 | 1.6 - 3.6V | 44A | -40°C - 105°C |
| ATxmega128D4-ANR[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64D4-AN | 64K + 4K | 2K | 4K | | | | |
| ATxmega64D4-ANR[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32D4-AN | 32K + 4K | 1K | 4K | | | | |
| ATxmega32D4-ANR[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16D4-AN | 16K + 4K | 1K | 2K | | | | |
| ATxmega16D4-ANR[4] | 16K + 4K | 1K | 2K | | | | |
| ATxmega128D4-M7 | 128K + 8K | 2K | 8K | | | 44M1 | |
| ATxmega128D4-M7R[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64D4-M7 | 64K + 4K | 2K | 4K | | | | |
| ATxmega64D4-M7R[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32D4-M7 | 32K + 4K | 1K | 4K | | | | |
| ATxmega32D4-M7R[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16D4-M7 | 16K + 4K | 1K | 2K | | | | |
| ATxmega16D4-M7R[4] | 16K + 4K | 1K | 2K | | | | |

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information see "Packaging information" on page 64.
4. Tape and Reel.

| Package type | |
|---|---|
| **44A** | 44-lead, 10*10mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP) |
| **44M1** | 44-Pad, 7*7*1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN) |
| **49C2** | 49-ball (7 * 7 Array), 0.65mm pitch, 5.0*5.0*1.0mm, very thin, fine-pitch ball grid array package (VFBGA) |

## Typical Applications

| | | |
|---|---|---|
| Industrial control | Climate control | Low power battery applications |
| Factory automation | RF and ZigBee® | Power tools |
| Building control | USB connectivity | HVAC |
| Board control | Sensor control | Utility metering |
| White goods | Optical | Medical applications |

# 3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA device achieves throughputs CPU approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The AVR XMEGA D4 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 34 general purpose I/O lines, 16-bit real-time counter (RTC); four flexible, 16-bit timer/counters with compare and PWM channels; two USARTs; two two-wire serial interfaces (TWIs); two serial peripheral interfaces (SPIs); one twelve-channel, 12-bit ADC with optional differential input with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

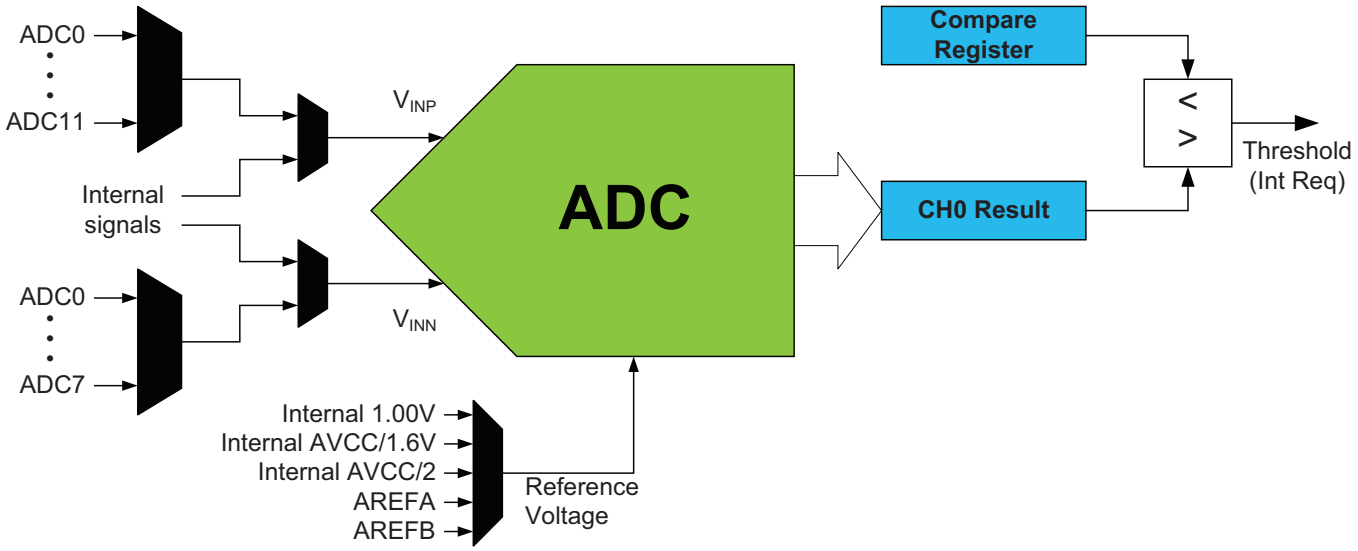
The XMEGA D4 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI interface. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

**Figure 25-1. ADC overview**




The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 5.0µs for 12-bit to 3.6µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

Notation of this peripheral is ADCA. The PORTA has ADCA inputs 0..7 and PORTB has ADCA inputs 8..11.

**Table 28-3. Port C - Alternate Functions**

| PORT C | PIN# | INTERRUPT | TCC0[1][2] | AWEXC | TCC1 | USARTC0[3] | SPIC[4] | TWIC | CLOCKOUT[5] | EVENTOUT[6] |
|---|---|---|---|---|---|---|---|---|---|---|
| **GND** | 8 | | | | | | | | | |
| **VCC** | 9 | | | | | | | | | |
| **PC0** | 10 | SYNC | OC0A | $\overline{\text{OC0ALS}}$ | | | | SDA | | |
| **PC1** | 11 | SYNC | OC0B | OC0AHS | | XCK0 | | SCL | | |
| **PC2** | 12 | SYNC/ASYNC | OC0C | $\overline{\text{OC0BLS}}$ | | RXD0 | | | | |
| **PC3** | 13 | SYNC | OC0D | OC0BHS | | TXD0 | | | | |
| **PC4** | 14 | SYNC | | $\overline{\text{OC0CLS}}$ | OC1A | | $\overline{\text{SS}}$ | | | |
| **PC5** | 15 | SYNC | | OC0CHS | OC1B | | MOSI | | | |
| **PC6** | 16 | SYNC | | $\overline{\text{OC0DLS}}$ | | | MISO | | $\text{clk}_{\text{RTC}}$ | |
| **PC7** | 17 | SYNC | | OC0DHS | | | SCK | | $\text{clk}_{\text{PER}}$ | EVOUT |

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D and E and between pin 4 and 7.

**Table 28-4. Port D - Alternate Functions**

| PORT D | PIN # | INTERRUPT | TCD0 | USARTD0 | SPID | CLOCKOUT | EVENTOUT |
|---|---|---|---|---|---|---|---|
| **GND** | 18 | | | | | | |
| **VCC** | 19 | | | | | | |
| **PD0** | 20 | SYNC | OC0A | | | | |
| **PD1** | 21 | SYNC | OC0B | XCK0 | | | |
| **PD2** | 22 | SYNC/ASYNC | OC0C | RXD0 | | | |
| **PD3** | 23 | SYNC | OC0D | TXD0 | | | |
| **PD4** | 24 | SYNC | | | $\overline{\text{SS}}$ | | |
| **PD5** | 25 | SYNC | | | MOSI | | |
| **PD6** | 26 | SYNC | | | MISO | | |
| **PD7** | 27 | SYNC | | | SCK | $\text{clk}_{\text{PER}}$ | EVOUT |

**Table 28-5. Port E - Alternate Functions**

| PORT E | PIN # | INTERRUPT | TCE0 | TWIE |
|---|---|---|---|---|
| **PE0** | 28 | SYNC | OC0A | SDA |
| **PE1** | 29 | SYNC | OC0B | SCL |
| **GND** | 30 | | | |

### 32.1.6 ADC Characteristics

**Table 32-8. Power Supply, Reference and Input Range**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $V_{REF}$ | Reference voltage | | 1 | | $AV_{CC}$- 0.6 | |
| $R_{in}$ | Input resistance | Switched | | | 4.5 | kΩ |
| $C_{in}$ | Input capacitance | Switched | | | 5 | pF |
| $R_{AREF}$ | Reference input resistance | (leakage only) | | >10 | | MΩ |
| $C_{AREF}$ | Reference input capacitance | Static load | | 7 | | pF |
| Vin | Input range | | 0 | | $V_{REF}$ | V |
| | Conversion range | Differential mode, Vinp - Vinn | $-V_{REF}$ | | $V_{REF}$ | |
| | Conversion range | Single ended unsigned mode, Vinp | -ΔV | | $V_{REF}$-ΔV | |
| ΔV | Fixed offset voltage | | | 200 | | LSB |

**Table 32-9. Clock and Timing**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{ADC}$ | ADC clock frequency | Maximum is 1/4 of peripheral clock frequency | 100 | | 1800 | kHz |
| | | Measuring internal signals | | 125 | | |
| $f_{ClkADC}$ | Sample rate | | 16 | | 300 | ksps |
| $f_{ADC}$ | Sample rate | Current limitation (CURRLIMIT) off | | | 300 | |
| | | CURRLIMIT = LOW | | | 250 | |
| | | CURRLIMIT = MEDIUM | | | 150 | |
| | | CURRLIMIT = HIGH | | | 50 | |
| | Sampling time | Configurable in steps of 1/2 $Clk_{ADC}$ cycles up to 32 $Clk_{ADC}$ cycles | 0.28 | | 320 | µs |
| | Conversion time (latency) | (RES+1)/2 + GAIN<br>RES (Resolution) = 8 or 12, GAIN=0 to 3 | 4.5 | | 10 | $Clk_{ADC}$ cycles |
| | Start-up time | ADC clock cycles | | 12 | 24 | |
| | ADC settling time | After changing reference or input mode | | 7 | 7 | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_Q$ | Negative impedance | XOSCPWR=1, FRQRANGE=1, CL=20pF | 9MHz crystal | | 1500 | | Ω |
| | | | 12MHz crystal | | 650 | | |
| | | | 16MHz crystal | | 270 | | |
| | | XOSCPWR=1, FRQRANGE=2, CL=20pF | 12MHz crystal | | 1000 | | |
| | | | 16MHz crystal | | 440 | | |
| | | XOSCPWR=1, FRQRANGE=3, CL=20pF | 12MHz crystal | | 1300 | | |
| | | | 16MHz crystal | | 590 | | |
| | ESR | SF = safety factor | | | | min($R_Q$)/SF | kΩ |
| | Start-up time | XOSCPWR=0, FRQRANGE=0 | 0.4MHz resonator, CL=100pF | | 1.0 | | ms |
| | | XOSCPWR=0, FRQRANGE=1 | 2MHz crystal, CL=20pF | | 2.6 | | |
| | | XOSCPWR=0, FRQRANGE=2 | 8MHz crystal, CL=20pF | | 0.8 | | |
| | | XOSCPWR=0, FRQRANGE=3 | 12MHz crystal, CL=20pF | | 1.0 | | |
| | | XOSCPWR=1, FRQRANGE=3 | 16MHz crystal, CL=20pF | | 1.4 | | |
| $C_{XTAL1}$ | Parasitic capacitance XTAL1 pin | | | | 5.9 | | pF |
| $C_{XTAL2}$ | Parasitic capacitance XTAL2 pin | | | | 8.3 | | |
| $C_{LOAD}$ | Parasitic capacitance load | | | | 3.5 | | |

### 32.1.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

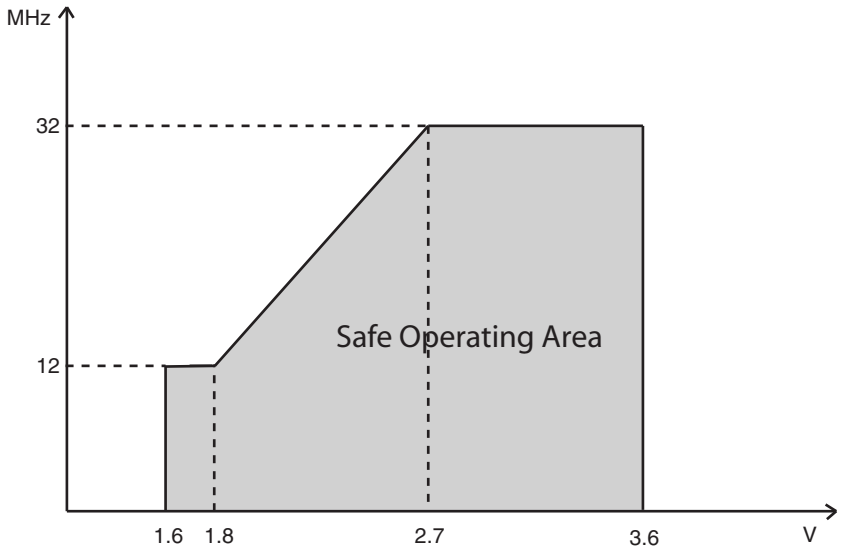
**Table 32-26. External 32.768kHz Crystal Oscillator and TOSC Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ESR/R1 | Recommended crystal equivalent series resistance (ESR) | Crystal load capacitance 6.5pF | | | 60 | kΩ |
| | | Crystal load capacitance 9.0pF | | | 35 | |
| | | Crystal load capacitance 12pF | | | 28 | |
| $C_{TOSC1}$ | Parasitic capacitance TOSC1 pin | | | 3.5 | | pF |
| $C_{TOSC2}$ | Parasitic capacitance TOSC2 pin | | | 3.5 | | |
| | Recommended safety factor | capacitance load matched to crystal specification | 3 | | | |

Note: See Figure 32-4 for definition.

The maximum CPU clock frequency depends on $V_{CC}$. As shown in Figure 32-15 the Frequency vs. $V_{CC}$ curve is linear between $1.8V < V_{CC} < 2.7V$.

**Figure 32-15.Maximum Frequency vs. $V_{CC}$**



### 32.3.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

**Table 32-77. 32MHz Internal Oscillator Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 30 | | 55 | MHz |
| | Factory calibrated frequency | | | 32 | | |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | |
| | DFLL calibration step size | | | 0.22 | | |

### 32.3.13.4 32kHz Internal ULP Oscillator Characteristics

**Table 32-78. 32kHz Internal ULP Oscillator Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Factory calibrated frequency | | | 32 | | kHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -12 | | 12 | % |
| | Accuracy | | -30 | | 30 | |

### 32.3.13.5 Internal Phase Locked Loop (PLL) Characteristics

**Table 32-79. Internal PLL Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input frequency | Output frequency must be within $f_{OUT}$ | 0.4 | | 64 | MHz |
| $f_{OUT}$ | Output frequency(1) | $V_{CC}$= 1.6 - 1.8V | 20 | | 48 | |
| | | $V_{CC}$= 2.7 - 3.6V | 20 | | 128 | |
| | Start-up time | | | 25 | | µs |
| | Re-lock time | | | 25 | | |

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 32.3.13.6 External Clock Characteristics

**Figure 32-17.External Clock Drive Waveform**

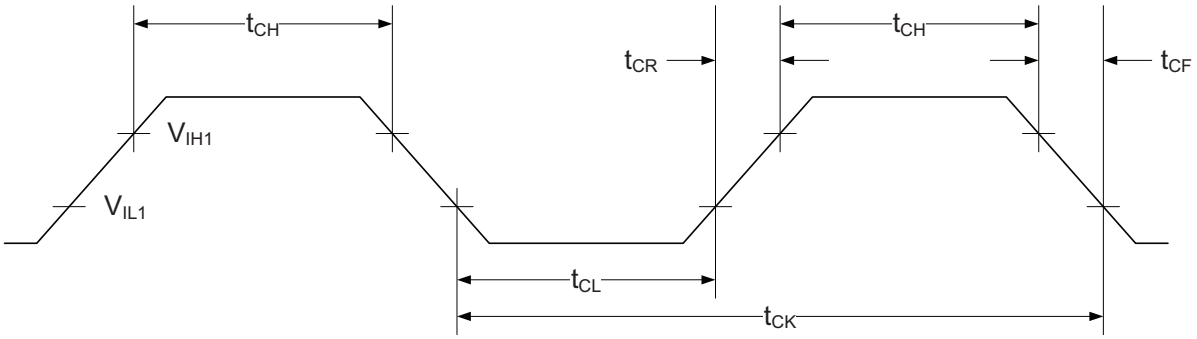



**Table 32-80. External Clock Used as System Clock without Prescaling**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock frequency[1] | $V_{CC}$ = 1.6 - 1.8V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 32 | |
| $t_{CK}$ | Clock period | $V_{CC}$ = 1.6 - 1.8V | 83.3 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 31.5 | | | |
| $t_{CH}$ | Clock high time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CL}$ | Clock low time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CR}$ | Rise time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $t_{CF}$ | Fall time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Note: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.

**Table 32-84. SPI Timing Characteristics and Requirements**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SCK period | Master | | (See Table 17-4 in XMEGA D Manual) | | ns |
| $t_{SCKW}$ | SCK high/low width | Master | | 0.5*SCK | | |
| $t_{SCKR}$ | SCK rise time | Master | | 2.7 | | |
| $t_{SCKF}$ | SCK fall time | Master | | 2.7 | | |
| $t_{MIS}$ | MISO setup to SCK | Master | | 10 | | |
| $t_{MIH}$ | MISO hold after SCK | Master | | 10 | | |
| $t_{MOS}$ | MOSI setup SCK | Master | | 0.5*SCK | | |
| $t_{MOH}$ | MOSI hold after SCK | Master | | 1 | | |
| $t_{SSCK}$ | Slave SCK period | Slave | 4*t $Clk_{PER}$ | | | |
| $t_{SSCKW}$ | SCK high/low width | Slave | 2*t $Clk_{PER}$ | | | |
| $t_{SSCKR}$ | SCK rise time | Slave | | | 1600 | |
| $t_{SSCKF}$ | SCK fall time | Slave | | | 1600 | |
| $t_{SIS}$ | MOSI setup to SCK | Slave | 3 | | | |
| $t_{SIH}$ | MOSI hold after SCK | Slave | t $Clk_{PER}$ | | | |
| $t_{SSS}$ | $\overline{SS}$ setup to SCK | Slave | 21 | | | |
| $t_{SSH}$ | $\overline{SS}$ hold after SCK | Slave | 20 | | | |
| $t_{SOS}$ | MISO setup SCK | Slave | | 8.0 | | |
| $t_{SOH}$ | MISO hold after SCK | Slave | | 13.0 | | |
| $t_{SOSS}$ | MISO setup after $\overline{SS}$ low | Slave | | 11.0 | | |
| $t_{SOSH}$ | MISO hold after $\overline{SS}$ high | Slave | | 8.0 | | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{HD;STA}$ | Hold time (repeated) START condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{LOW}$ | Low period of SCL clock | $f_{SCL} \leq 100kHz$ | 4.7 | | | |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |
| $t_{HIGH}$ | High period of SCL clock | $f_{SCL} \leq 100kHz$ | 4.0 | | | |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{HD;DAT}$ | Data hold time | $f_{SCL} \leq 100kHz$ | 0 | | 3.45 | µs |
| | | $f_{SCL} > 100kHz$ | 0 | | 0.9 | |
| $t_{SU;DAT}$ | Data setup time | $f_{SCL} \leq 100kHz$ | 250 | | | ns |
| | | $f_{SCL} > 100kHz$ | 100 | | | |
| $t_{SU;STO}$ | Setup time for STOP condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. $C_b$ = Capacitance of one bus line in pF.
3. $f_{PER}$ = Peripheral clock frequency.

### 33.2.1.3 Power-down Mode Supply Current

**Figure 33-94. Power-down Mode Supply Current vs. $V_{CC}$**

***All functions disabled***

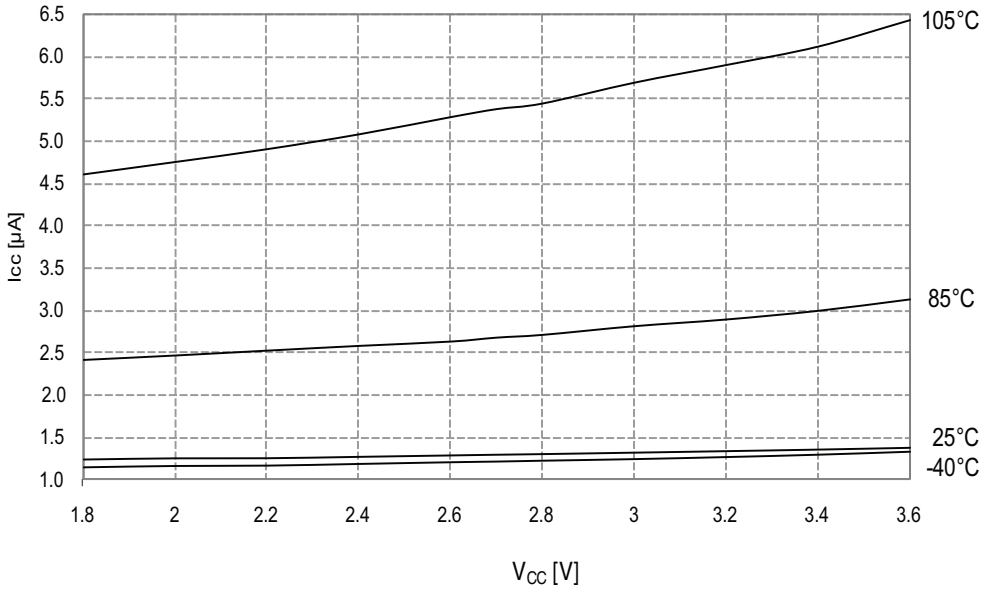



**Figure 33-95. Power-down Mode Supply Current vs. $V_{CC}$**

***Watchdog and sampled BOD enabled***

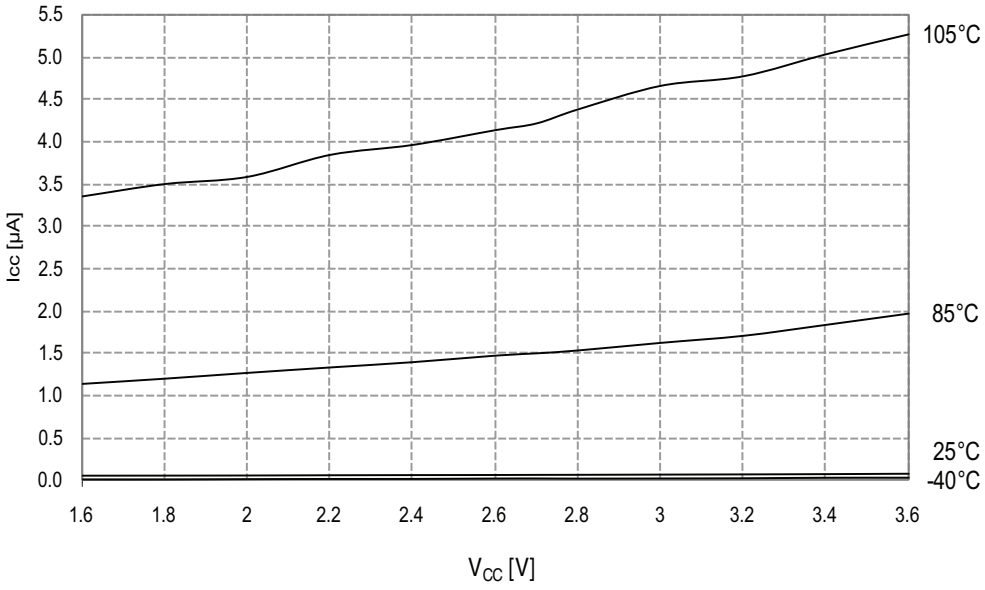


**Figure 33-140. Reset Pin Input Threshold Voltage vs. $V_{CC}$**

***$V_{IH}$ - Reset pin read as "1"***

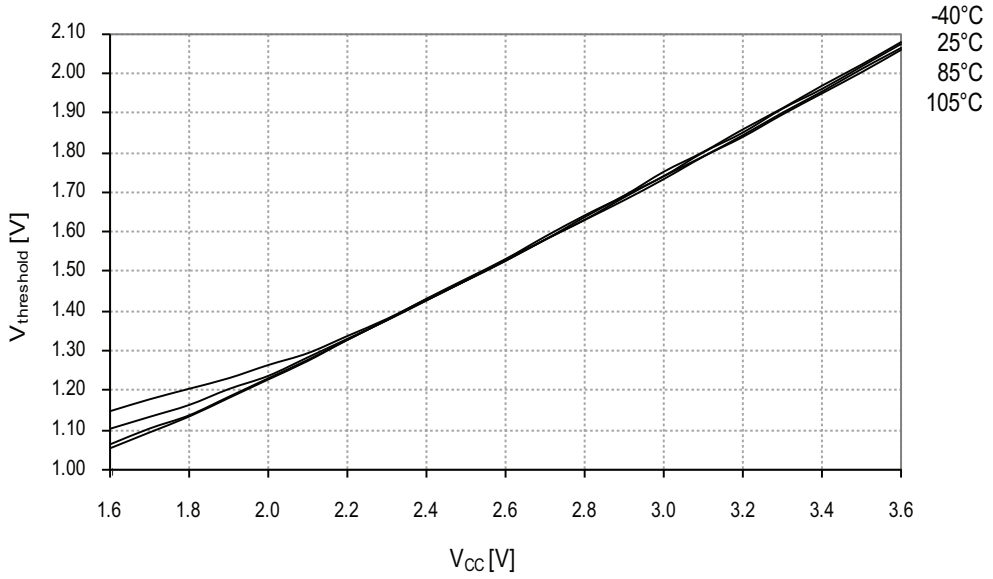
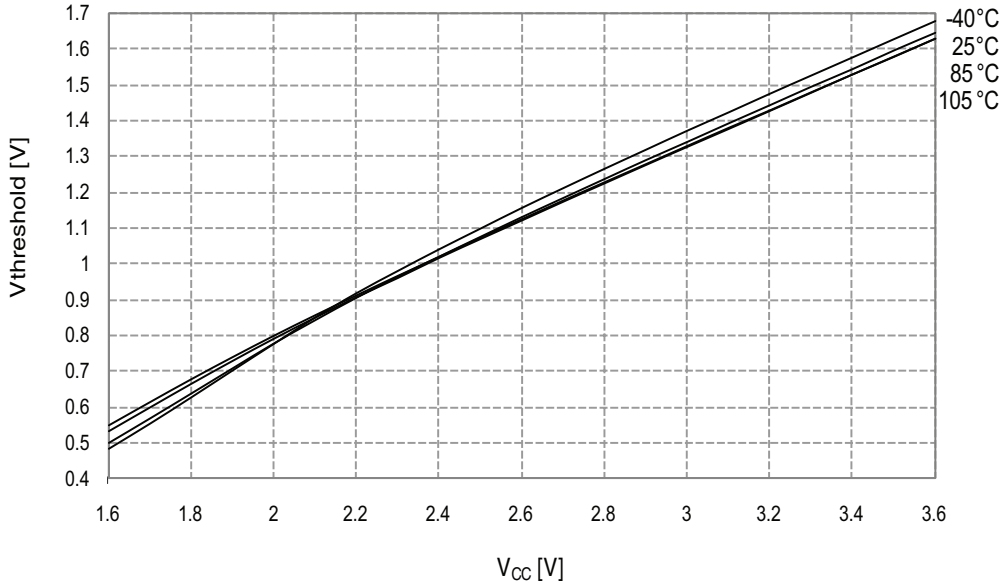



**Figure 33-141. Reset Pin Input Threshold Voltage vs. $V_{CC}$**

***$V_{IL}$ - Reset pin read as "0"***



## 33.3.2 I/O Pin Characteristics

### 33.3.2.1 Pull-up

**Figure 33-179. I/O Pin Pull-up Resistor Current vs. Input Voltage**

$V_{CC}$ = 1.8V

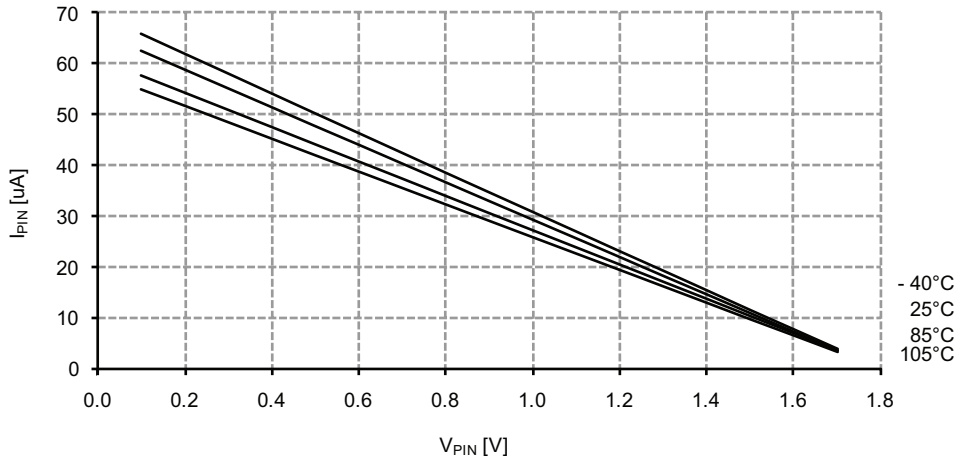



**Figure 33-180. I/O Pin Pull-up Resistor Current vs. Input Voltage**

$V_{CC}$ = 3.0V

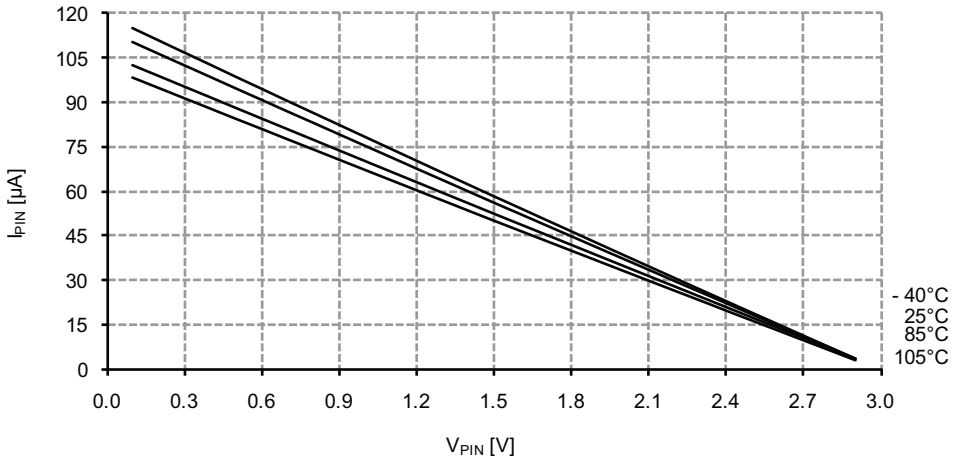
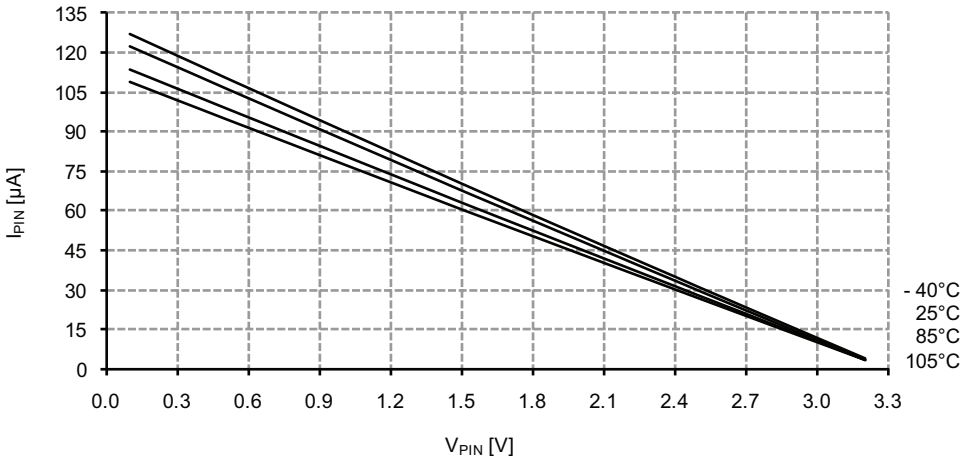


**Figure 33-181. I/O Pin Pull-up Resistor Current vs. Input Voltage**

$V_{CC}$ = 3.3V




### 33.3.2.2 Output Voltage vs. Sink/Source Current

**Figure 33-182. I/O Pin Output Voltage vs. Source Current**

$V_{CC}$ = 1.8V

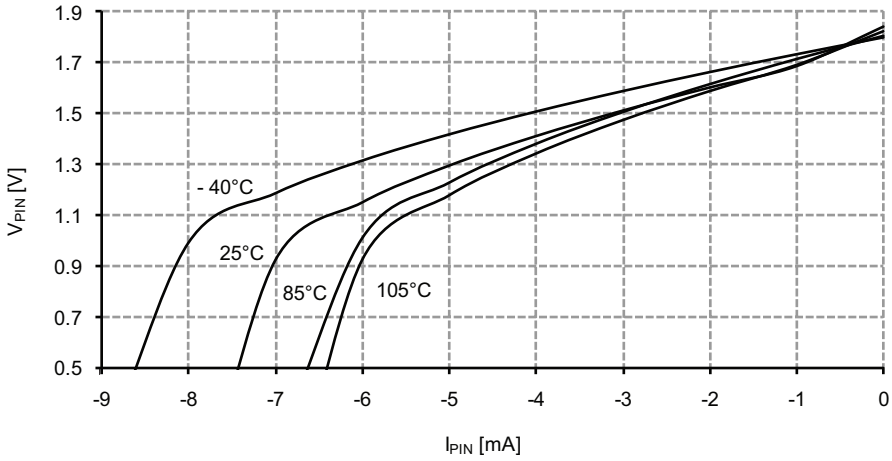


**Figure 33-203. Gain Error vs. Temperature**

***$V_{CC}$ = 2.7V, $V_{REF}$ = external 1.0V***

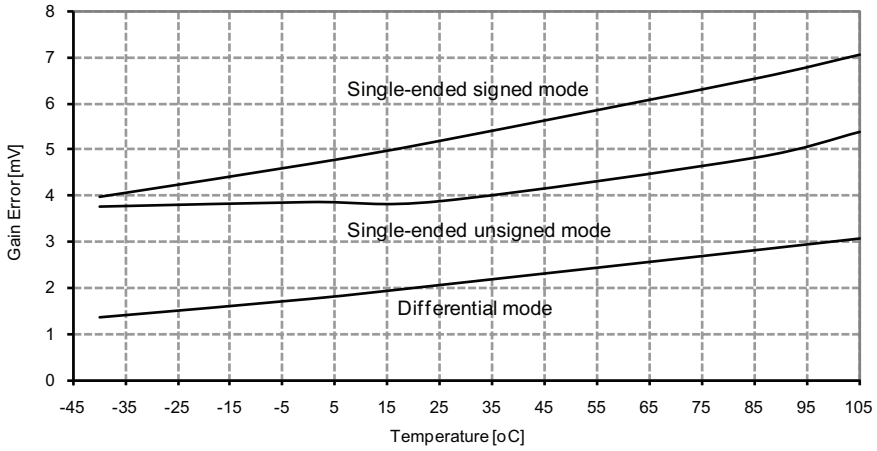



**Figure 33-204. Offset Error vs. $V_{CC}$**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps***

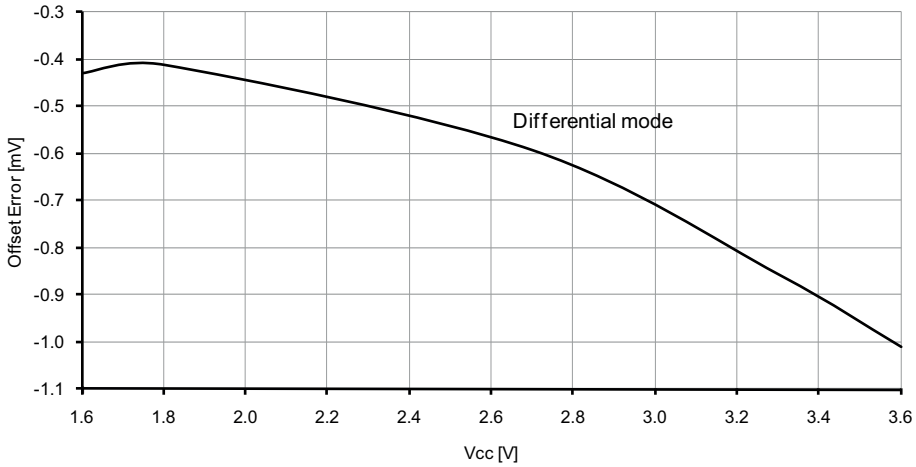


**Figure 33-223. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage**

***$V_{CC}$ = 3.3V***

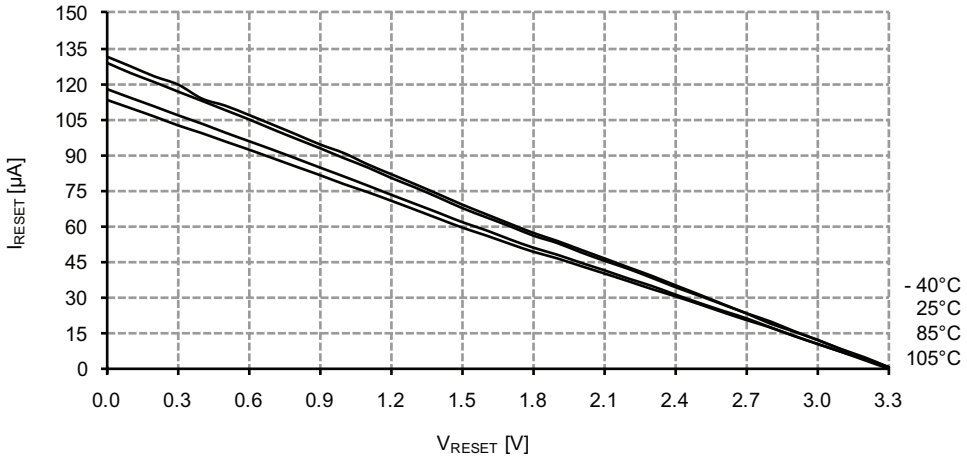



**Figure 33-224. Reset Pin Input Threshold Voltage vs. $V_{CC}$**

***$V_{IH}$ - Reset pin read as "1"***

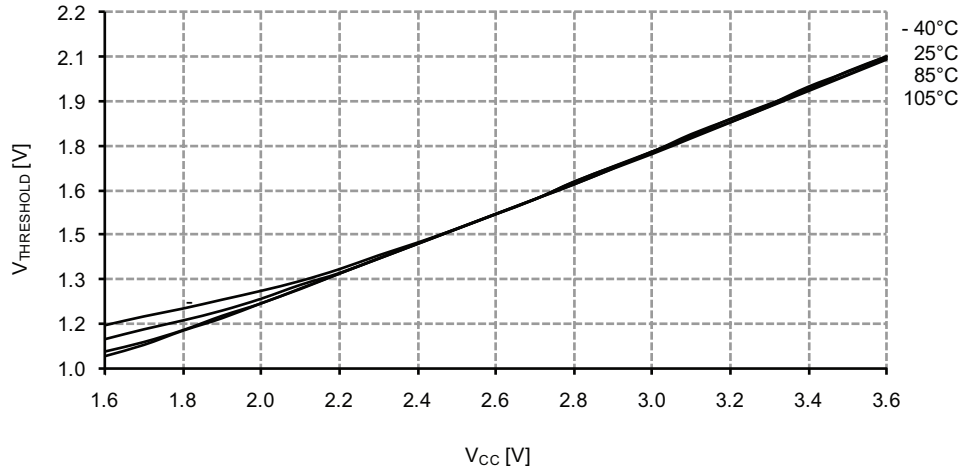


**Figure 33-255. Idle Mode Supply Current vs. $V_{CC}$**

*$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz*

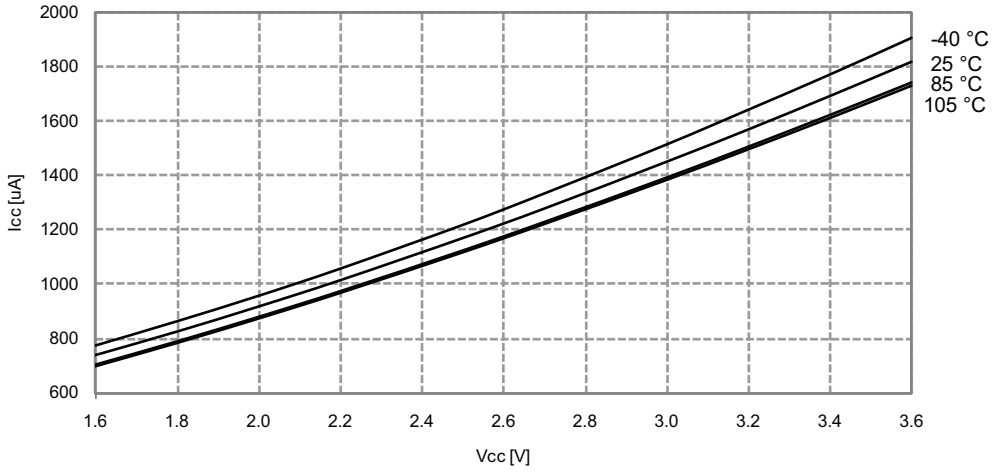
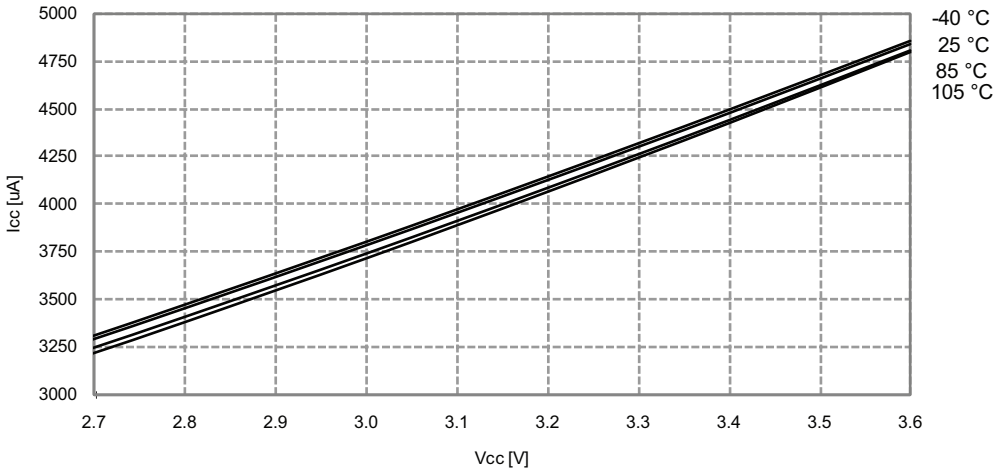



**Figure 33-256. Idle Mode Current vs. $V_{CC}$**

*$f_{SYS}$ = 32MHz internal oscillator*



### Problem fix/Workaround

**Table 34-1. Configure PWM and CWCM According to this Table**

| PGM | CWCM | Description |
|---|---|---|
| 0 | 0 | PGM and CWCM disabled |
| 0 | 1 | PGM enabled |
| 1 | 0 | PGM and CWCM enabled |
| 1 | 1 | PGM enabled |

## 10 PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

### Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

## 11. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

### Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

## 12. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC and Analog Comparator.

### Problem fix/Workaround

If the bandgap is used as reference for either the ADC or the Analog Comparator, the BOD must not be set in sampled mode.

## 13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

### Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

## 14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

### Problem fix/Workaround

None.

## 15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

***Table of Contentsi***