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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128d4-mnr

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA device achieves throughputs CPU approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The AVR XMEGA D4 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 34 general purpose I/O lines, 16-bit real-time counter (RTC); four flexible, 16-bit timer/counters with compare and PWM channels; two USARTs; two two-wire serial interfaces (TWIs); two serial peripheral interfaces (SPIs); one twelve-channel, 12-bit ADC with optional differential input with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The XMEGA D4 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI interface. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

6. AVR CPU

6.1 Features

- 8/16-bit, high-performance Atmel AVR RISC CPU
 - 137 instructions
 - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Stack pointer accessible in I/O memory space
- Direct addressing of up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8-, 16-, and 32-bit arithmetic
- Configuration change protection of system-critical features

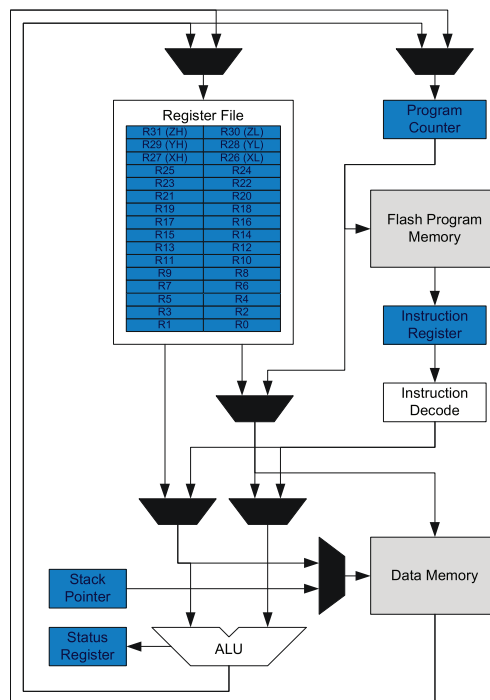
6.2 Overview

All Atmel AVR XMEGA devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program in the flash memory. Interrupt handling is described in a separate section, refer to “[Interrupts and Programmable Multilevel Interrupt Controller](#)” on page 27.

6.3 Architectural Overview

In order to maximize performance and parallelism, the AVR CPU uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This enables instructions to be executed on every clock cycle. For details of all AVR instructions, refer to <http://www.atmel.com/avr>.

Figure 6-1. Block Diagram of the AVR CPU Architecture



The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit arithmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

13. Interrupts and Programmable Multilevel Interrupt Controller

13.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
 - Interrupt prioritizing according to level and vector address
 - Three selectable interrupt levels for all interrupts: low, medium and high
 - Selectable, round-robin priority scheme within low-level interrupts
 - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

13.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

13.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA D4 devices are shown in [Table 13-1 on page 28](#). Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA D manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in [Table 13-1 on page 28](#). The program address is the word address.

Table 32-5. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition ⁽¹⁾	Min.	Typ.	Max.	Units
I _{CC}	ULP oscillator			0.8		μA
	32.768kHz int. oscillator			29		
	2MHz int. oscillator			85		
		DFLL enabled with 32.768kHz int. osc. as reference		115		
	32MHz int. oscillator			245		
		DFLL enabled with 32.768kHz int. osc. as reference		410		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference		290		
	Watchdog timer			1.0		
	BOD	Continuous mode		138		
		Sampled mode, includes ULP oscillator		1.2		
	Internal 1.0V reference			175		mA
	Temperature sensor			170		
	ADC	16ksps V _{REF} = Ext ref		1.2		
			CURRLIMIT = LOW	1.0		
			CURRLIMIT = MEDIUM	0.9		
			CURRLIMIT = HIGH	0.8		
		75ksps V _{REF} = Ext ref	CURRLIMIT = LOW	1.7		
		200ksps V _{REF} = Ext ref		3.1		
	USART	Rx and Tx enabled, 9600 BAUD		11		μA
	Flash memory and EEPROM programming			4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

32.1.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 32-23. Internal PLL Characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.1.13.6 External Clock Characteristics

Figure 32-3. External Clock Drive Waveform

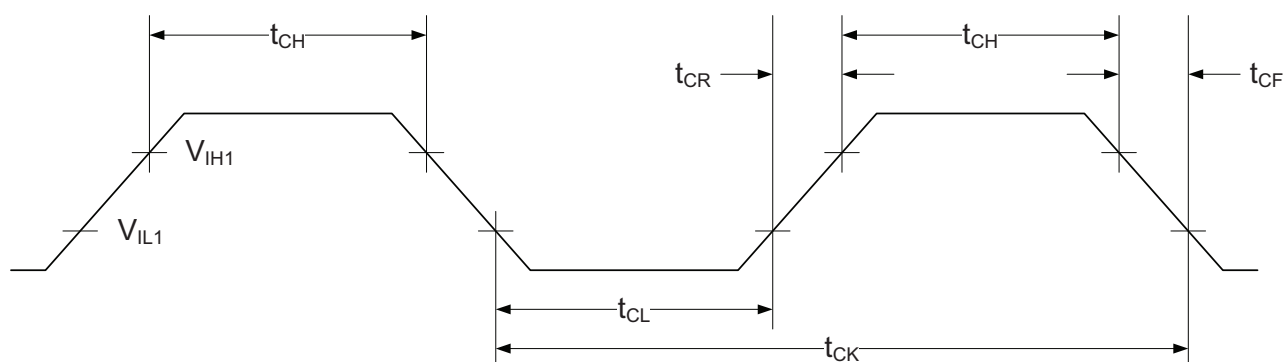


Table 32-24. External Clock⁽¹⁾

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency ⁽²⁾	$V_{CC} = 1.6 - 1.8V$	0		90	MHz
		$V_{CC} = 2.7 - 3.6V$	0		142	
t_{CK}	Clock period	$V_{CC} = 1.6 - 1.8V$	11			ns
		$V_{CC} = 2.7 - 3.6V$	7.0			
$t_{CH/CL}$	Clock high/low time	$V_{CC} = 1.6 - 1.8V$	4.5			
		$V_{CC} = 2.7 - 3.6V$	2.4			
$V_{IL/IH}$	Low/high level input voltage		See Table 32-7 on page 69			V
Δt_{CK}	Reduction in period time from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-56. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ ⁽¹⁾			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ ⁽¹⁾⁽²⁾		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ ⁽²⁾	$20+0.1C_b$ ⁽¹⁾⁽²⁾		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	μA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} ⁽³⁾ $> \max(10f_{SCL}, 250kHz)$	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			μs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	μs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			ns
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			μs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			μs
		$f_{SCL} > 100kHz$	1.3			

- Notes:
1. Required only for $f_{SCL} > 100kHz$.
 2. C_b = Capacitance of one bus line in pF.
 3. f_{PER} = Peripheral clock frequency.

32.3.6 ADC Characteristics

Table 32-64. Power Supply, Reference and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		$V_{CC} - 0.3$		$V_{CC} + 0.3$	V
V_{REF}	Reference voltage		1.0		$AV_{CC} - 0.6$	
R_{in}	Input resistance	Switched		4.0		k Ω
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		M Ω
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		$AV_{CC} + 0.1$	V
	Conversion range	Differential mode, $V_{inp} - V_{inn}$	$-V_{REF}$		V_{REF}	
V_{IN}	Conversion range	Single ended unsigned mode, V_{inp}	$-\Delta V$		$V_{REF} - \Delta V$	
ΔV	Fixed offset voltage			190		LSB

Table 32-65. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		1400	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate				200	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off			200	
		CURRLIMIT = LOW	14		150	
		CURRLIMIT = MEDIUM			100	
		CURRLIMIT = HIGH			50	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	μs
	Conversion time (latency)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0, 1, 2 or 3	5	7	10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	
		After ADC flush		1	1	

32.3.10 External Reset Characteristics

Table 32-71. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	95		ns
V_{RST}	Reset threshold voltage (V_{IH})	$V_{CC} = 2.7 - 3.6V$	$0.60 \cdot V_{CC}$			V
		$V_{CC} = 1.6 - 2.7V$	$0.60 \cdot V_{CC}$		$0.50 \cdot V_{CC}$	
	Reset threshold voltage (V_{IL})	$V_{CC} = 2.7 - 3.6V$			$0.40 \cdot V_{CC}$	
		$V_{CC} = 1.6 - 2.7V$			$0.50 \cdot V_{CC}$	
R_{RST}	Reset pin pull-up resistor			25		k Ω

32.3.11 Power-on Reset Characteristics

Table 32-72. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{POT-}^{(1)}$	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.3.12 Flash and EEPROM Memory Characteristics

Table 32-73. Endurance and Data Retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K		Cycle
			85°C	10K		
			105°C	2K		
		Data retention	25°C	100		Year
			85°C	25		
			105°C	10		
	EEPROM	Write/Erase cycles	25°C	100K		Cycle
			85°C	100K		
			105°C	30K		
		Data retention	25°C	100		Year
			85°C	25		
			105°C	10		

32.4 ATxmega128D4

32.4.1 Absolute Maximum Ratings

Stresses beyond those listed in [Table 32-86](#) under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-86. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		$V_{CC}+0.5$	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_J	Junction temperature				150	

32.4.2 General Operating Ratings

The device must operate within the ratings listed in [Table 32-87](#) in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-87. General Operating Conditions

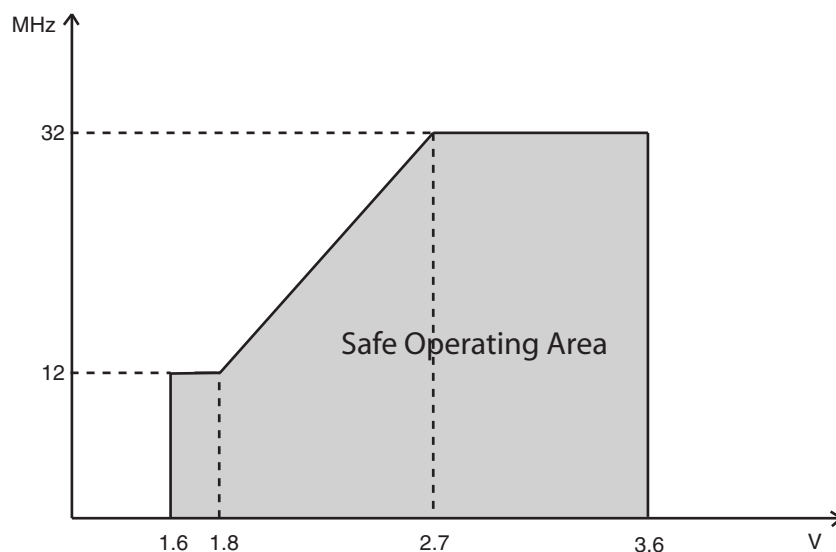
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_J	Junction temperature		-40		105	

Table 32-88. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	$V_{CC} = 1.6V$	0		12	MHz
		$V_{CC} = 1.8V$	0		12	
		$V_{CC} = 2.7V$	0		32	
		$V_{CC} = 3.6V$	0		32	

The maximum CPU clock frequency depends on V_{CC} . As shown in [Figure 32-22](#) the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 32-22. Maximum Frequency vs. V_{CC}



32.4.14 SPI Characteristics

Figure 32-26. SPI Timing Requirements in Master Mode

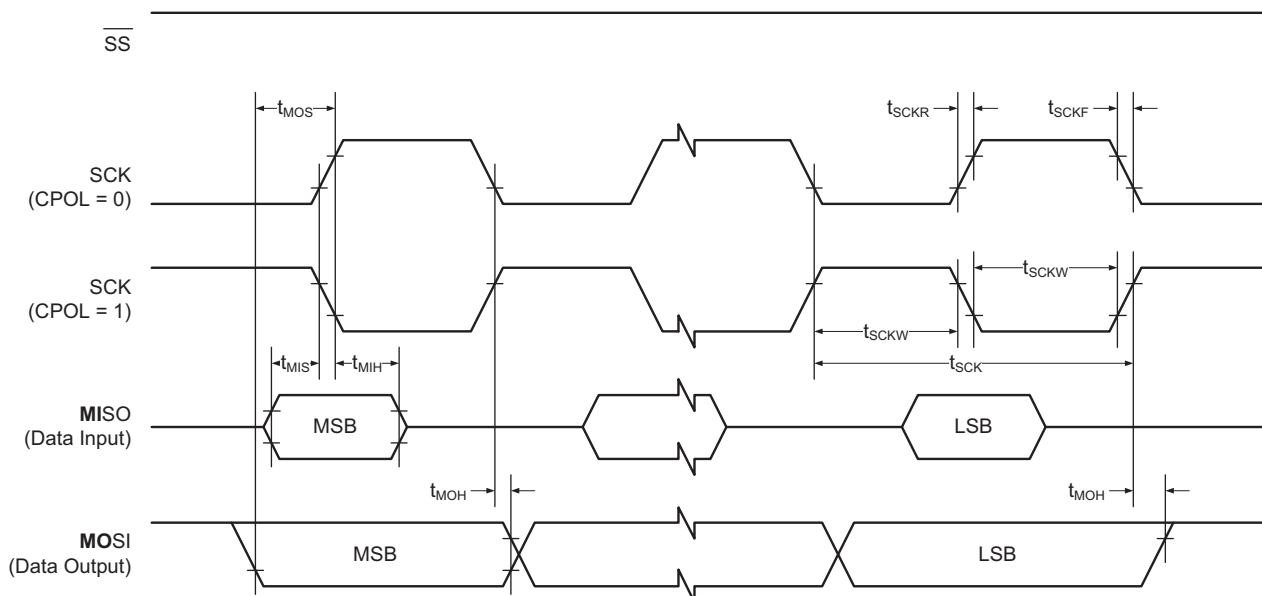


Figure 32-27. SPI Timing Requirements in Slave Mode

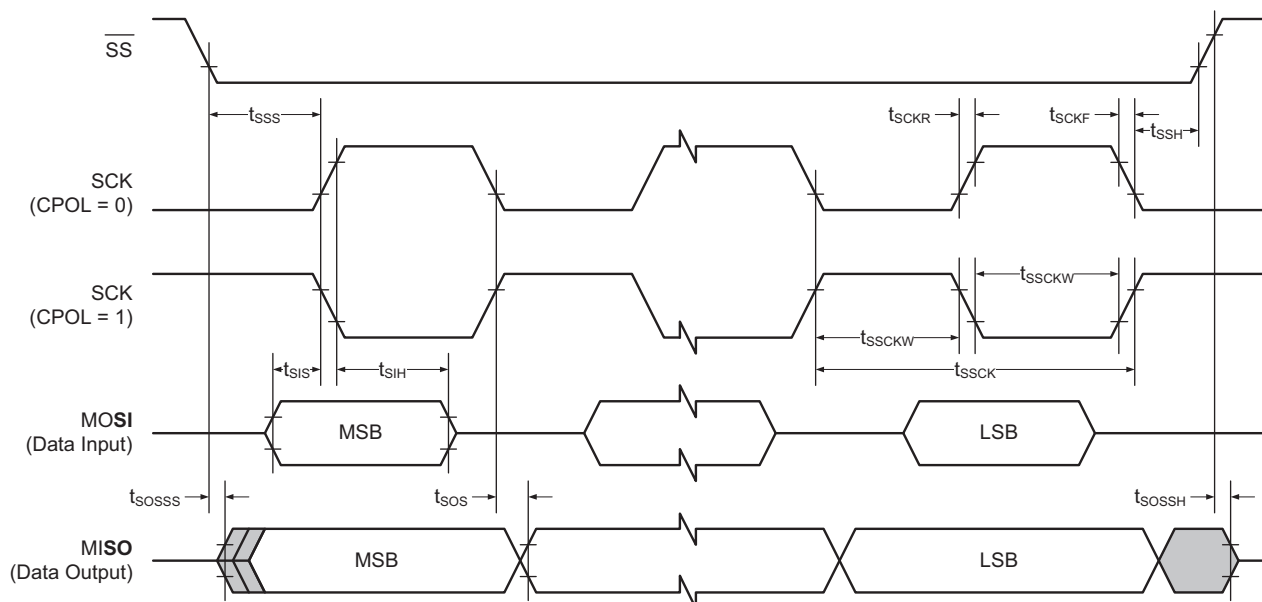


Figure 33-3. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768\text{kHz}$ internal oscillator

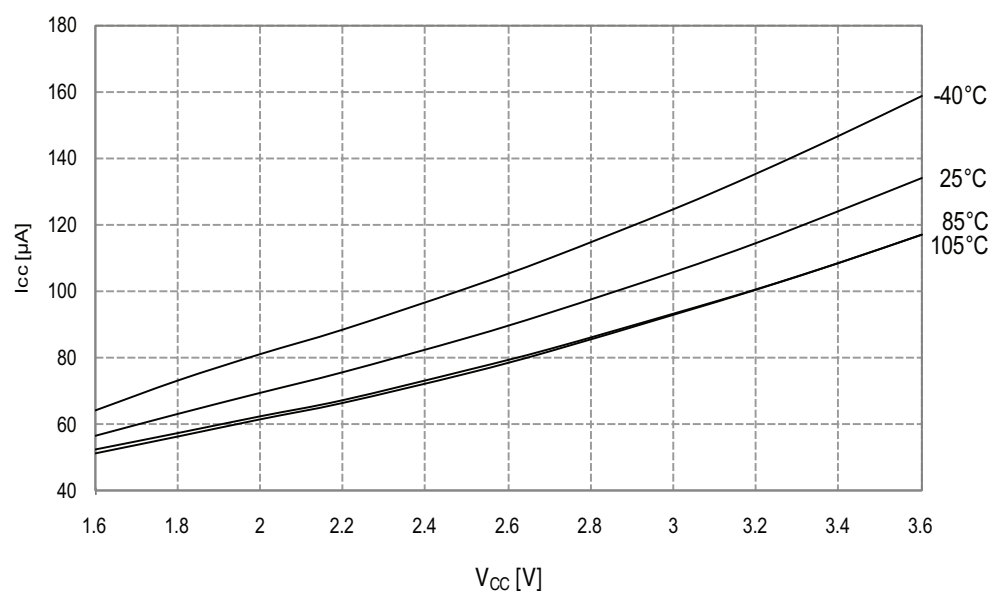


Figure 33-4. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 1\text{MHz}$ external clock.

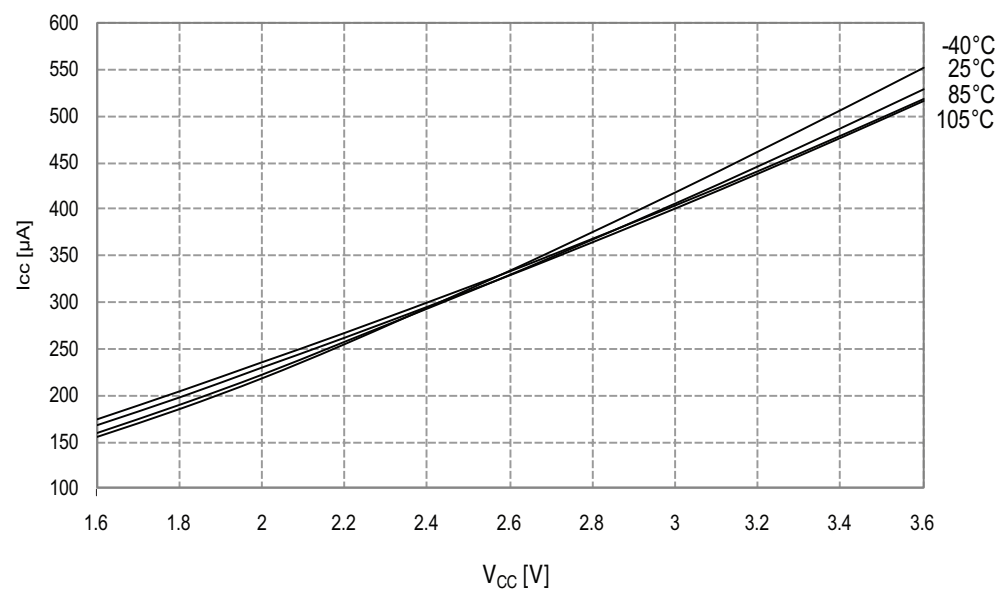


Figure 33-41. DNL Error vs. Input Code

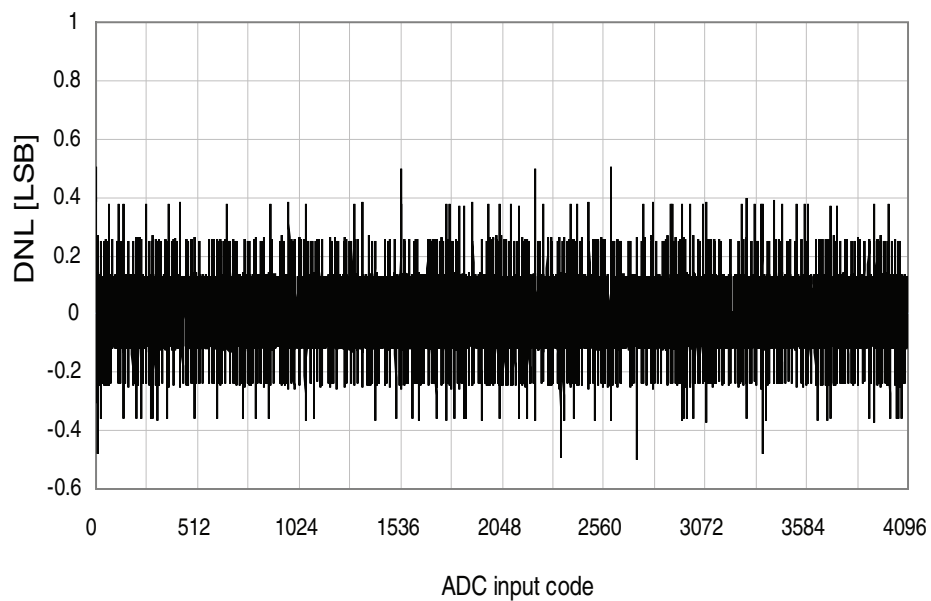


Figure 33-42. Gain Error vs. V_{REF}

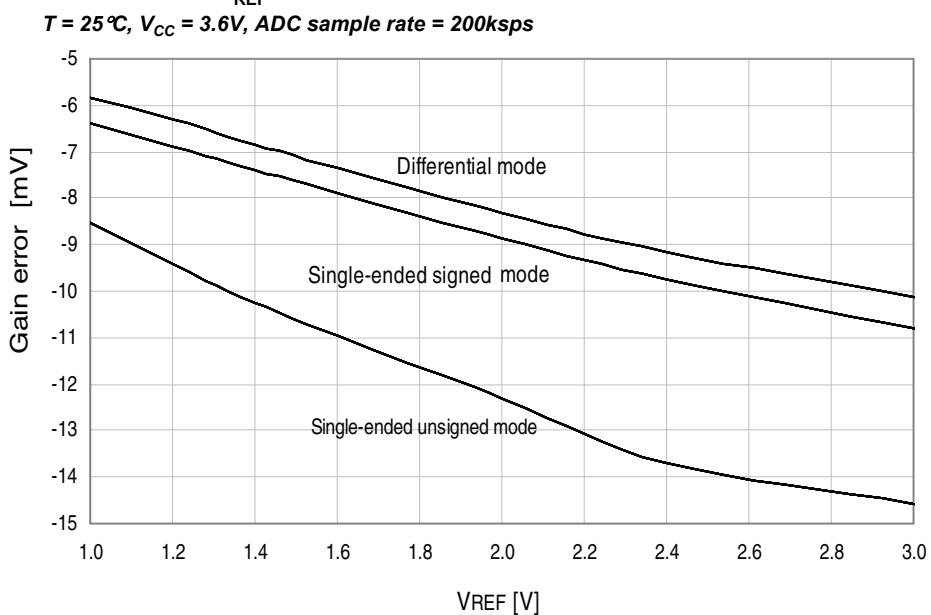


Figure 33-120. DNL Error vs. Input code

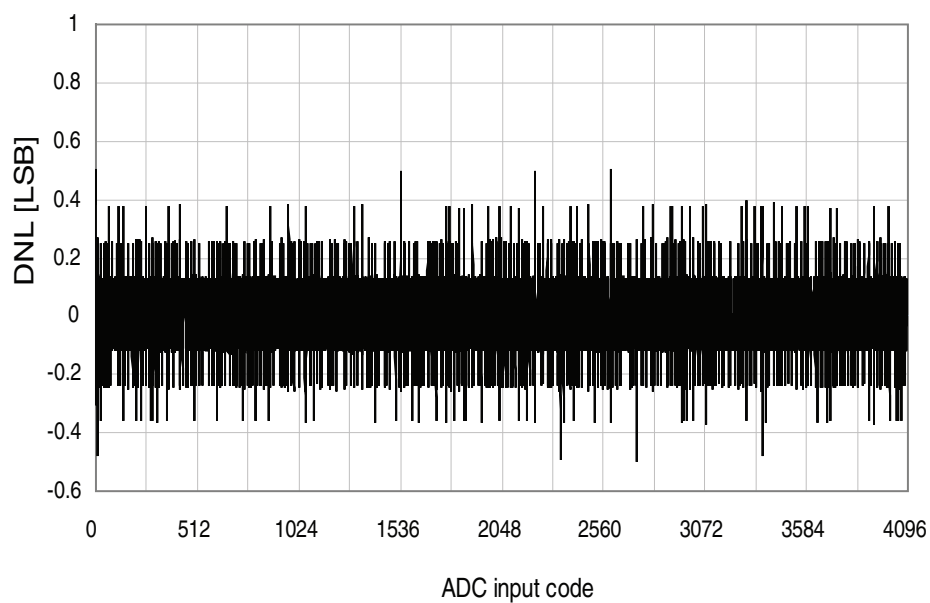
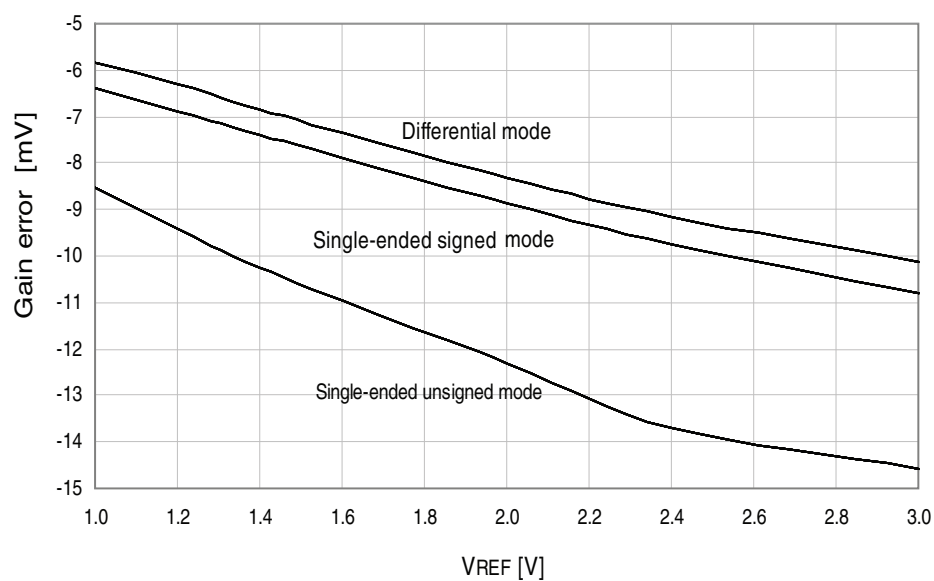


Figure 33-121. Gain Error vs. V_{REF}

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, ADC sample rate = 200ksps



33.2.8 Power-on Reset Characteristics

Figure 33-142. Power-on Reset Current Consumption vs. V_{CC}
BOD level = 3.0V, enabled in continuous mode

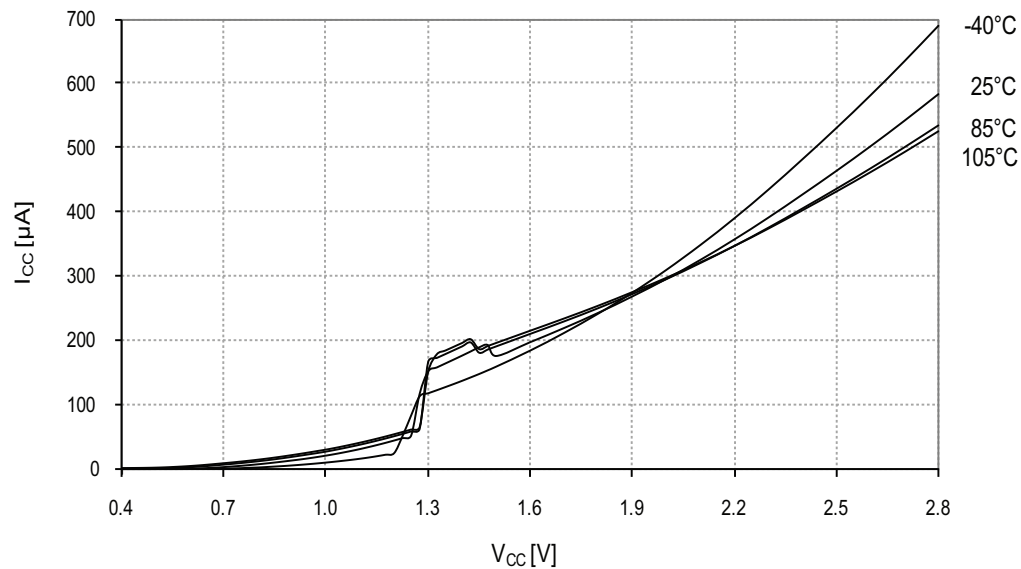


Figure 33-143. Power-on Reset Current Consumption vs. V_{CC}
BOD level = 3.0V, enabled in sampled mode

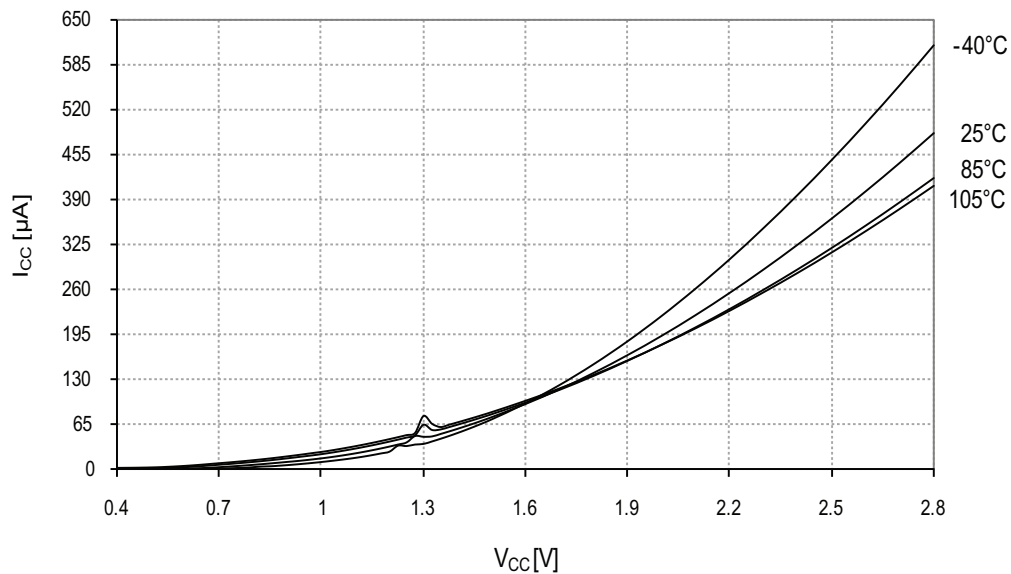


Figure 33-161. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768\text{kHz}$ internal oscillator

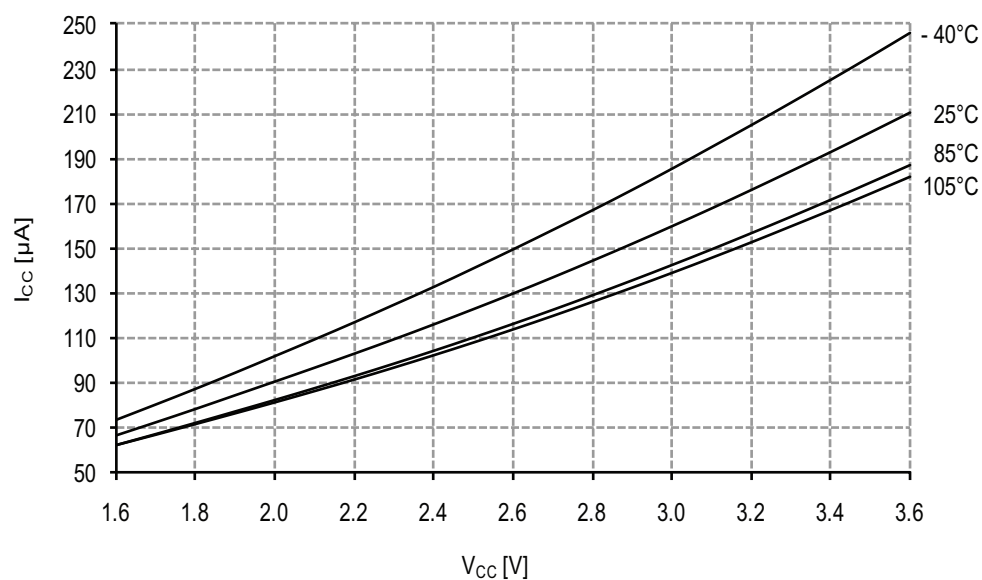


Figure 33-162. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 1\text{MHz}$ external clock

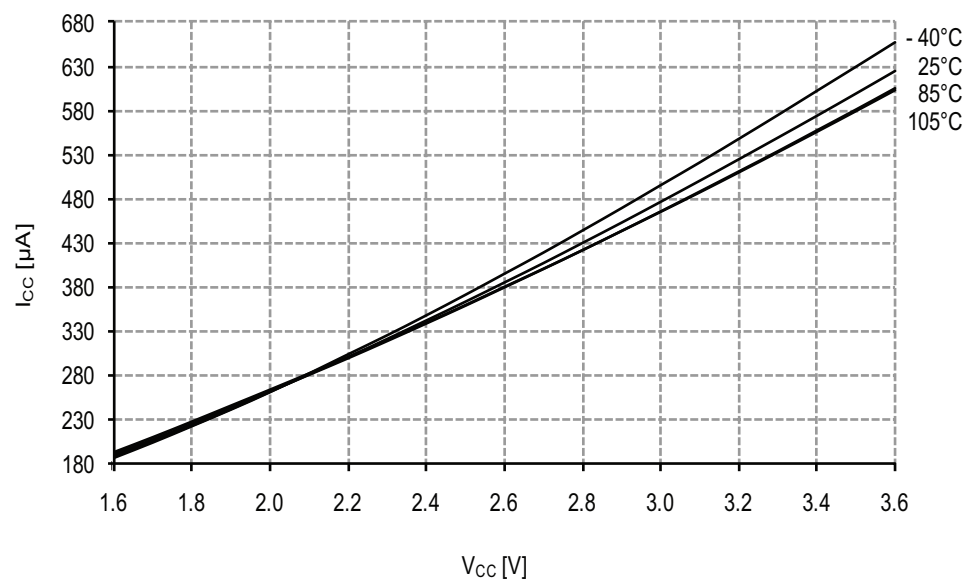


Figure 33-197. DNL Error vs. External V_{REF}
 $T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, external reference

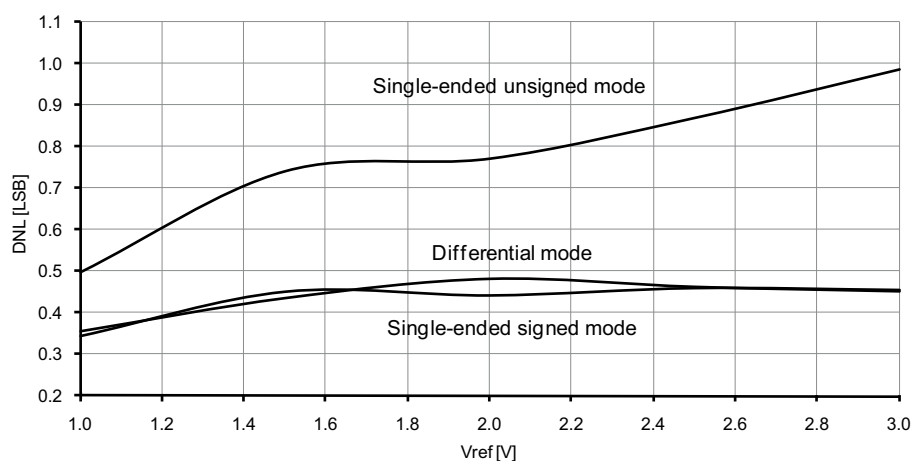


Figure 33-198. DNL Error vs. Sample rate
 $T = 25^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$, $V_{REF} = 1.0\text{V}$ external

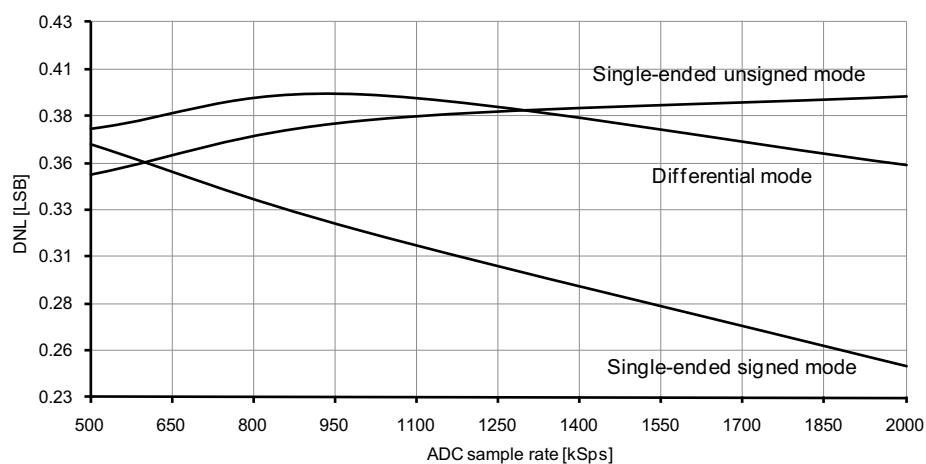


Figure 33-285. Gain Error vs. V_{CC}

$T = 25^{\circ}\text{C}$, $V_{REF} = \text{external } 1.0\text{V}$, ADC sampling speed = 500ksps

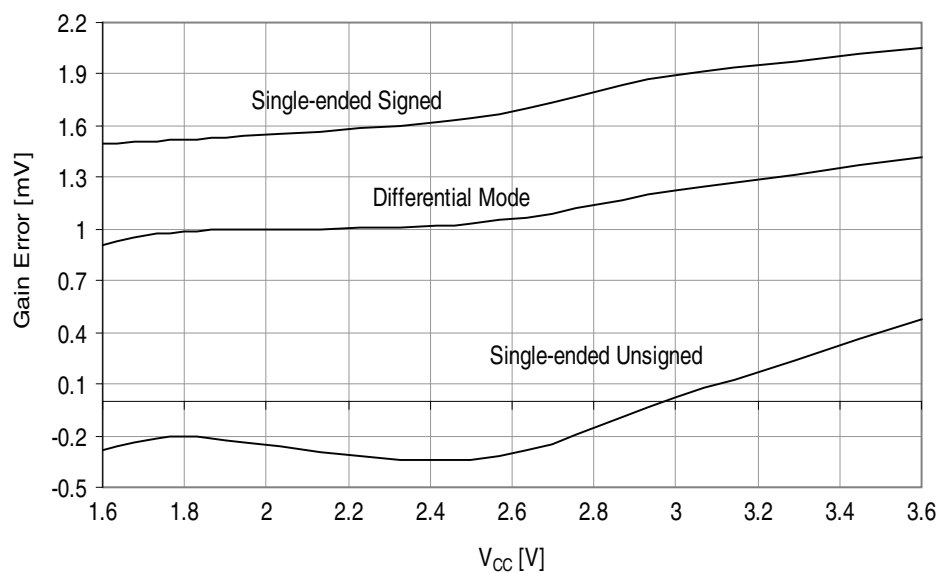


Figure 33-286. Offset Error vs. V_{REF}

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, ADC sampling speed = 500ksps

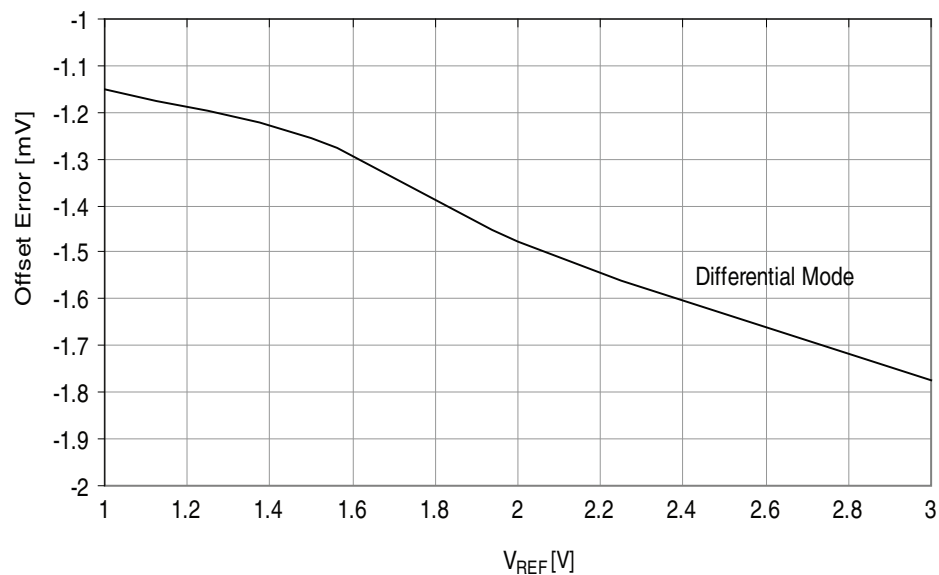
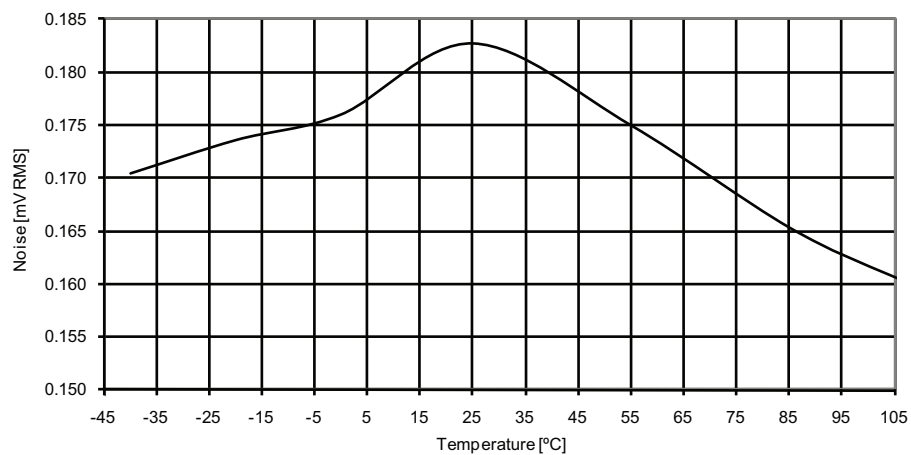


Figure 33-293. DAC Noise vs. Temperature

$V_{CC} = 3.0V$, $V_{REF} = 2.4V$



33.4.5 Analog Comparator Characteristics

Figure 33-294. Analog Comparator Hysteresis vs. V_{CC}

High-speed, small hysteresis

