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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16d4-an

9. System Clock and Clock Options

9.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

9.2 Overview

Atmel AVR XMEGA D4 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 9-1 on page 20 presents the principal clock system in the XMEGA D4 family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in "Power Management and Sleep Modes" on page 22.

12. WDT – Watchdog Timer

12.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

12.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

22. USART

22.1 Features

- Two identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
    - Synchronous clock rates up to 1/2 of the device clock frequency
    - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits
- Fractional baud rate generator
    - Can generate desired baud rate from any system clock frequency
    - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
    - Odd or even parity generation and parity check
    - Data overrun and framing error detection
    - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
    - Transmit complete
    - Transmit data register empty
    - Receive complete
- Multiprocessor communication mode
    - Addressing scheme to address a specific devices on a multidevice bus
    - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
    - Double buffered operation
    - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

22.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

PORTC and PORTD each has one USART. Notation of these peripherals are USARTC0 and USARTD0 respectively.

25. ADC – 12-bit Analog to Digital Converter

25.1 Features

- One Analog to Digital Converters (ADC)
- 12-bit resolution
- Up to 200 thousand samples per second
  - Down to 3.6μs conversion time with 8-bit resolution
  - Down to 5.0μs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 12 single-ended inputs
  - 12x4 differential inputs without gain
  - 12x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Three internal inputs
  - Internal temperature sensor
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional interrupt/event on compare result

25.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to 200 thousand samples per second (ksps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

The ADC measurements can either be started by application software or an incoming event from another peripheral in the device. The ADC measurements can be started with predictable timing, and without software intervention.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The $AV_{CC}/10$ and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

28.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.
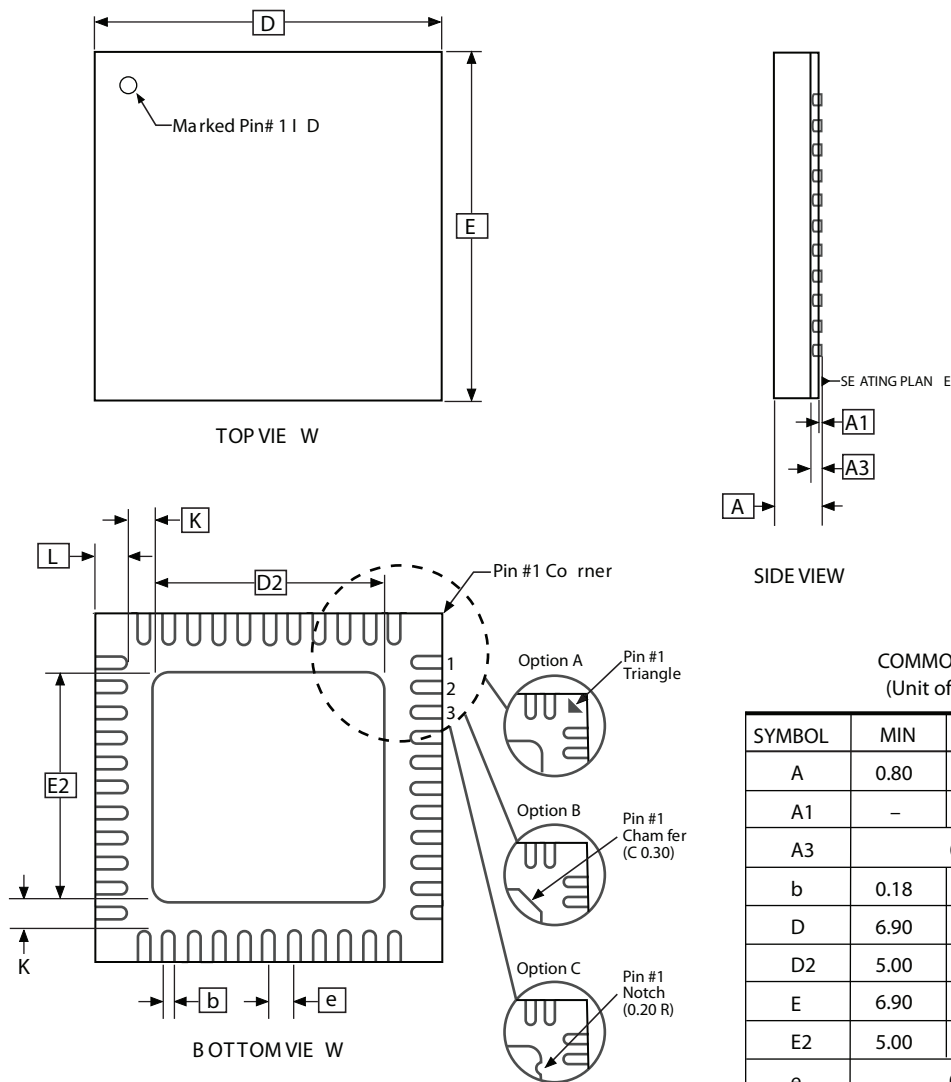
Table 28-1. Port A - Alternate Functions

PORT A	PIN#	INTERRUPT	ADCA POS/GAINPOS	ADCA NEG	ADCA GAINNEG	ACAPOS	ACANEG	ACAOUT	REFA
GND	38								
AVCC	39								
PA0	40	SYNC	ADC0	ADC0		AC0	AC0		AREF
PA1	41	SYNC	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	AC6			
PA7	3	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 28-2. Port B - Alternate Functions

PORT B	PIN#	INTERRUPT	ADCAPOS/GAINPOS	REFB
PB0	4	SYNC	ADC8	AREF
PB1	5	SYNC	ADC9	
PB2	6	SYNC/ASYNC	ADC10	
PB3	7	SYNC	ADC11	

31.2 44M1

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

Pin #1 Corner

Option A — Pin #1 Triangle

Option B — Pin #1 Chamfer (C 0.30)

Option C — Pin #1 Notch (0.20 R)

SEATING PLANE

Marked Pin# 1 ID

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

02/13/2014

Package Drawing Contact:
packagedrawings@atmel.com

TITLE	GPC	DRAWING NO.	REV.
44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	ZWS	44M1	H

32.1.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-7. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH}[1]/ I_{OL}[2]	I/O pin source/sink current			-20		20	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4- 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.7		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes: 1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.2.3 Current Consumption

Table 32-32. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		200		
			V_{CC} = 3.0V		410		
		2MHz, Ext. Clk	V_{CC} = 1.8V		350	600	
			V_{CC} = 3.0V		0.75	1.4	mA
		32MHz, Ext. Clk			7.5	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.0		µA
			V_{CC} = 3.0V		2.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		42		
			V_{CC} = 3.0V		85		
		2MHz, Ext. Clk	V_{CC} = 1.8V		85	225	
			V_{CC} = 3.0V		170	350	
		32MHz, Ext. Clk			2.7	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			2.0	4.5	
		T = 105°C			0.1	7.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.4	10	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.5		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

32.2.14 SPI Characteristics

Figure 32-12.SPI Timing Requirements in Master Mode
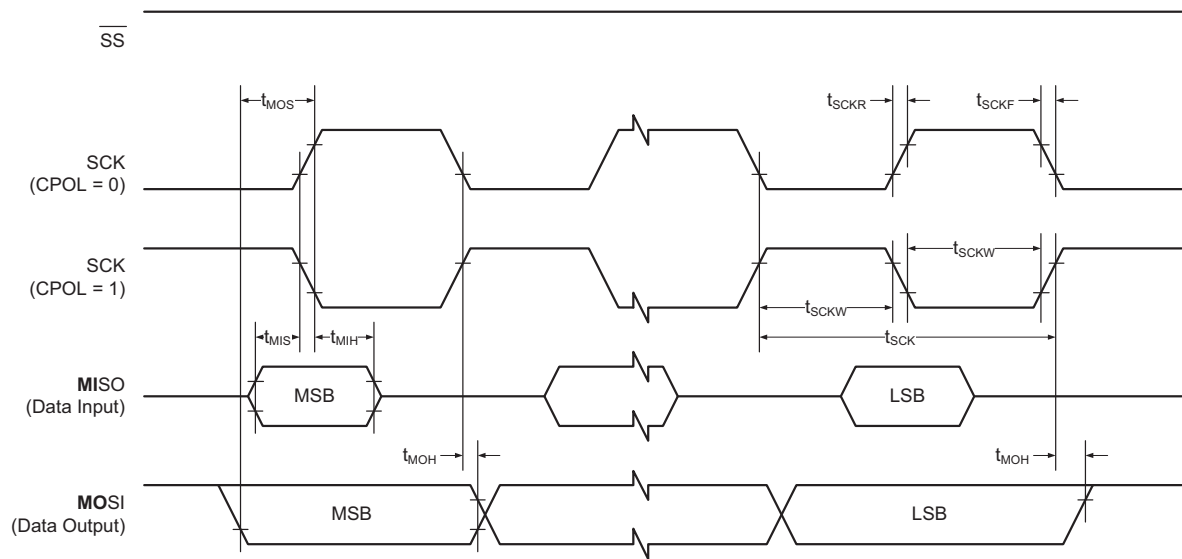
Figure 32-13.SPI Timing Requirements in Slave Mode
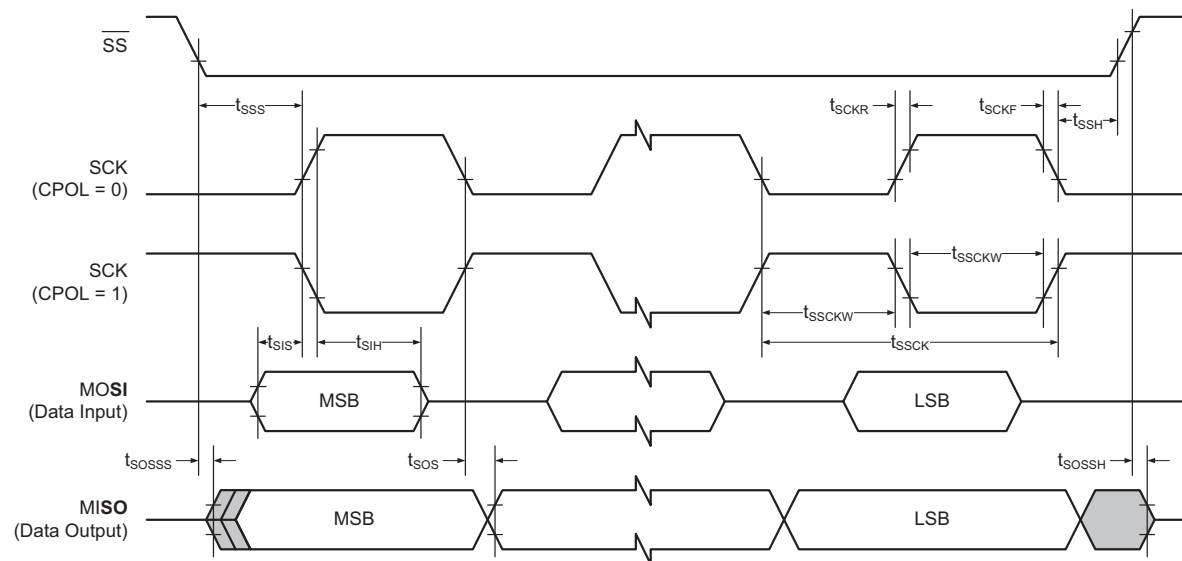
Figure 33-23. I/O pin pull-up Resistor Current vs. Input Voltage
$V_{CC} = 3.3V$
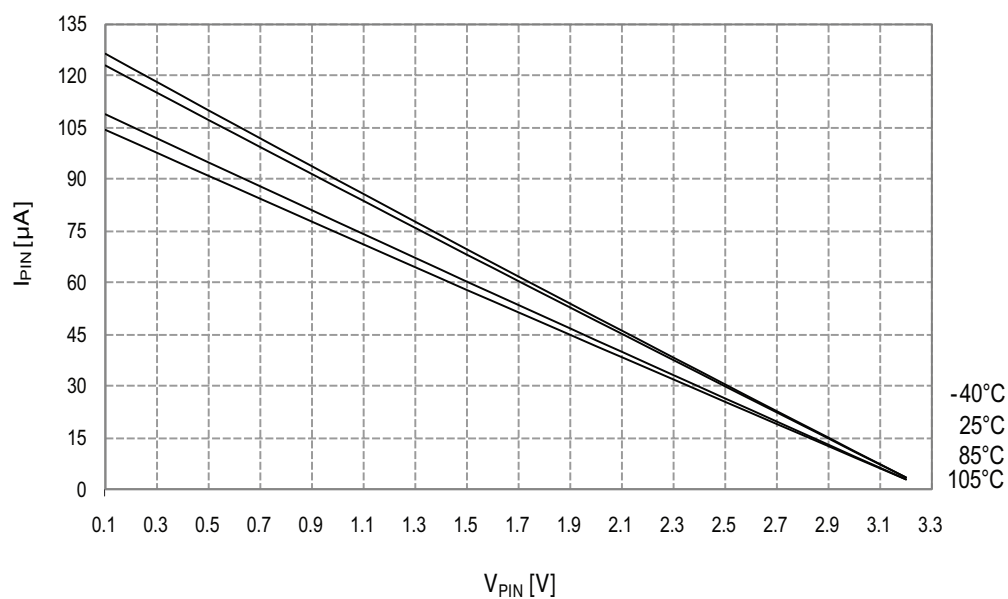
33.1.2.2 Output Voltage vs. Sink/Source Current

Figure 33-24. I/O Pin Output Voltage vs. Source Current
$V_{CC} = 1.8V$
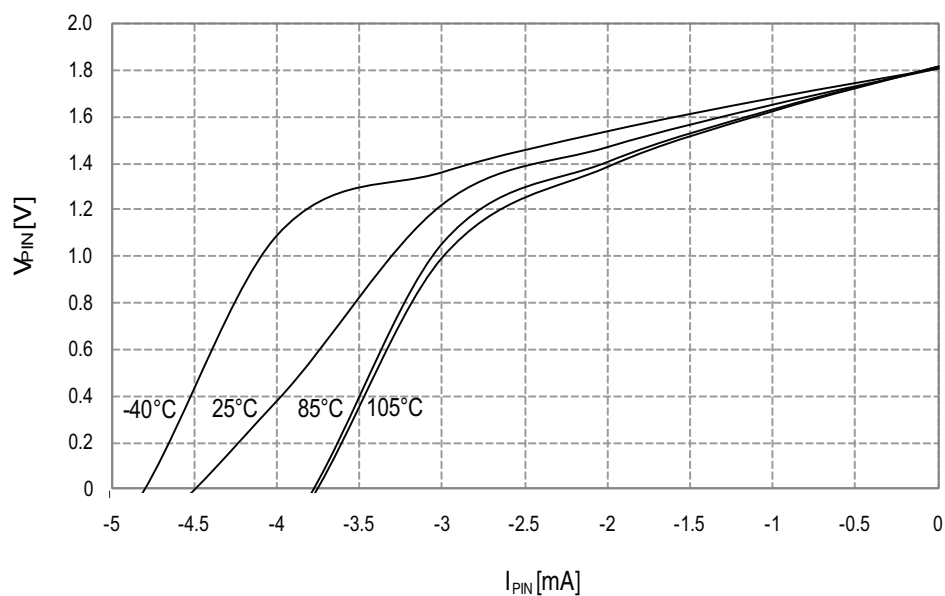
Figure 33-59. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage
$V_{CC} = 3.0V$
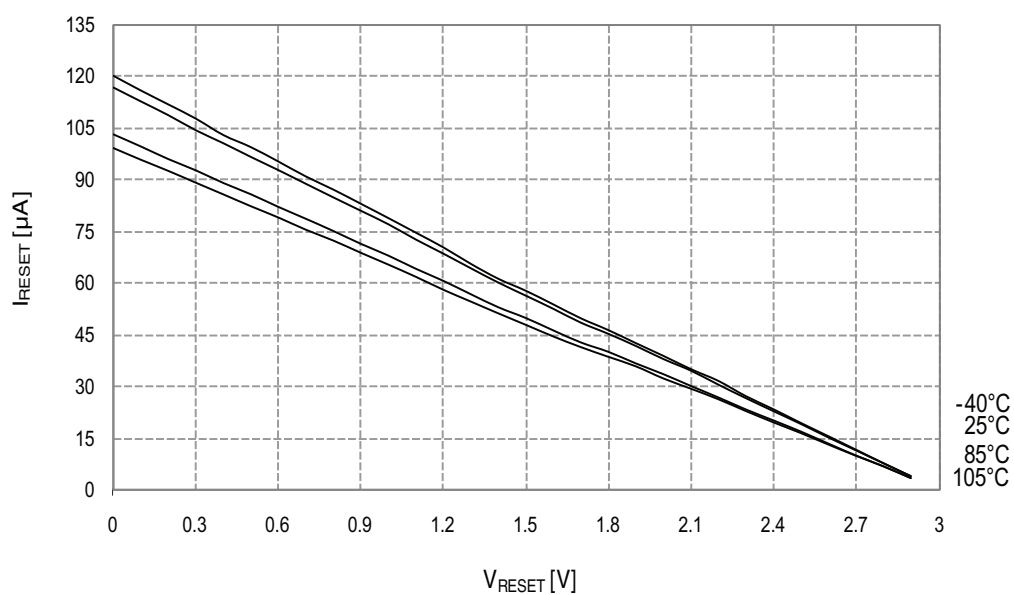
Figure 33-60. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage
$V_{CC} = 3.3V$
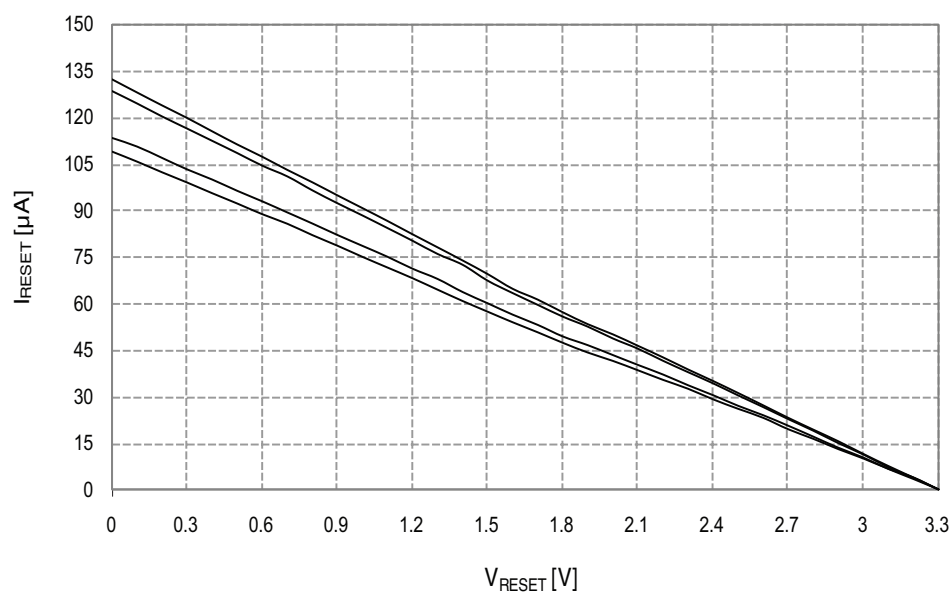
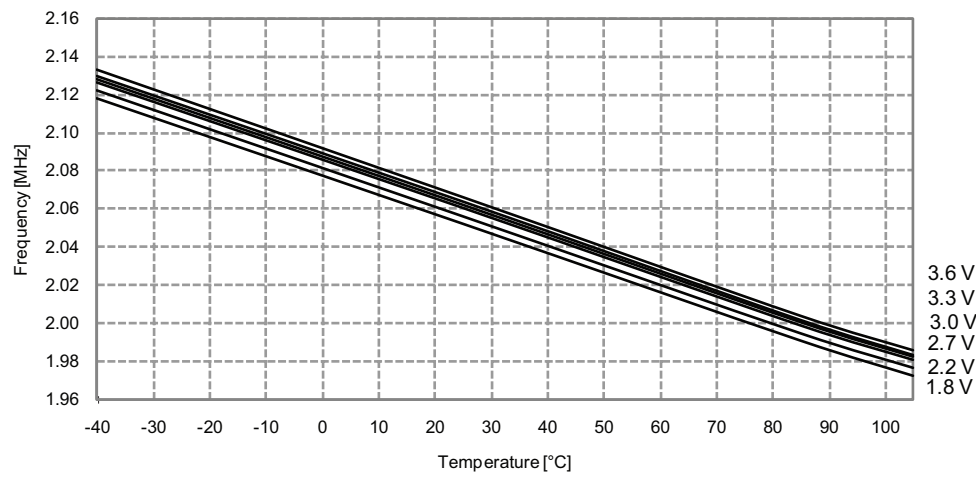**Figure 33-154. 48MHz Internal Oscillator Frequency vs. Temperature**
    DFLL enabled, from the 32.768kHz internal oscillator
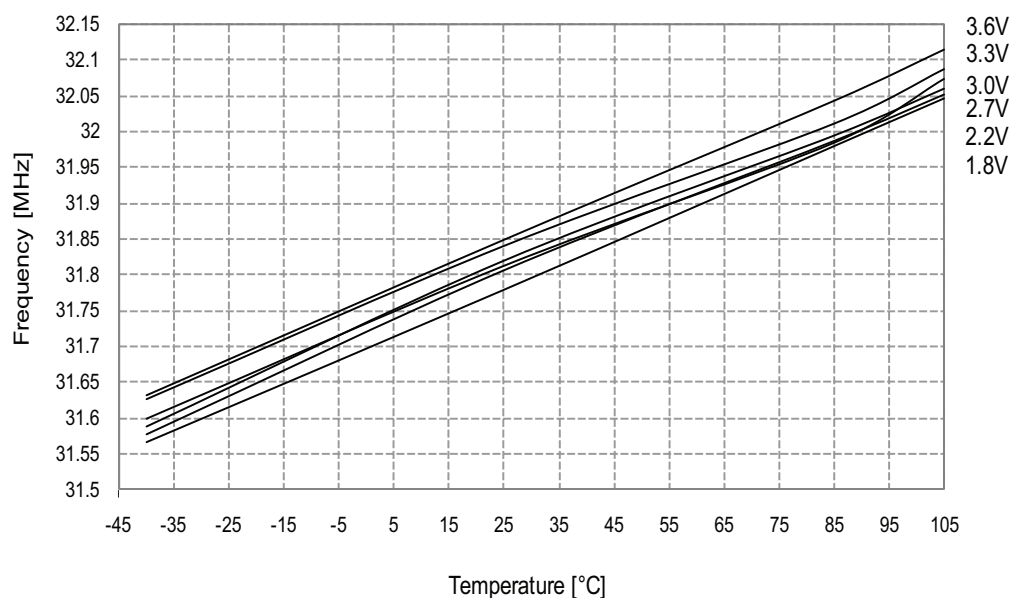
Figure 33-155. 48MHz Internal Oscillator CALA Calibration Step Size
    V_CC = 3.0V
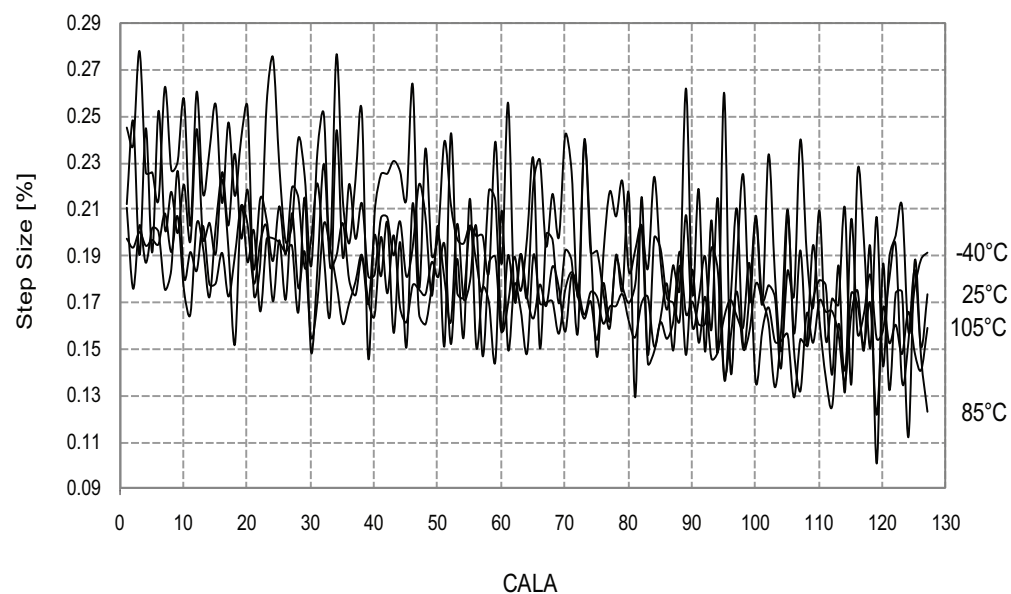
Figure 33-211. Analog Comparator Hysteresis vs. V$_{CC}$
Low power, small hysteresis
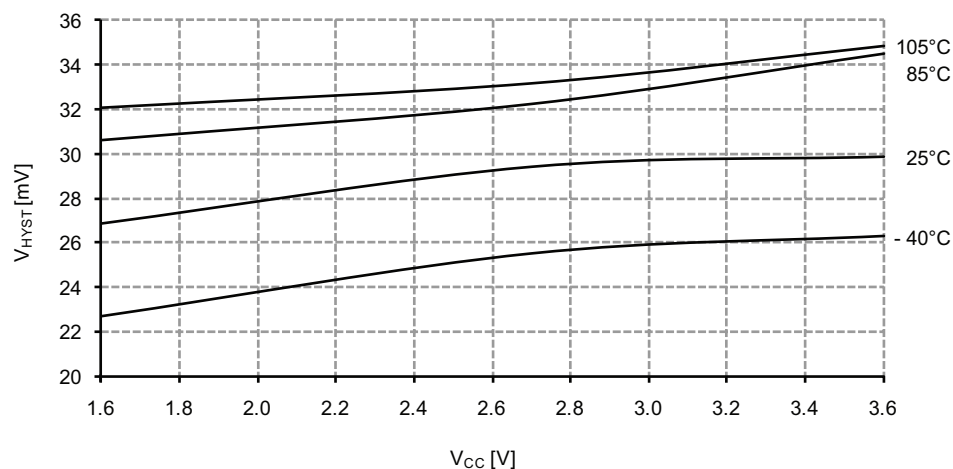
Figure 33-212. Analog Comparator Hysteresis vs. V$_{CC}$
High-speed mode, large hysteresis
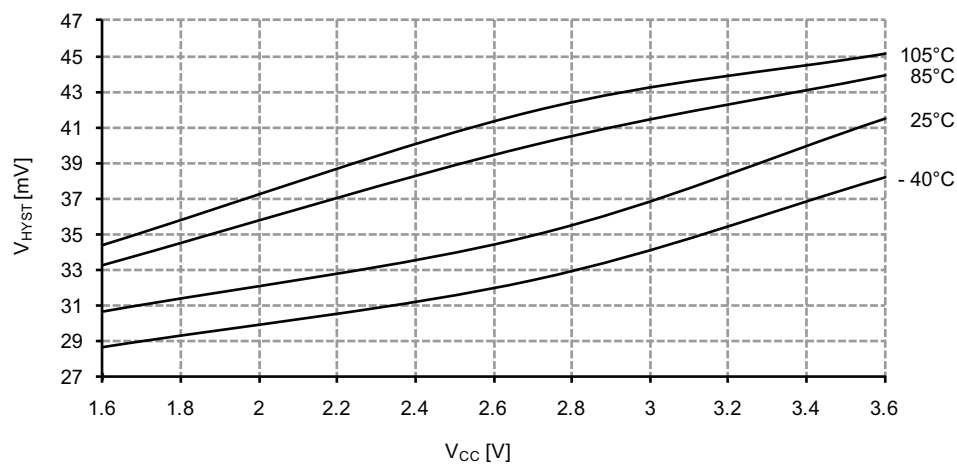
Figure 33-271. I/O Pin Output Voltage vs. Sink Current
V_{CC} = 3.0V
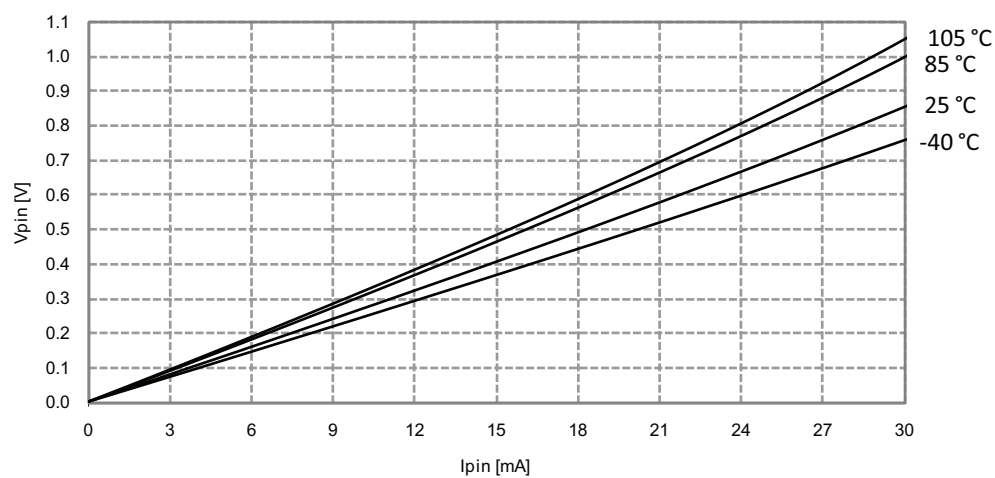
Figure 33-272. I/O Pin Output Voltage vs. Sink Current
V_{CC} = 3.3V
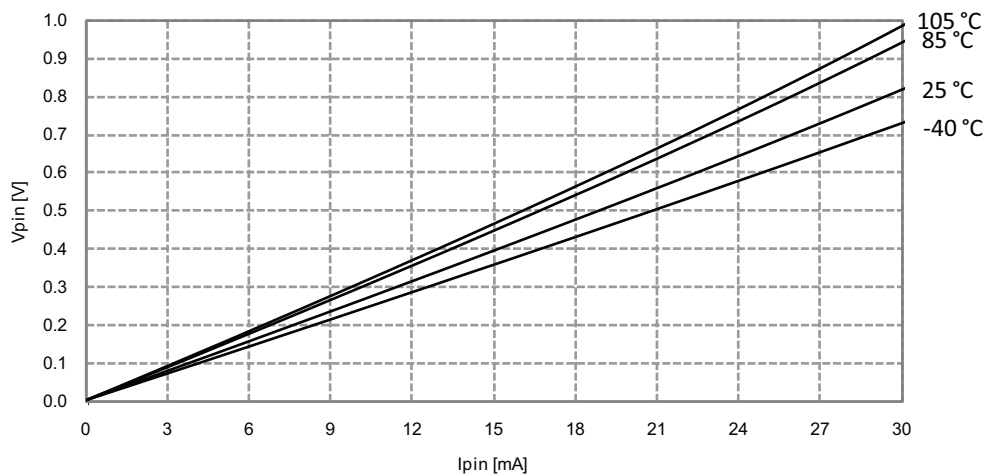
Figure 33-285. Gain Error vs. V$_{CC}$

T = 25°C, V$_{REF}$ = external 1.0V, ADC sampling speed = 500ksps
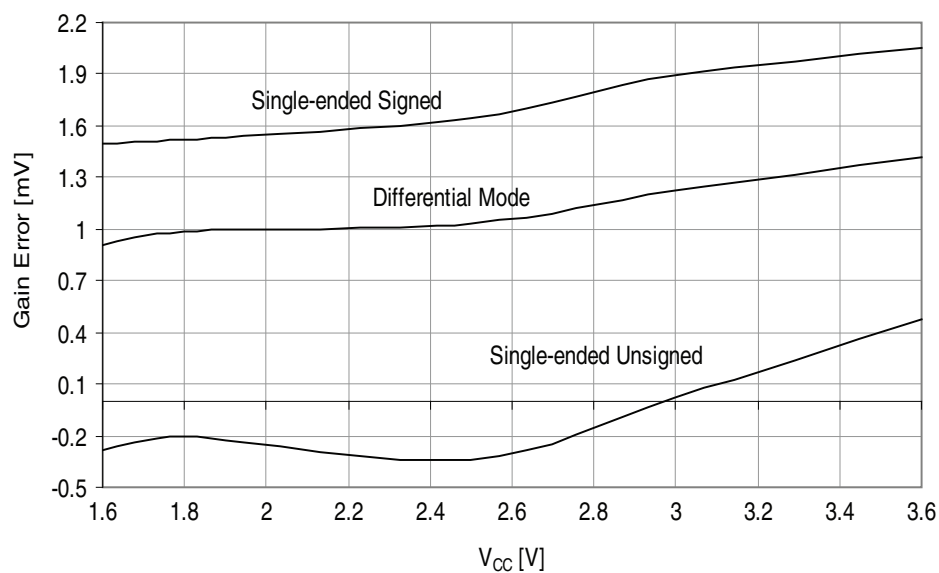
Figure 33-286. Offset Error vs. V$_{REF}$

T = 25°C, V$_{CC}$ = 3.6V, ADC sampling speed = 500ksps
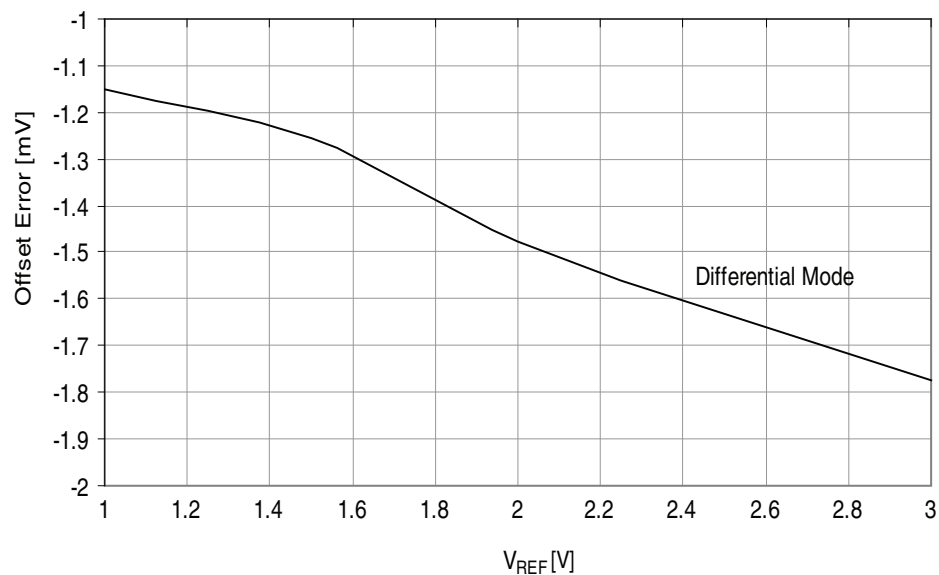
33.4.10.2 32.768kHz Internal Oscillator

Figure 33-313. 32.768kHz Internal Oscillator Frequency vs. Temperature
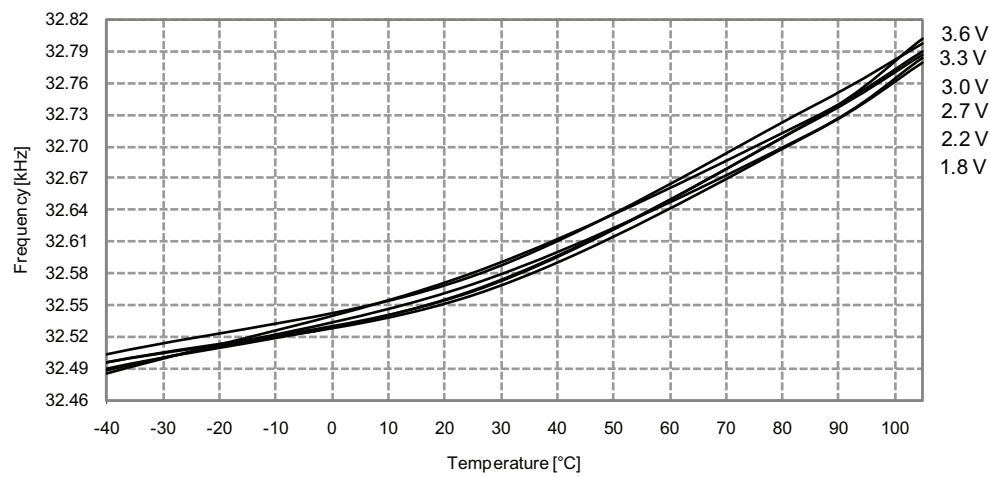
Figure 33-314. 32.768kHz Internal Oscillator Frequency vs. Calibration Value
   V_{CC} = 3.0V, T = 25°C
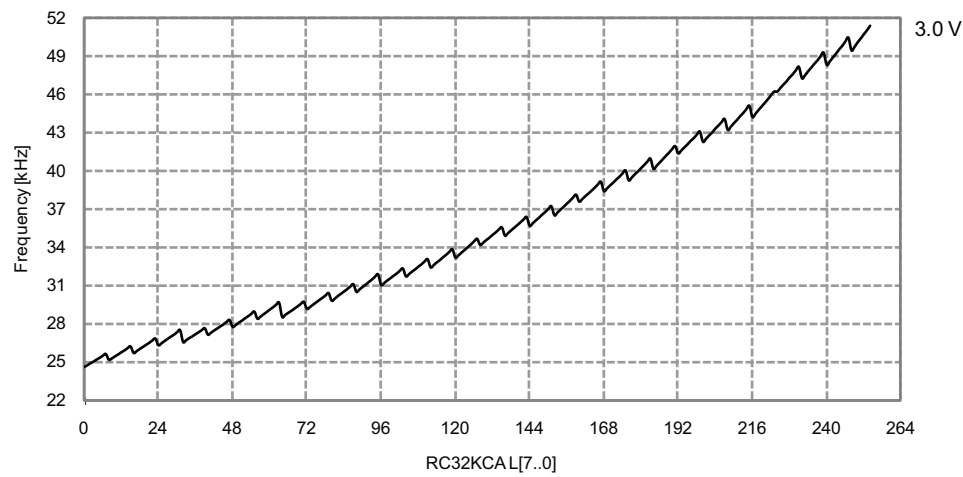
33.4.10.3 2MHz Internal Oscillator

Figure 33-315. 2MHz Internal Oscillator Frequency vs. Temperature
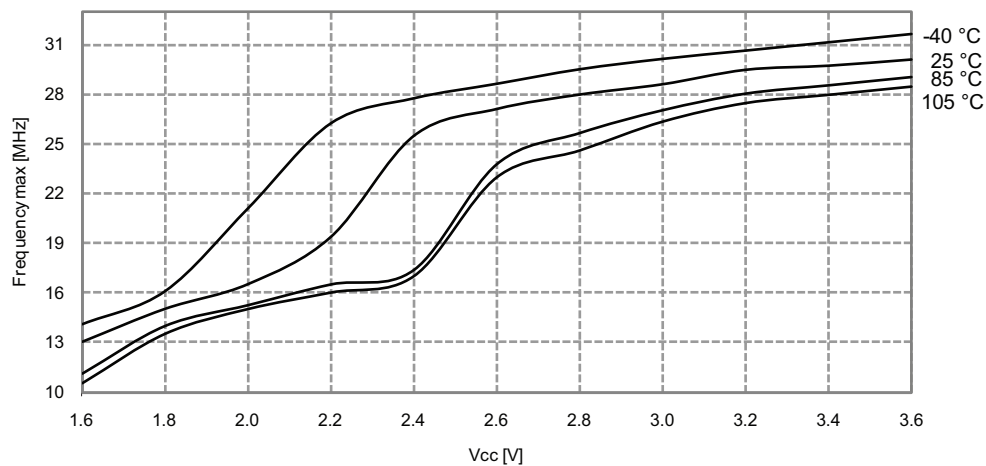   *DFLL disabled*

Figure 33-316. 2MHz Internal Oscillator Frequency vs. Temperature
       DFLL enabled, from the 32.768kHz internal oscillator
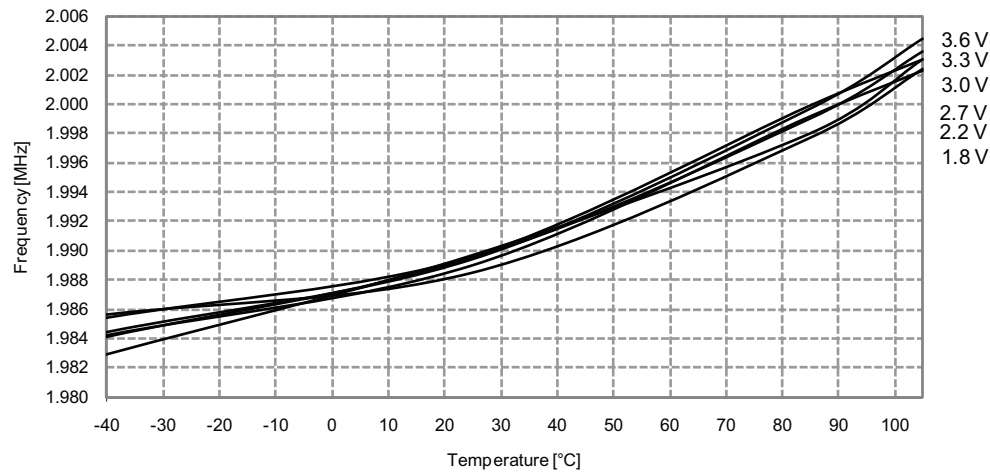
33.4.12 PDI Characteristics

Figure 33-325. Maximum PDI Frequency vs. V_{CC}

1x gain:	2.4V
2x gain:	1.2V
4x gain:	0.6v
8x gain:	300mV
16x gain:	150mV
32x gain:	75mV
64x gain:	38mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

5. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. ADC propagation delay is not correct when 8x -64x gain is used

The propagation delay will increase by only one ADC clock cycle for 8x and 16x gain setting, and 32x and 64x gain settings.

Problem fix/Workaround

None.

7. Bandgap measurement with the ADC is non-functional when VCC is below 2.7V

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

8. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

9. Configuration of PGM and CWCM not as described in XMEGA A Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.