Microchip Technology - ATXMEGA16D4-ANR Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16d4-anr

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (Hexadecimal Address)

Word address							
ATxmega128D4		**ATxmega64D4**		**ATxmega32D4**		**ATxmega16D4**	
0		0		0		0	Application section (128K/64K/32K/16K)
							...
EFFF	/	77FF	/	37FF	/	17FF	
F000	/	7800	/	3800	/	1800	Application table section (8K/4K/4K/4K)
FFFF	/	7FFF	/	3FFF	/	1FFF	
10000	/	8000	/	4000	/	2000	Boot section (8K/4K/4K/4K)
10FFF	/	87FF	/	47FF	/	27FF	

7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

20. TWI – Two-Wire Interface

20.1 Features

- Two identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
  - Phillips I^2C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

20.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I^2C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

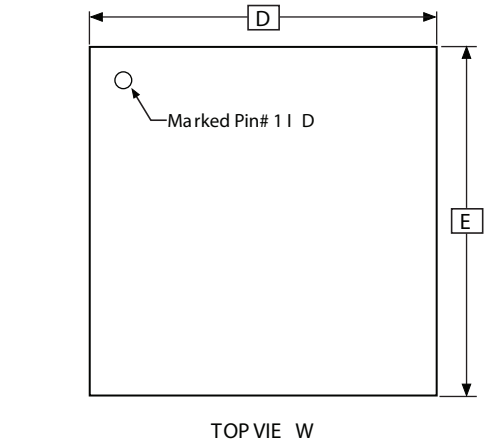
The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

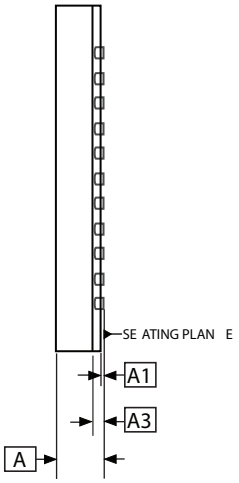
The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

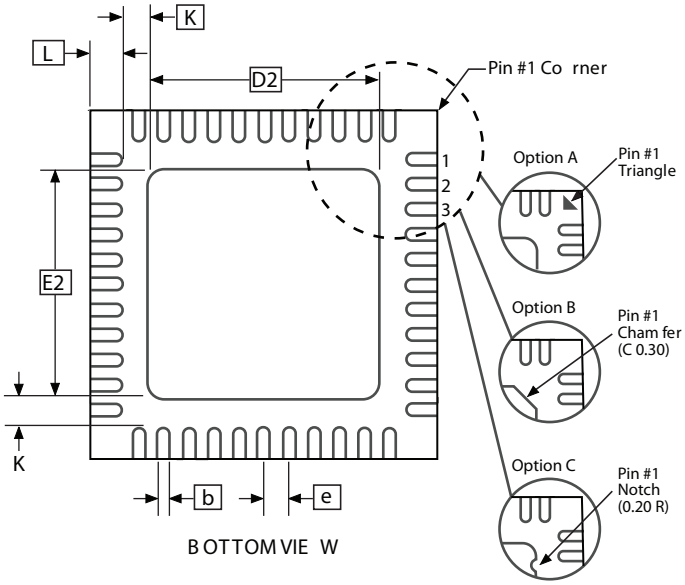
It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V_{CC} voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

31.2 44M1







Note: JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

02/13/2014

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	GPC ZWS	DRAWING NO. 44M1	REV. H

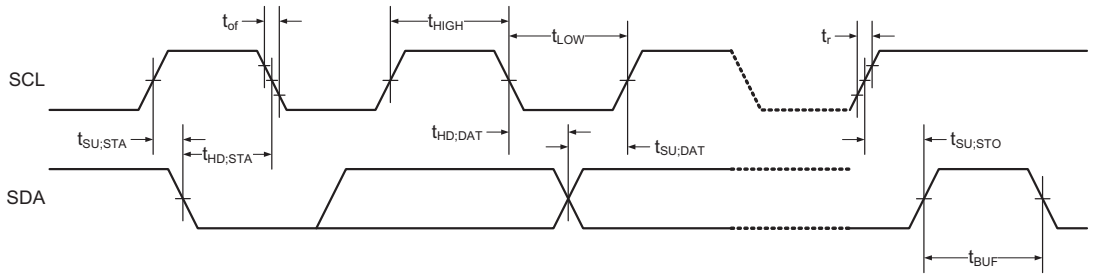
Table 32-27. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA C Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.1.15 Two-Wire Interface Characteristics

Table 32-28 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-21.

Figure 32-7. Two-wire Interface Bus Timing



32.3.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-69. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

32.3.9 Brownout Detection Characteristics

Table 32-70. Brownout Detection Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = safety factor				$min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

Table 32-113. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 17-4 in XMEGA D Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8.0		
t_{SOH}	MISO hold after SCK	Slave		13.0		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11.0		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8.0		

Figure 33-9. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

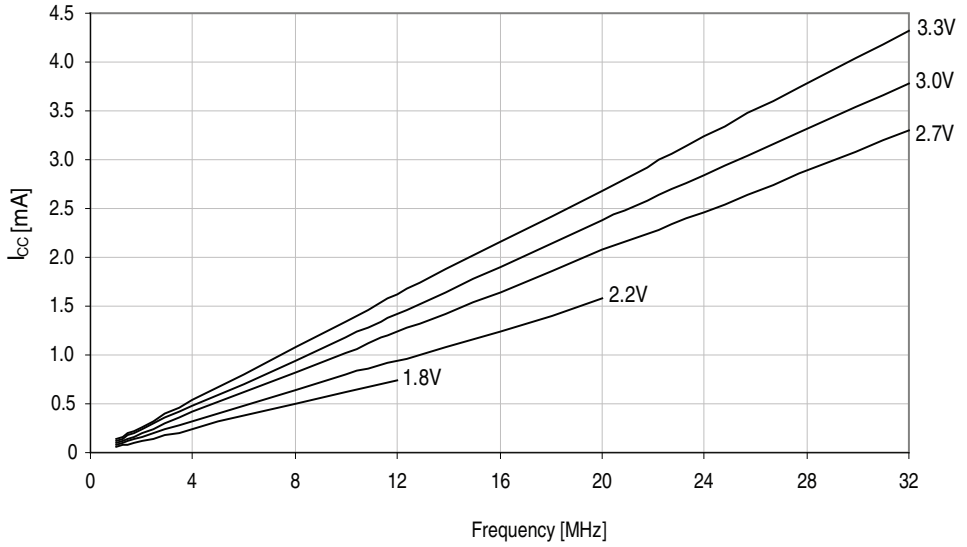


Figure 33-10. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

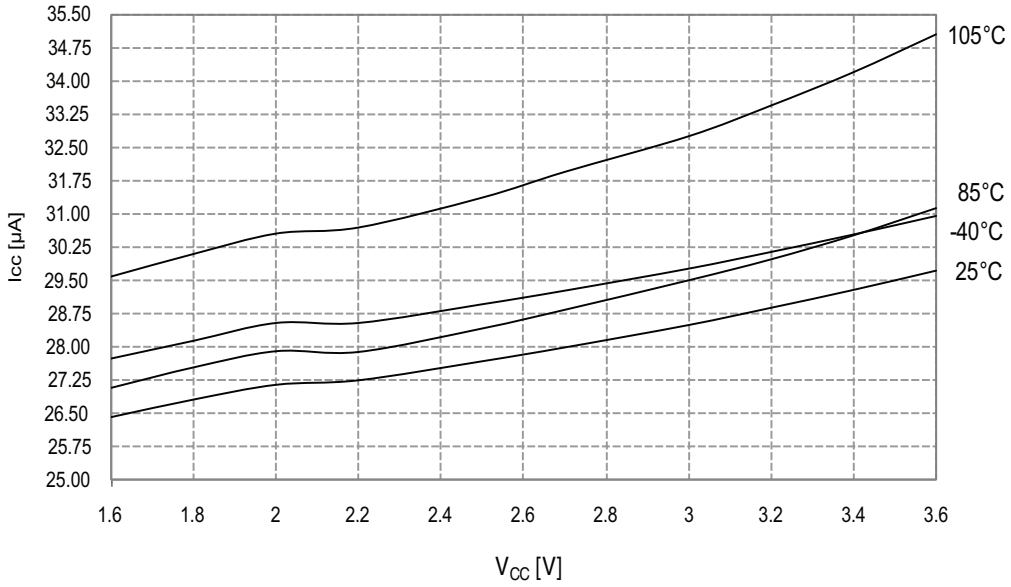
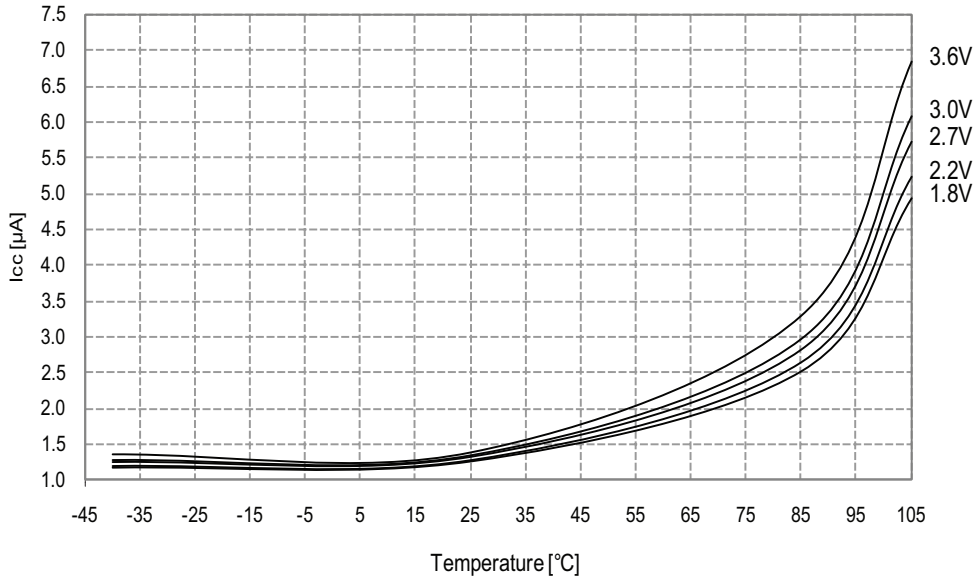


Figure 33-17. Power-down Mode Supply Current vs. Temperature

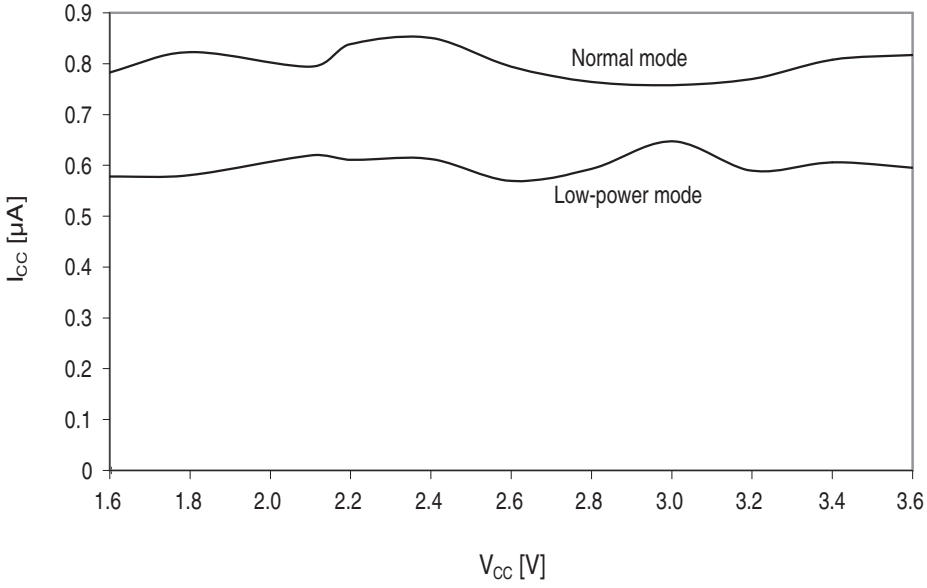
Watchdog and sampled BOD enabled and running from internal ULP oscillator



33.1.1.4 Power-save Mode Supply Current

Figure 33-18. Power-save Mode Supply Current vs.V_{CC}

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC



33.1.1.5 Standby Mode Supply Current

Figure 33-19. Standby Supply Current vs. V_{CC}

Standby, f_{SYS} = 1MHz

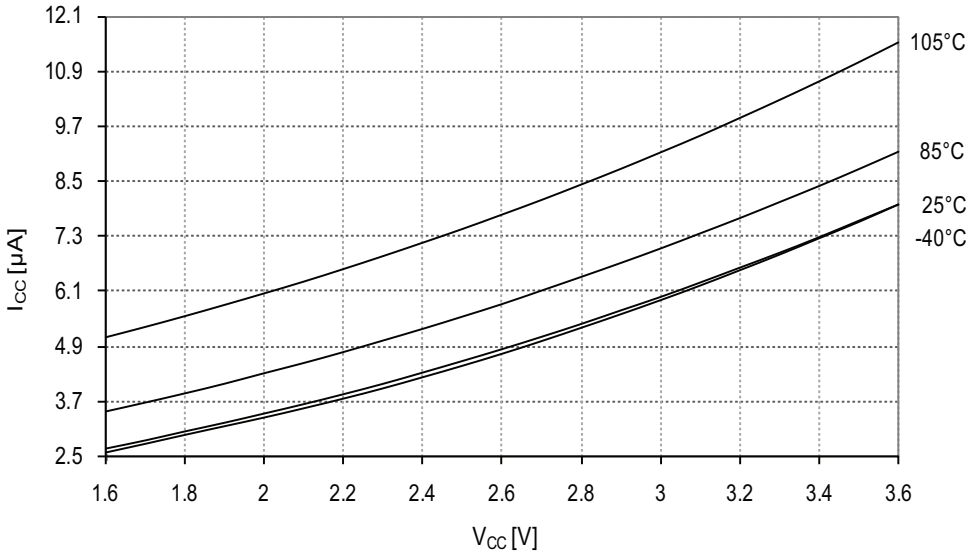


Figure 33-20. Standby Supply Current vs. V_{CC}

25°C, running from different crystal oscillators

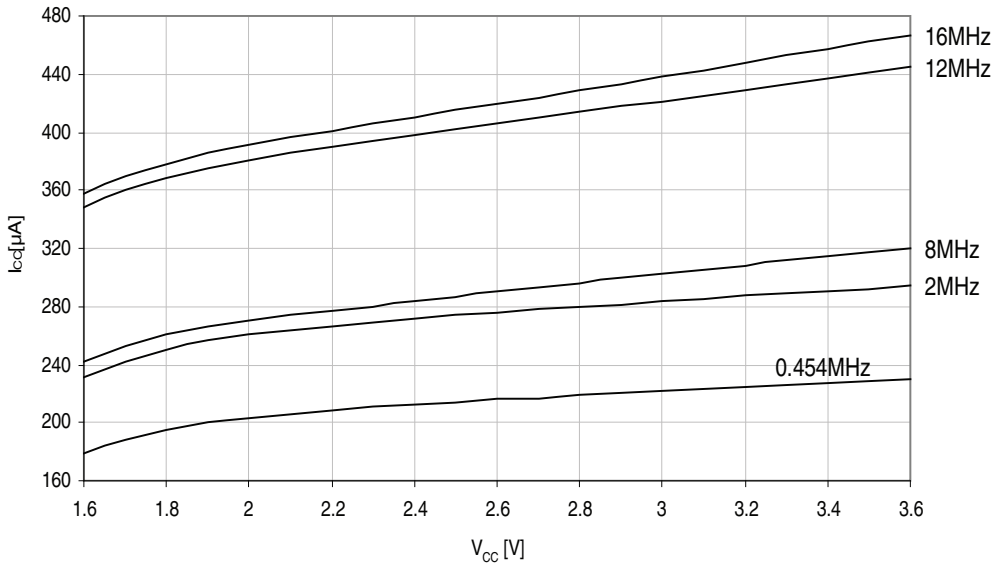


Figure 33-25. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

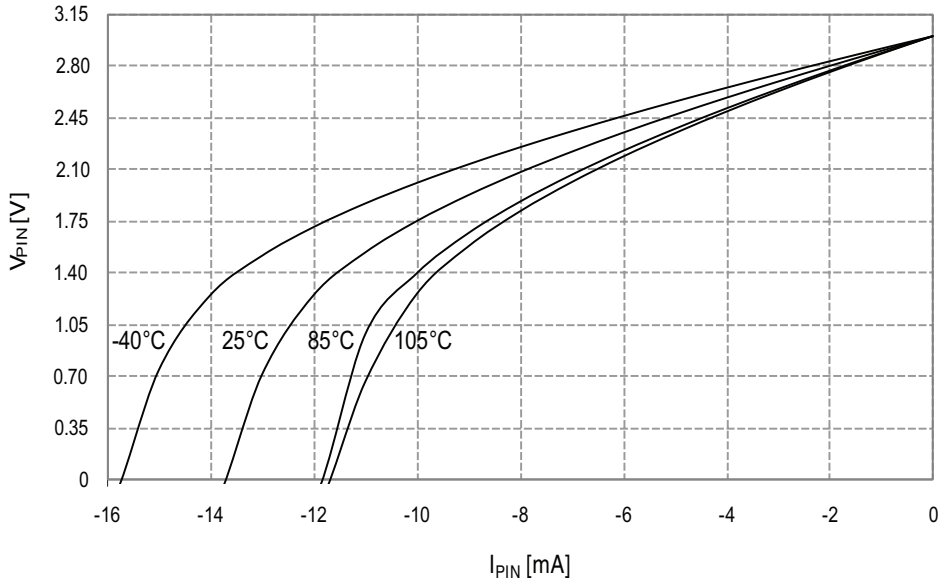


Figure 33-26. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

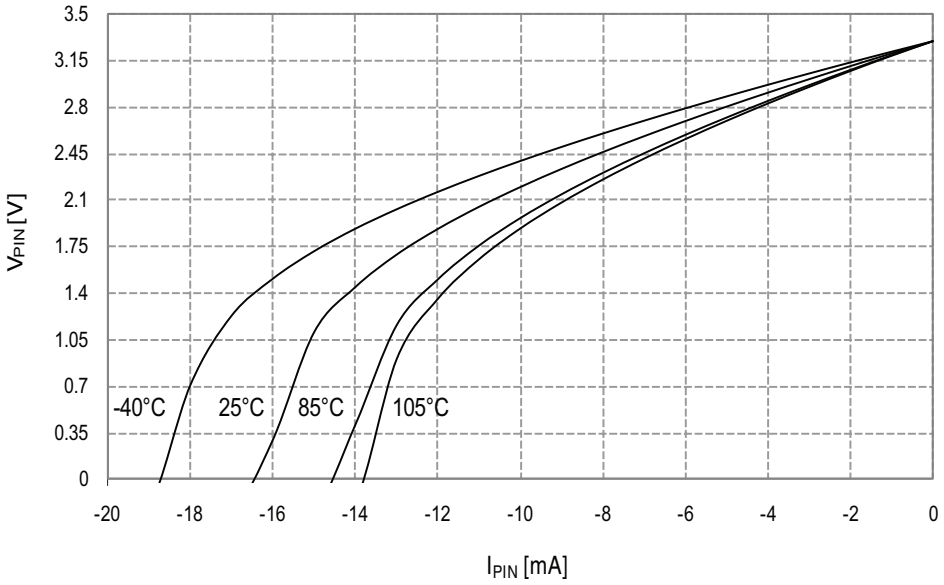
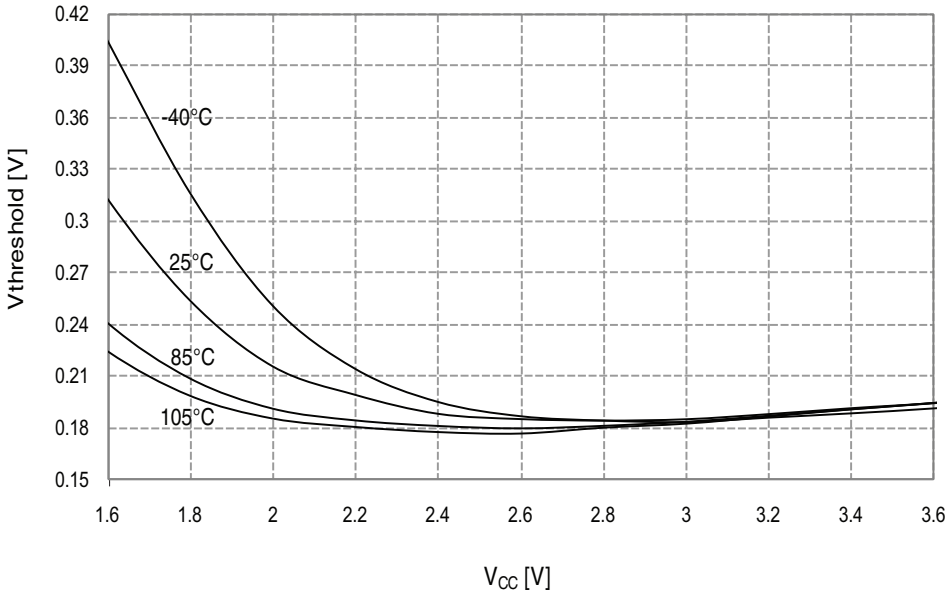


Figure 33-35. I/O Pin Input Hysteresis vs. V_{CC}



33.1.3 ADC Characteristics

Figure 33-36. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

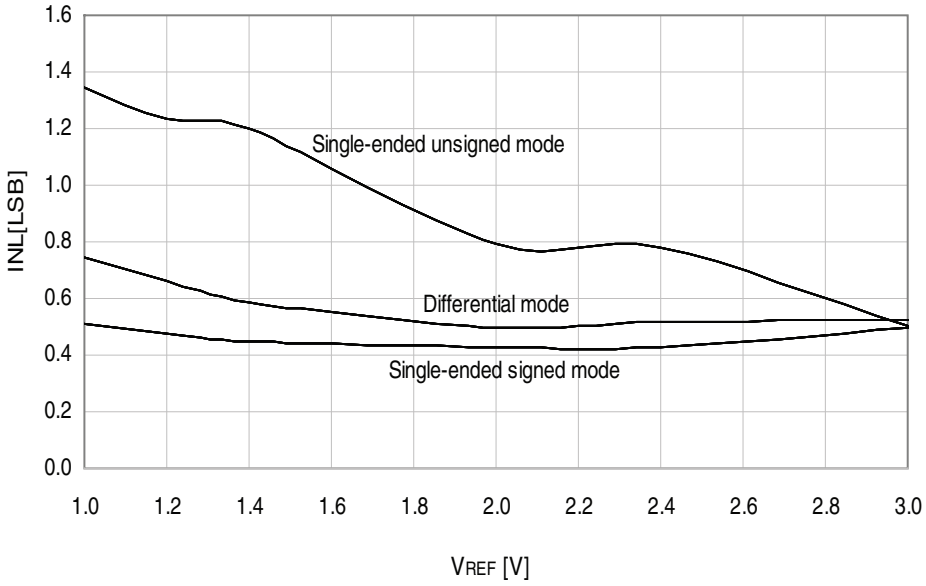


Figure 33-41. DNL Error vs. Input Code

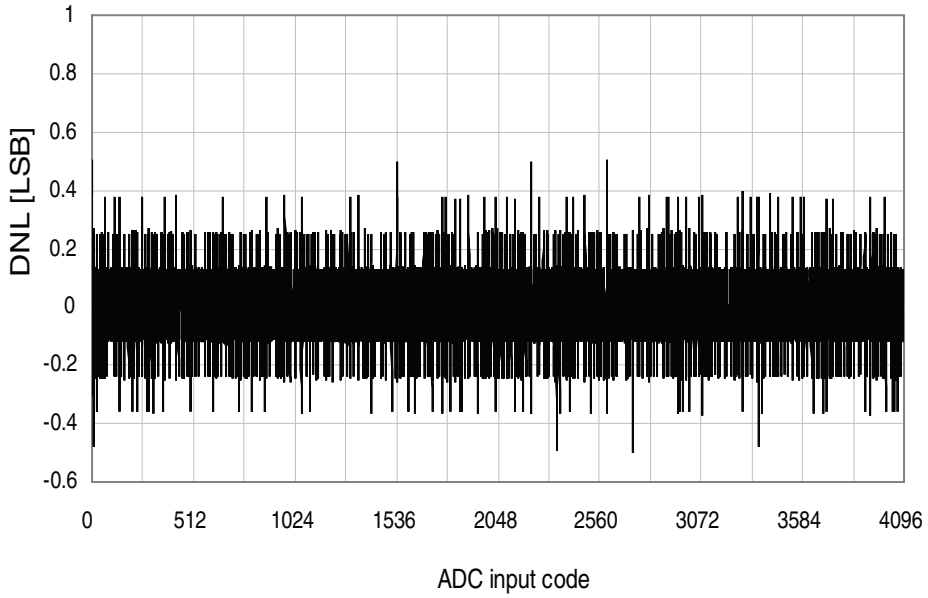


Figure 33-42. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps

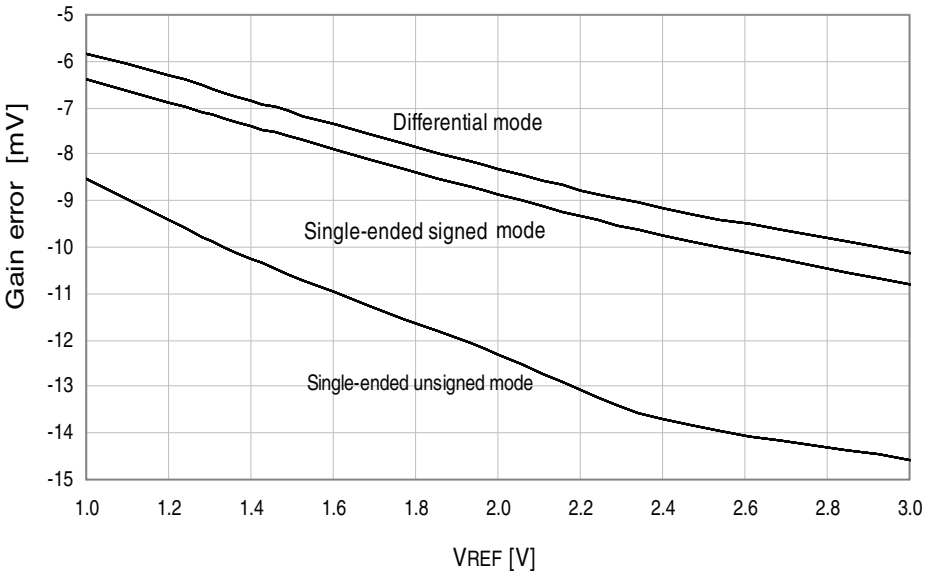
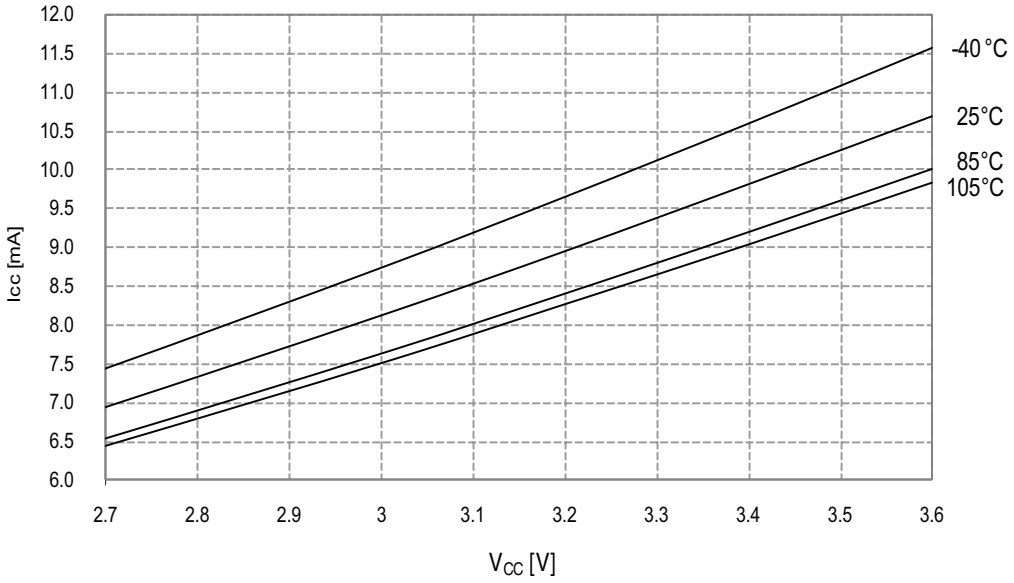


Figure 33-86. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.2.1.2 Idle Mode Supply Current

Figure 33-87. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

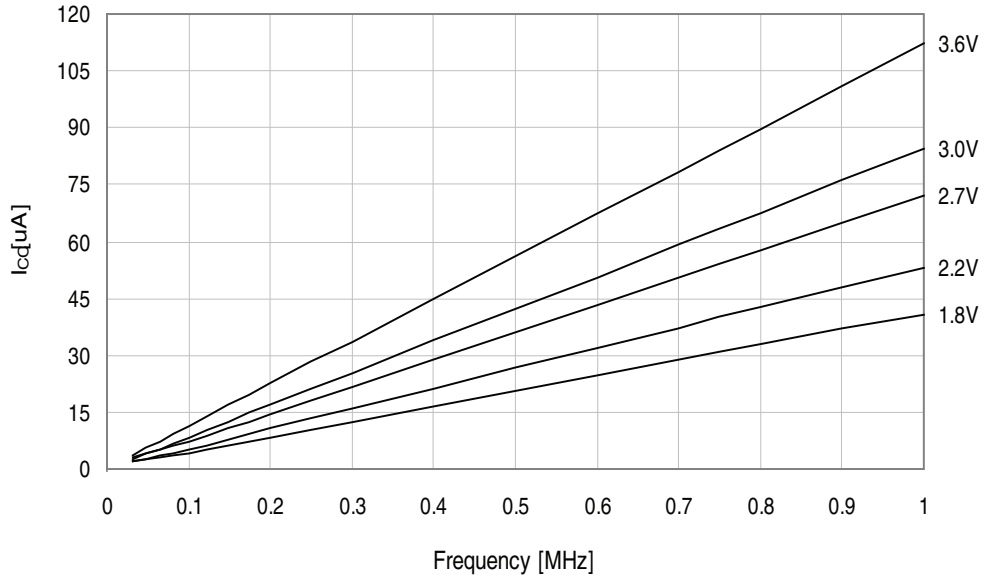


Figure 33-169. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

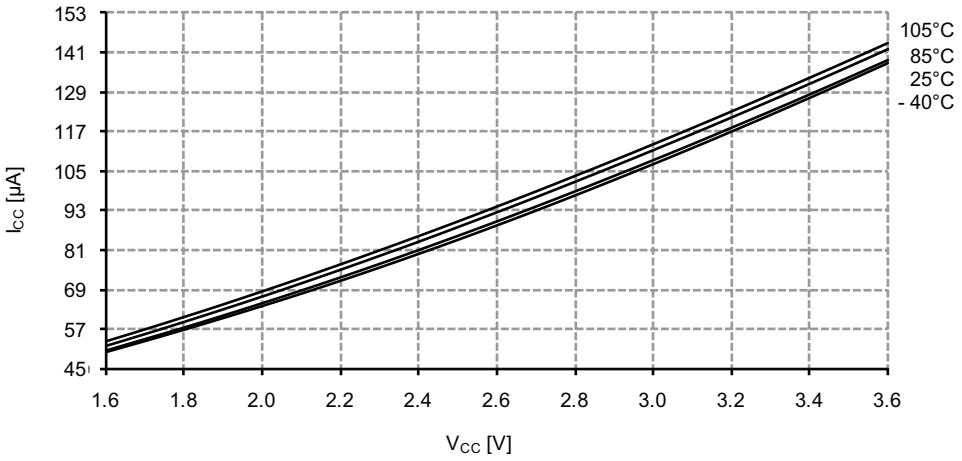


Figure 33-170. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

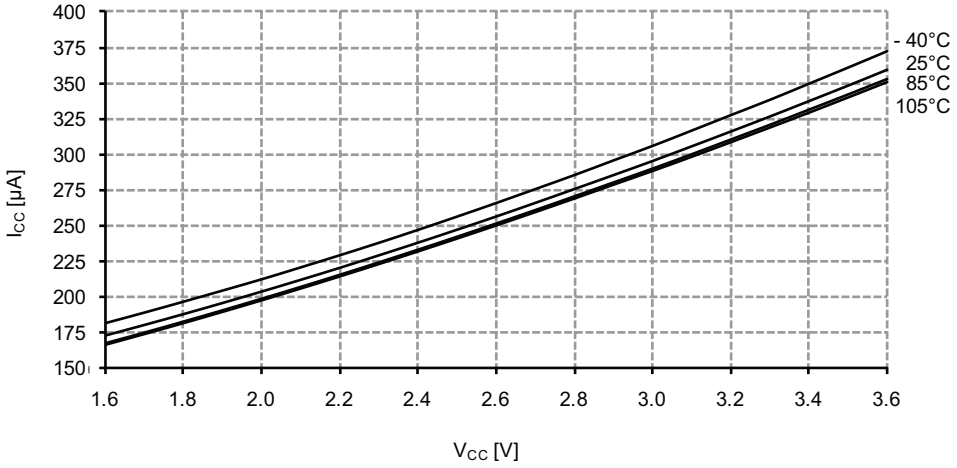


Figure 33-199. DNL Error vs. Input Code

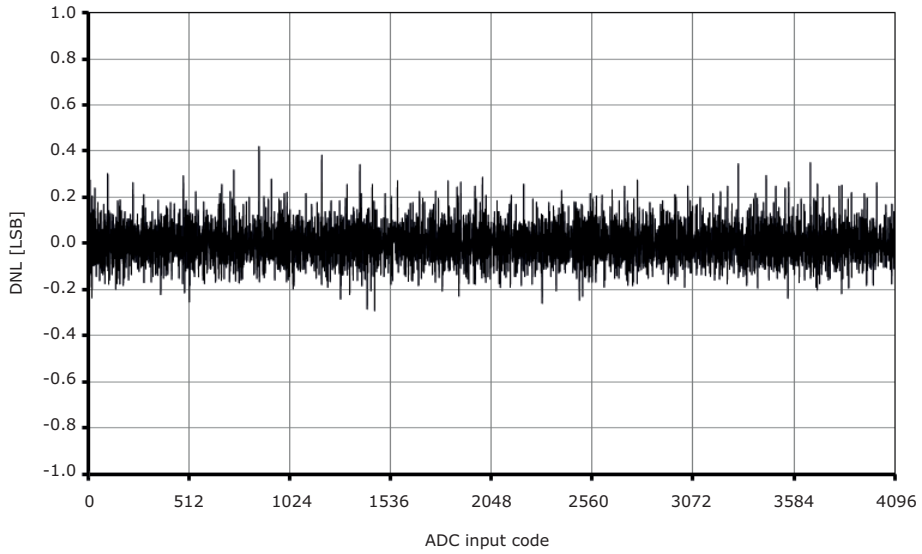


Figure 33-200. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps

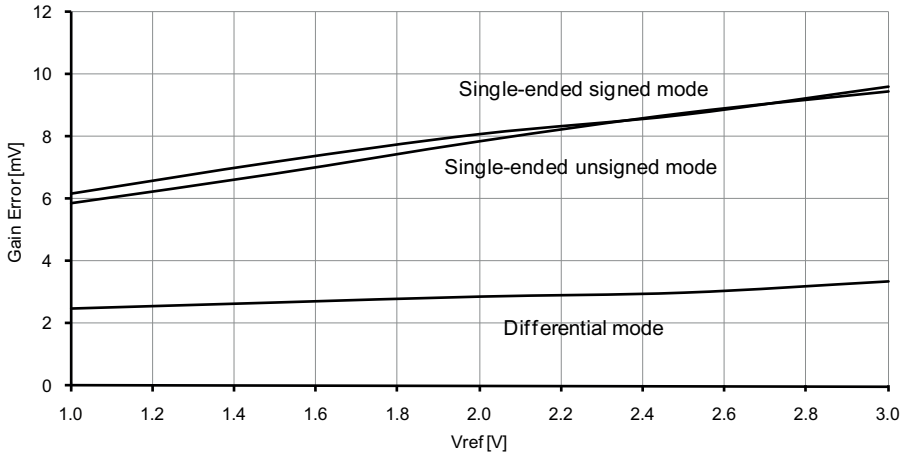
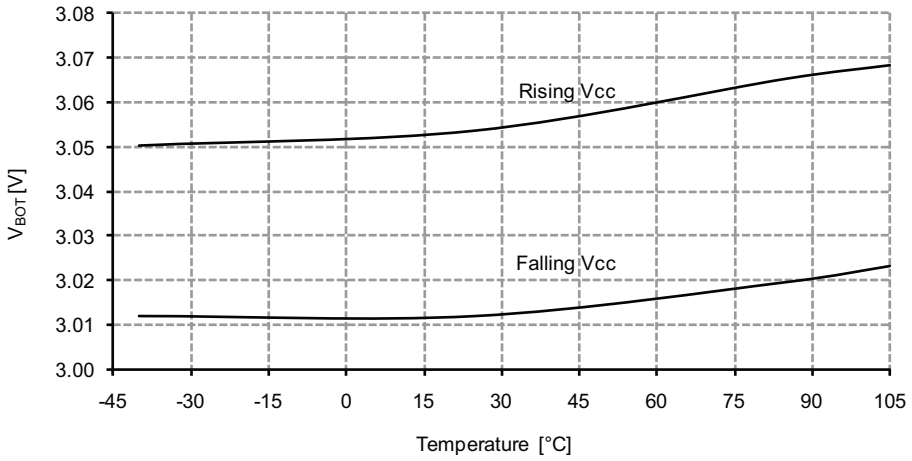


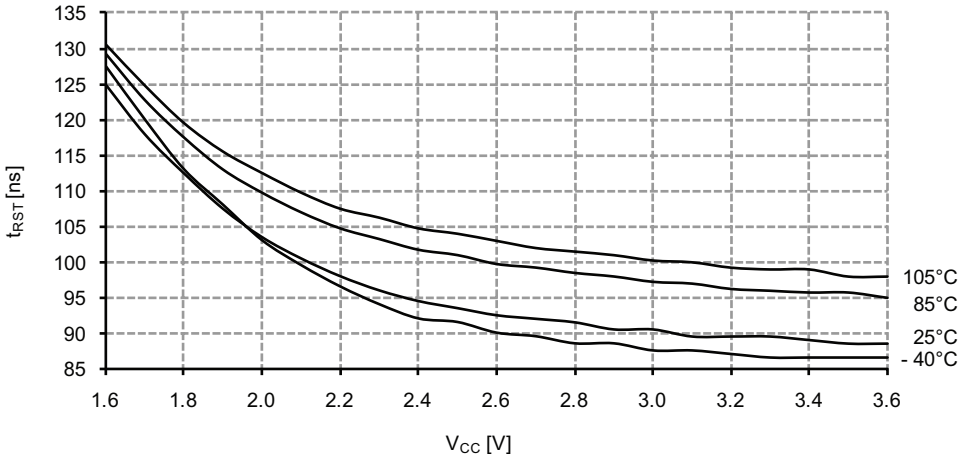
Figure 33-219. BOD Thresholds vs. Temperature

BOD level = 3.0V



33.3.8 External Reset Characteristics

Figure 33-220. Minimum Reset Pin Pulse Width vs. V_{CC}



33.4.4 DAC Characteristics

Figure 33-291. DAC INL Error vs. V_{REF}

V_{CC} = 3.6V

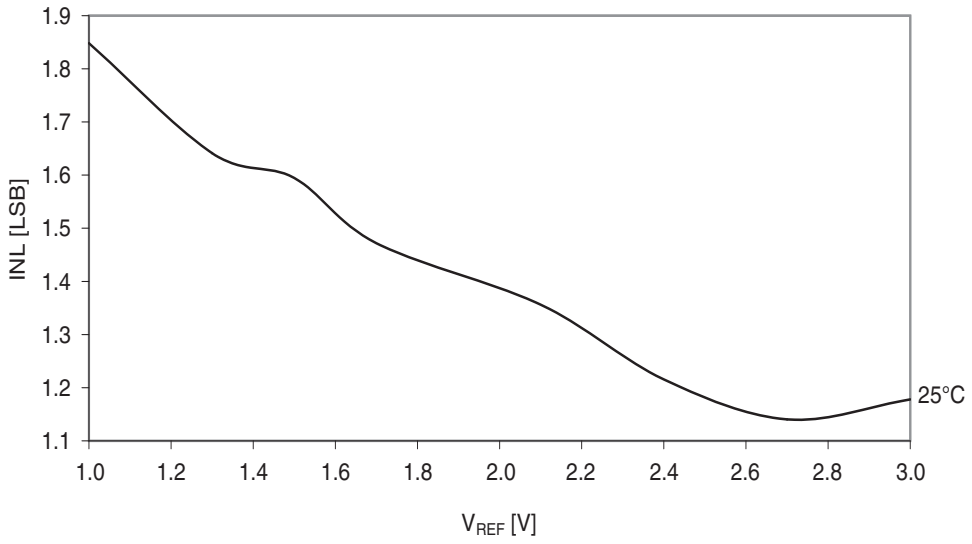


Figure 33-292. DNL Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V

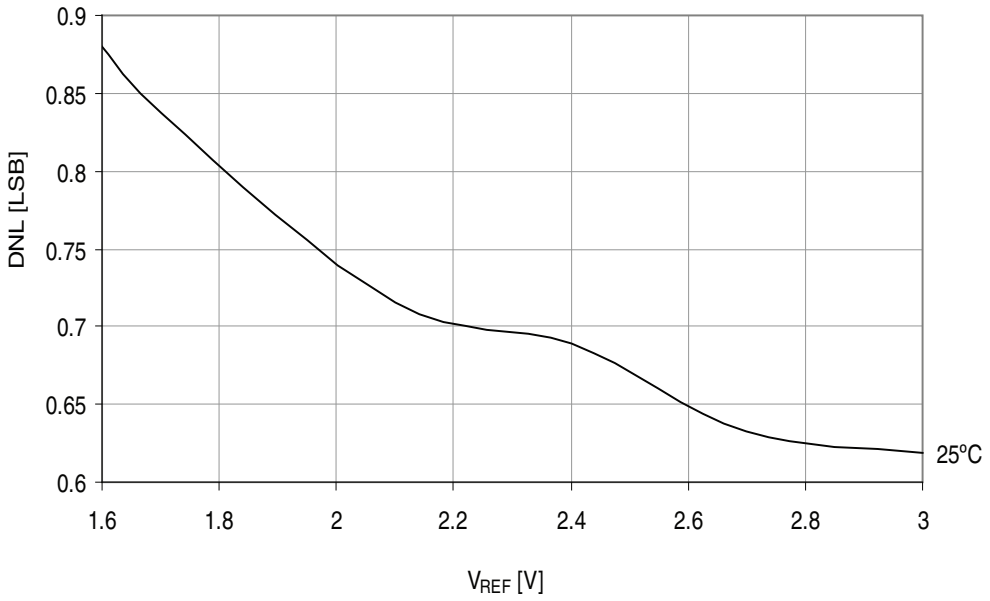


Figure 33-319. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

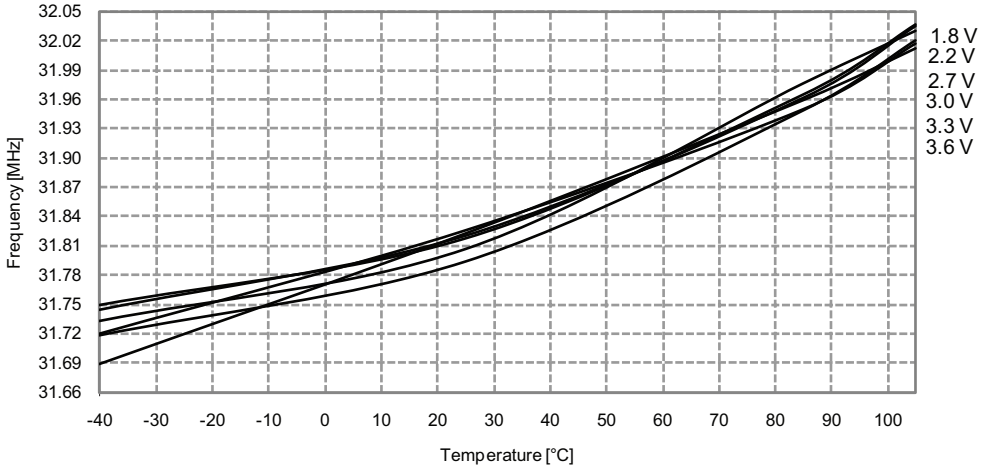
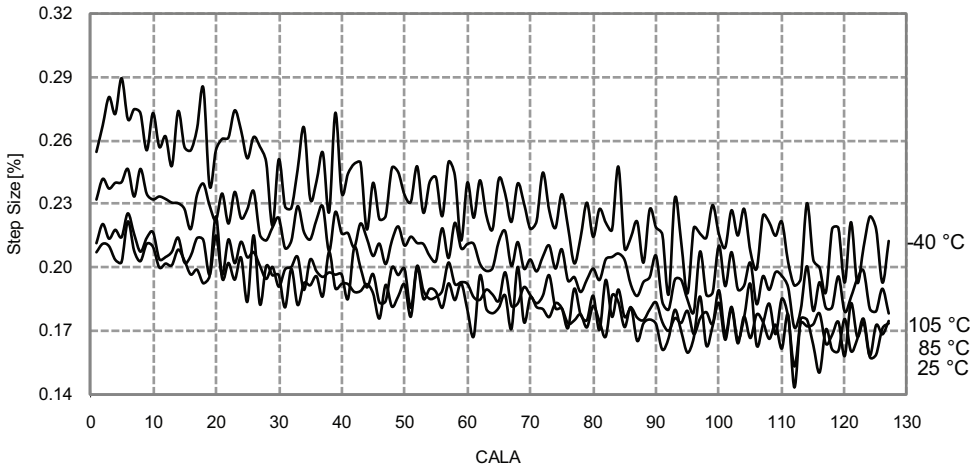


Figure 33-320. 32MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V



1. Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 ìs and could potentially give a wrong comparison result.

Problem fix/Workaround

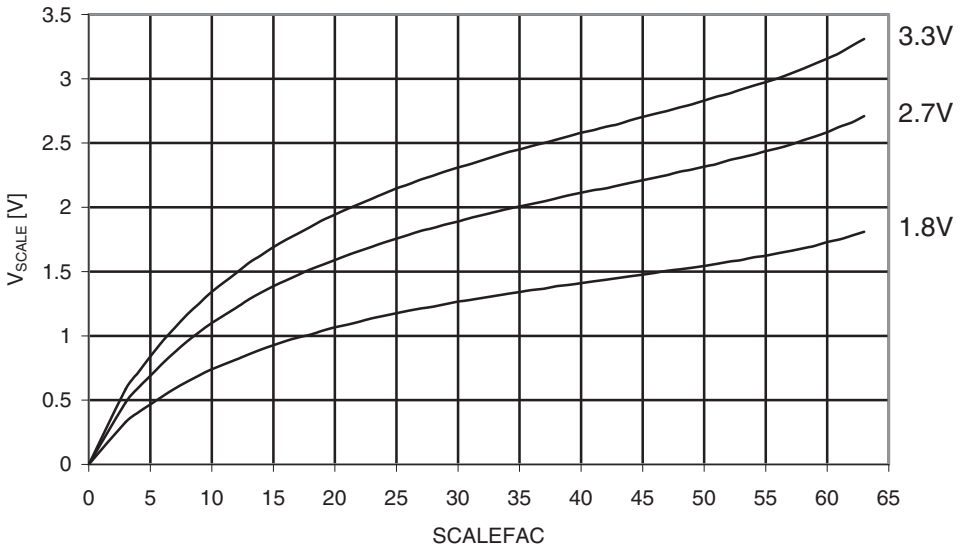
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 34-1. Analog Comparator Voltage Scaler vs. Scalefac

T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

- 6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.
- 6LSB for reference voltage below 1.1V when VCC is above 3.0V.
- 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None. Avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of: