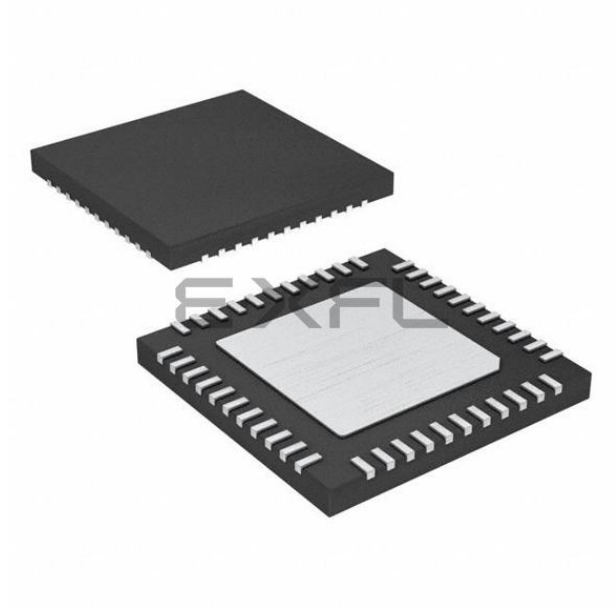

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16d4-mh

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 64.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 14.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes for Atmel AVR XMEGA D4 Devices

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega16D4	42	94	1E
ATxmega32D4	42	95	1E
ATxmega64D4	47	96	1E
ATxmega128D4	47	97	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

14. I/O Ports

14.1 Features

- 34 general purpose input and output pins with individual configuration
- Output driver with configurable driver and pull settings:
  - Totem-pole
  - Wired-AND
  - Wired-OR
  - Bus-keeper
  - Inverted I/O
- Input with synchronous and/or asynchronous sensing with interrupts and events
  - Sense both edges
  - Sense rising edges
  - Sense falling edges
  - Sense low level
- Optional pull-up and pull-down resistor on input and Wired-OR/AND configurations
- Asynchronous pin change sensing that can wake the device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins
  - Hardware read-modify-write through dedicated toggle/clear/set registers
  - Configuration of multiple pins in a single operation
  - Mapping of port registers into bit-accessible I/O memory space
- Peripheral clocks output on port pin
- Real-time counter clock output to port pin
- Event channels can be output on port pin
- Remapping of digital peripheral pin functions
  - Selectable USART, SPI, and timer/counter input/output pin locations

14.2 Overview

One port consists of up to eight port pins: pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, SPI, and timer/counters, can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

The notation of the ports are PORTA, PORTB, PORTC, PORTD, PORTE, and PORTR.

30. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One’s Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two’s Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
Branch instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3[1]

32.3.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-63. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH}(1)/ I_{OL}(2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.7 - 3.6V		2		V_{CC}+0.3	V
		V_{CC} = 2.0 - 2.7V		0.7*V_{CC}		V_{CC}+0.3	
		V_{CC} = 1.6 - 2.0V		0.7*V_{CC}		V_{CC}+0.3	
V_{IL}	Low level input voltage	V_{CC} = 2.7- 3.6V		-0.3		0.3*V_{CC}	
		V_{CC} = 2.0 - 2.7V		-0.3		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.0V		-0.3		0.3*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.0 - 3.6V	I_{OH} = -2mA	2.4	0.94*V_{CC}		
		V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.0 - 3.6V	I_{OL} = 2mA		0.05*V_{CC}	0.4	
		V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current	T = 25°C			<0.001	0.1	µA
R_P	Pull/Buss keeper resistor				24		kΩ
t_r	Rise time	No load			4		ns

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC must not exceed 200mA.
   The sum of all I_{OH} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all I_{OH} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC must not exceed 200mA.
   The sum of all I_{OL} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all I_{OL} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

32.3.6 ADC Characteristics

Table 32-64. Power Supply, Reference and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			190		LSB

Table 32-65. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		1400	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		14		200	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off			200	
		CURRLIMIT = LOW			150	
		CURRLIMIT = MEDIUM			100	
		CURRLIMIT = HIGH			50	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0, 1, 2 or 3	5	7	10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	
		After ADC flush		1	1	

Table 32-81. External Clock with Prescaler[1] for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency[2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock high time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock low time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise time (for maximum frequency)				1.5	
t_{CF}	Fall time (for maximum frequency)				1.5	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.3.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 32-82. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		

32.4.14 SPI Characteristics

Figure 32-26.SPI Timing Requirements in Master Mode

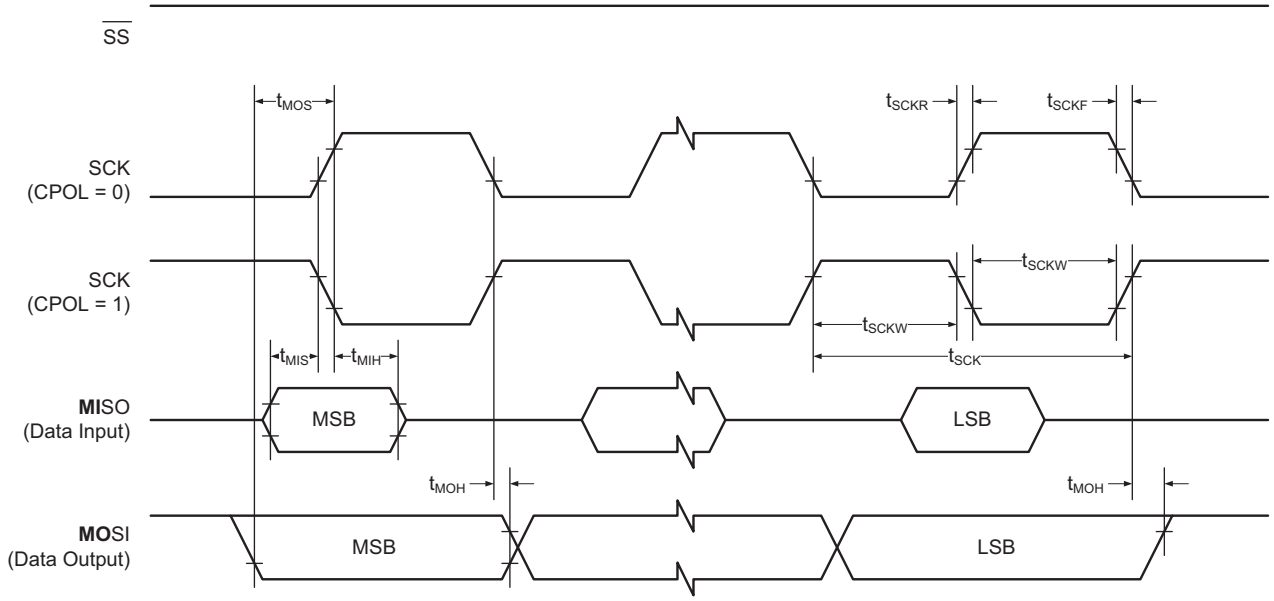
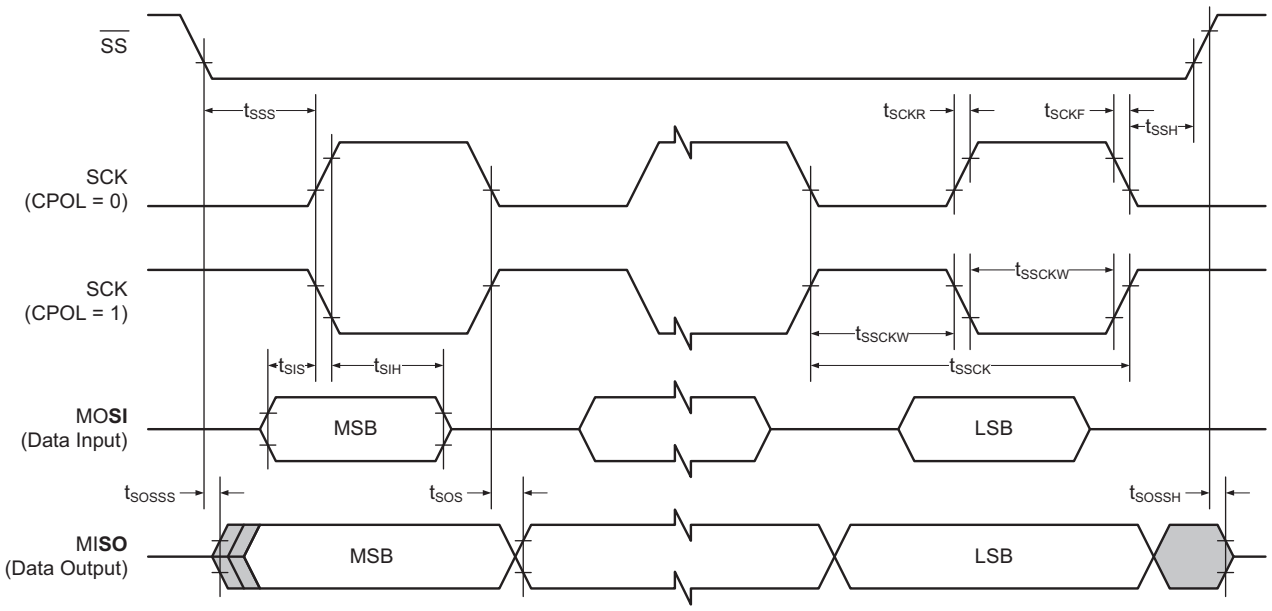


Figure 32-27.SPI Timing Requirements in Slave Mode



33.1.4 Analog Comparator Characteristics

Figure 33-47. Analog Comparator Hysteresis vs. V_{CC}

High speed, small hysteresis

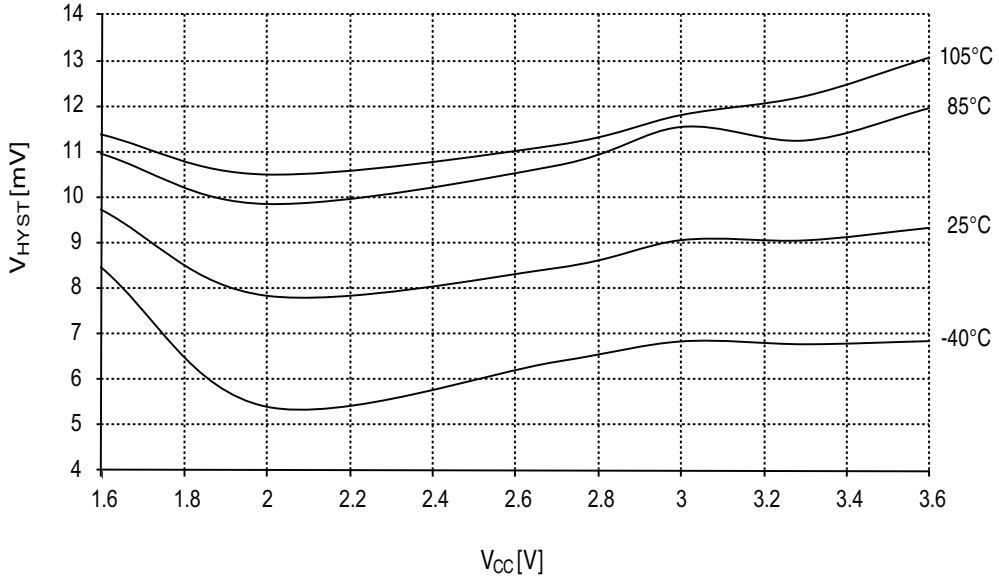


Figure 33-48. Analog Comparator Hysteresis vs. V_{CC}

High speed, large hysteresis

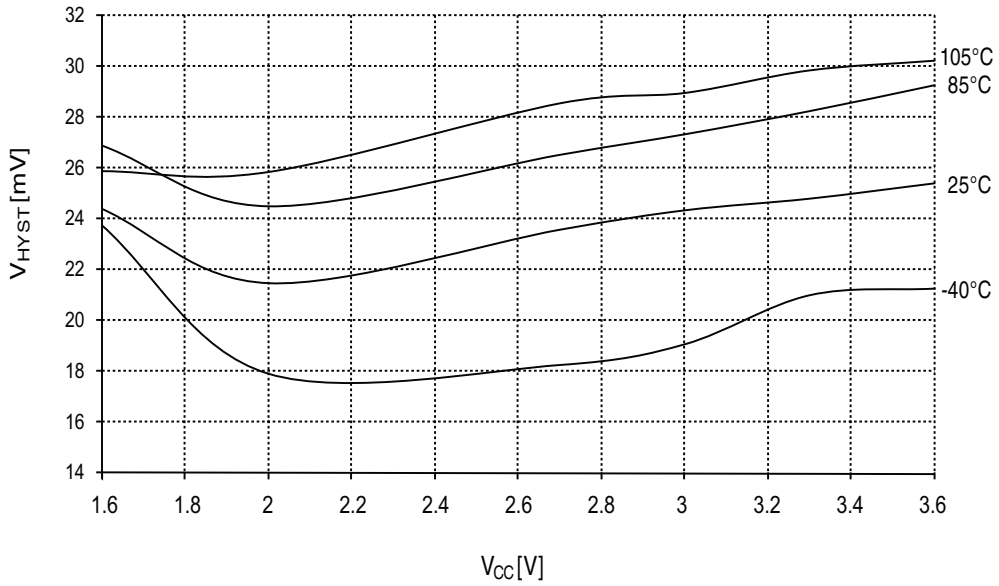


Figure 33-118. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

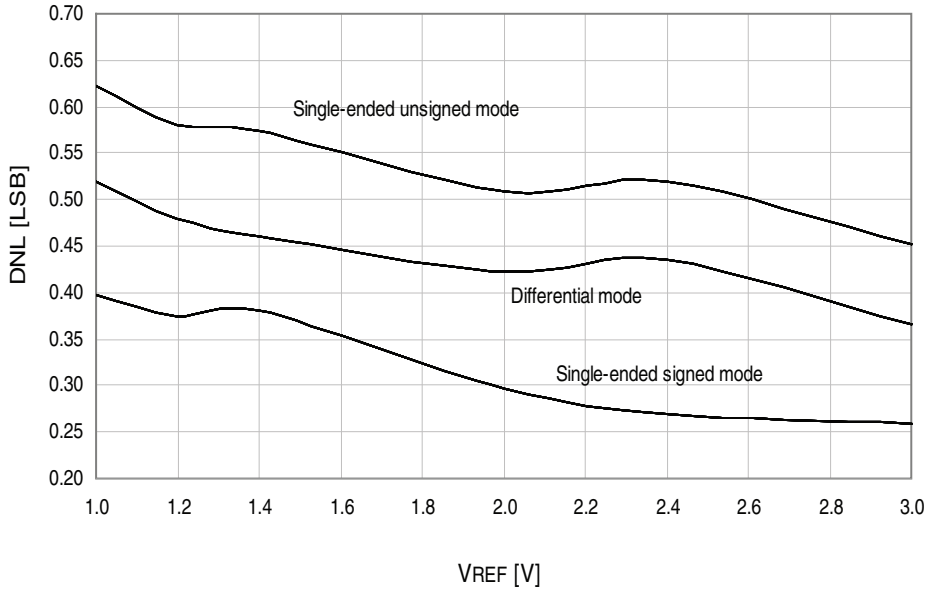


Figure 33-119. DNL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

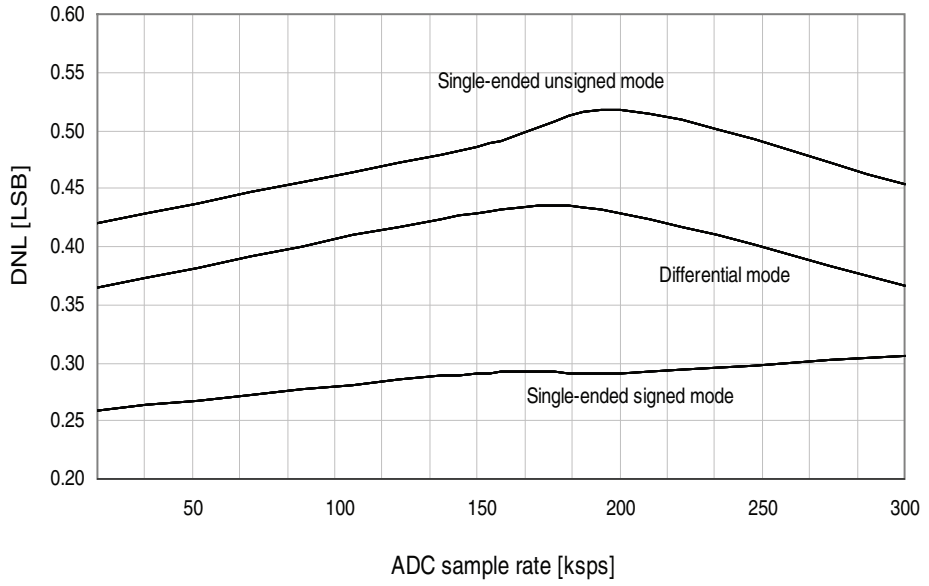


Figure 33-122. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 200ksps

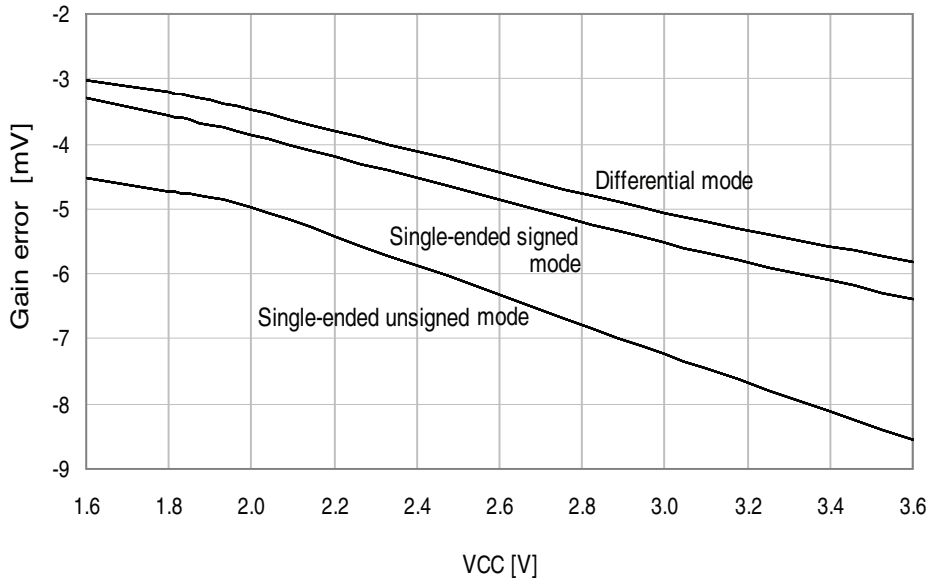


Figure 33-123. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

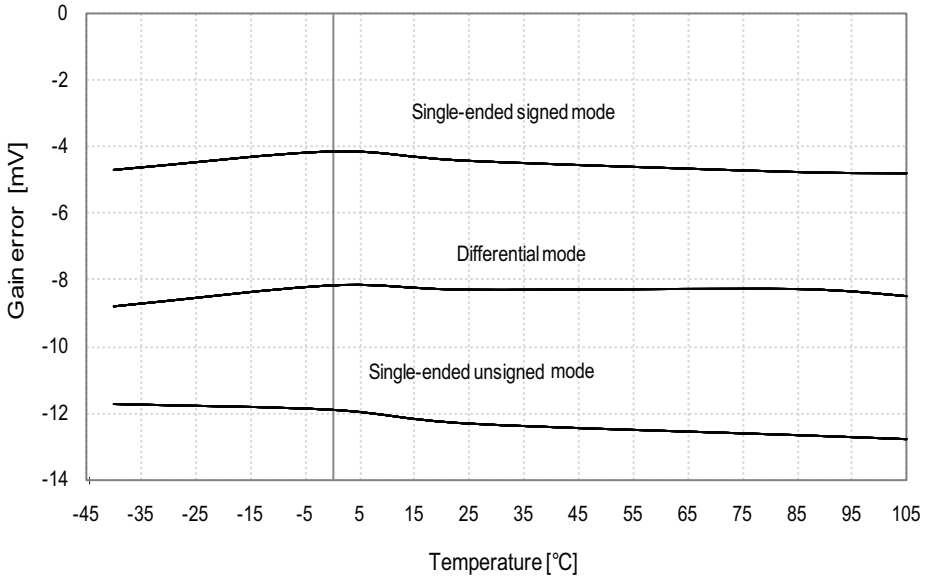
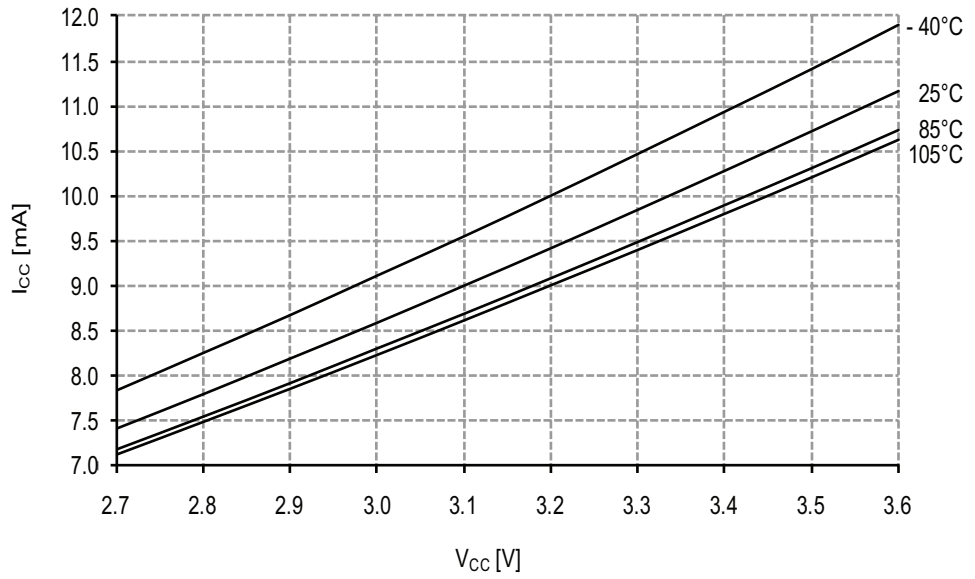


Figure 33-165. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.3.1.2 Idle Mode Supply Current

Figure 33-166. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

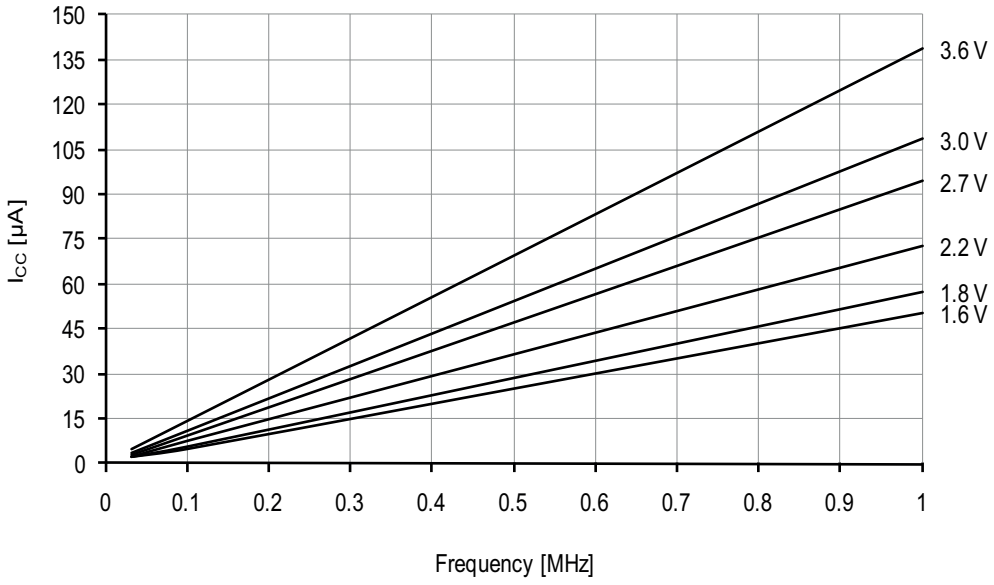


Figure 33-171. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

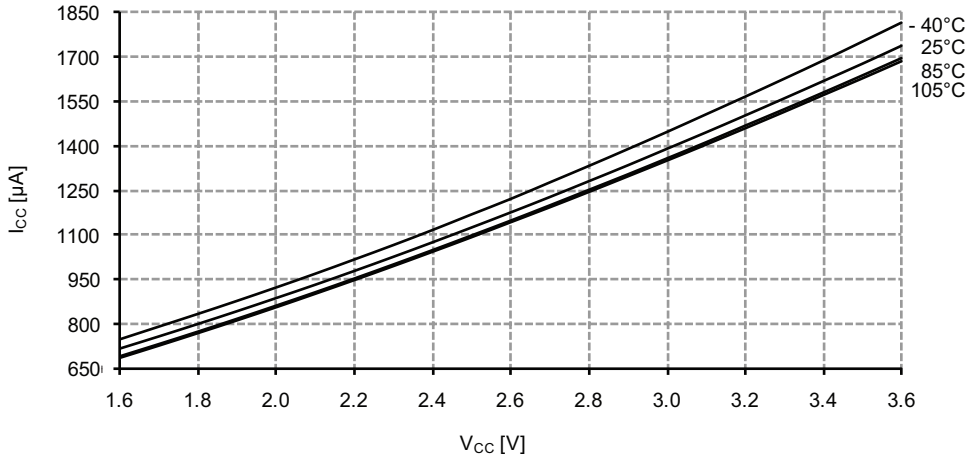


Figure 33-172. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

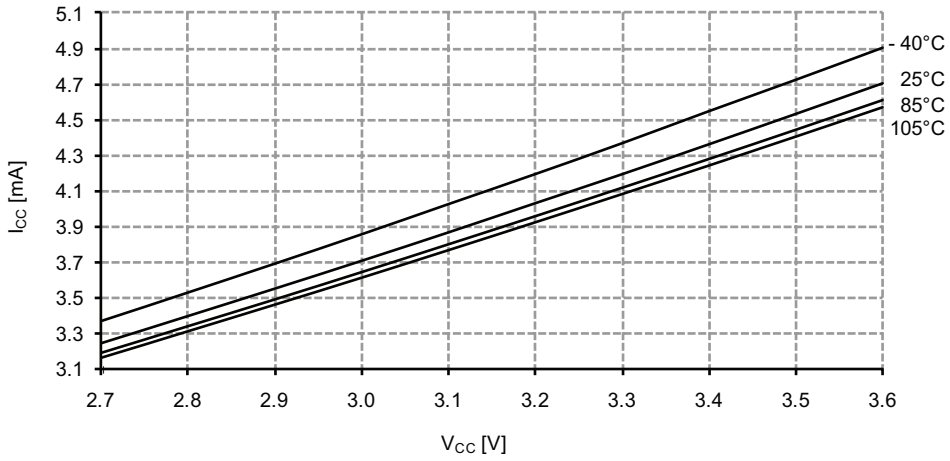
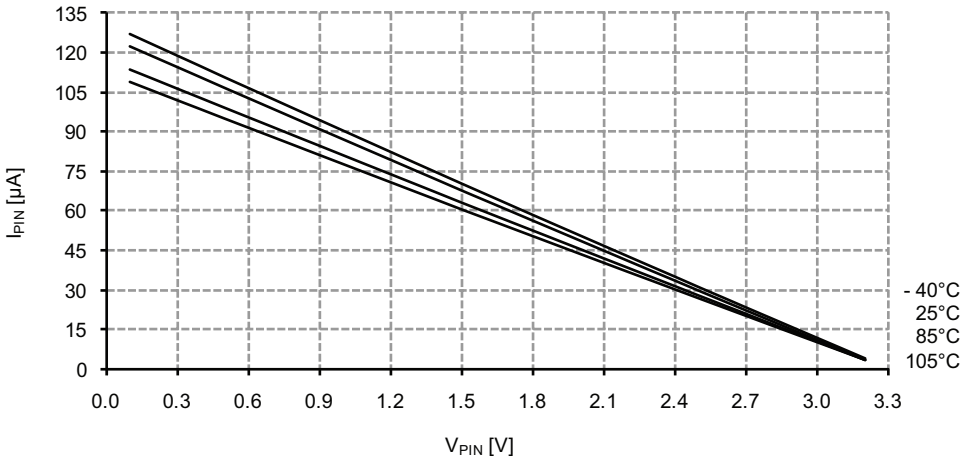


Figure 33-181. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



33.3.2.2 Output Voltage vs. Sink/Source Current

Figure 33-182. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V

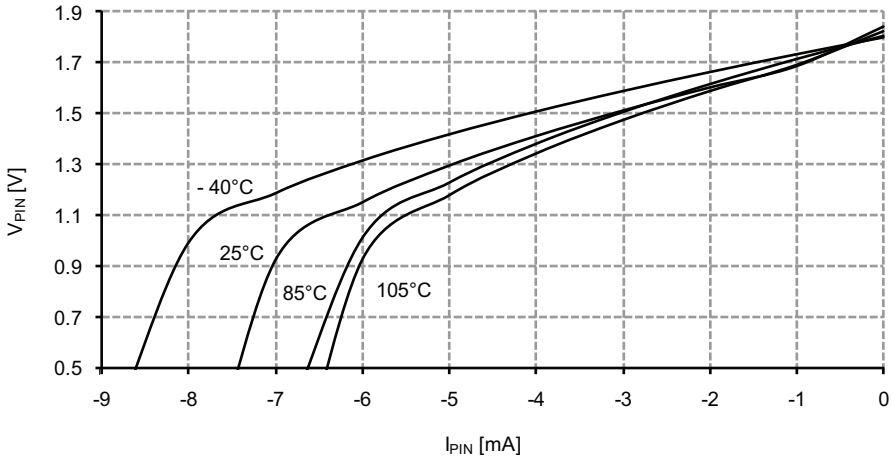


Figure 33-211. Analog Comparator Hysteresis vs. V_{CC}

Low power, small hysteresis

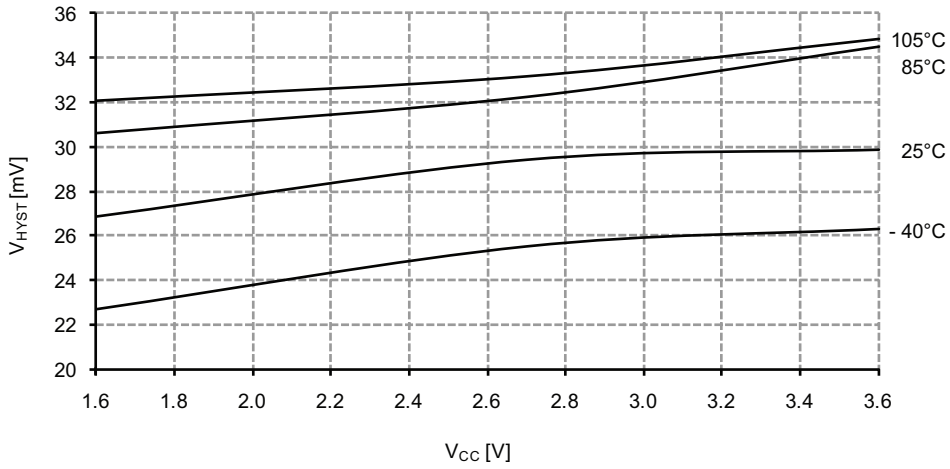


Figure 33-212. Analog Comparator Hysteresis vs. V_{CC}

High-speed mode, large hysteresis

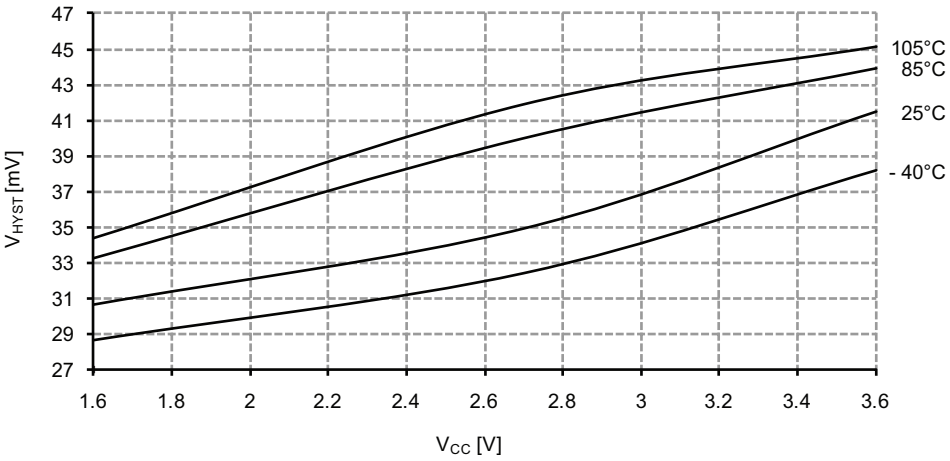


Figure 33-253. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

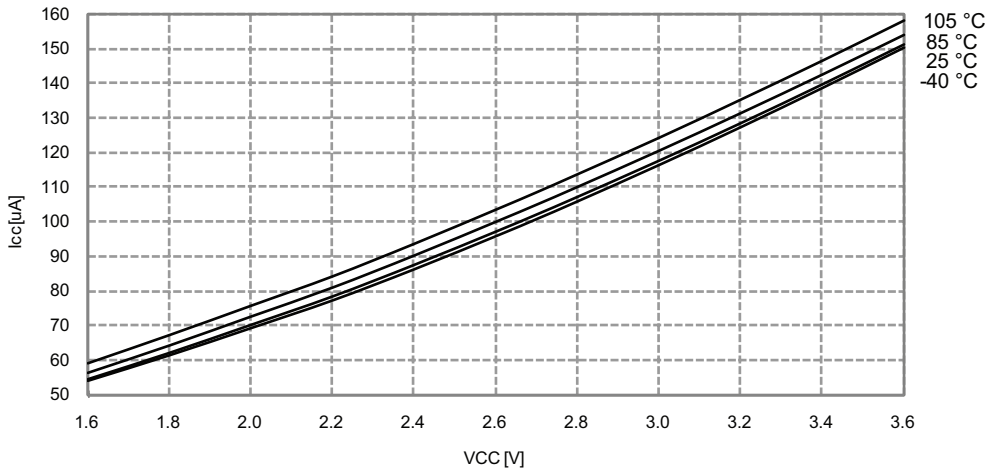
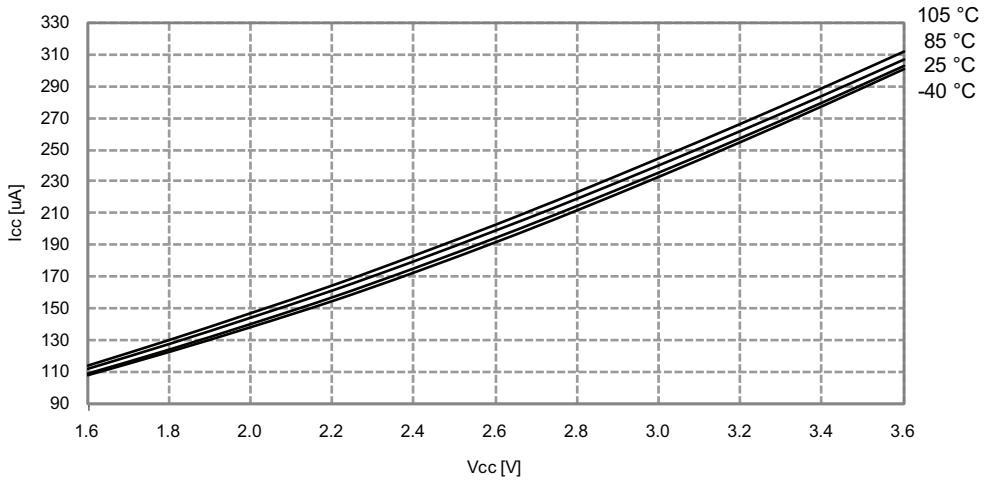


Figure 33-254. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator



33.4.1.5 Standby Mode Supply Current

Figure 33-261. Standby Supply Current vs. V_{CC}

Standby, f_{SYS} = 1MHz

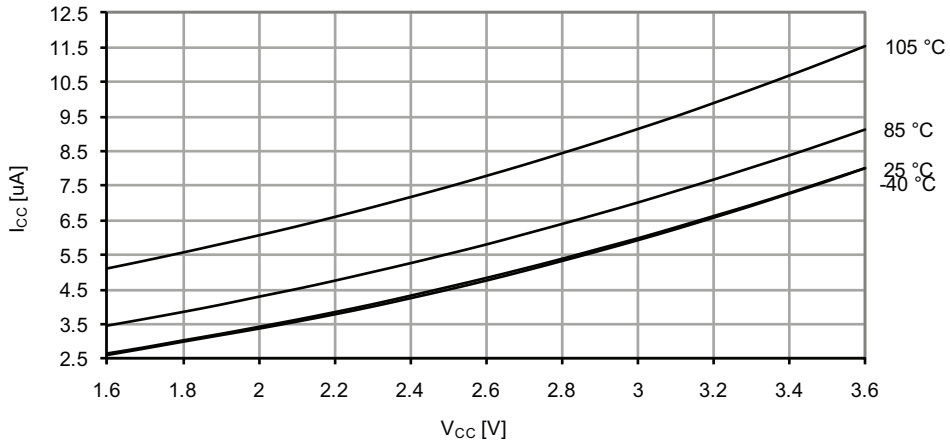
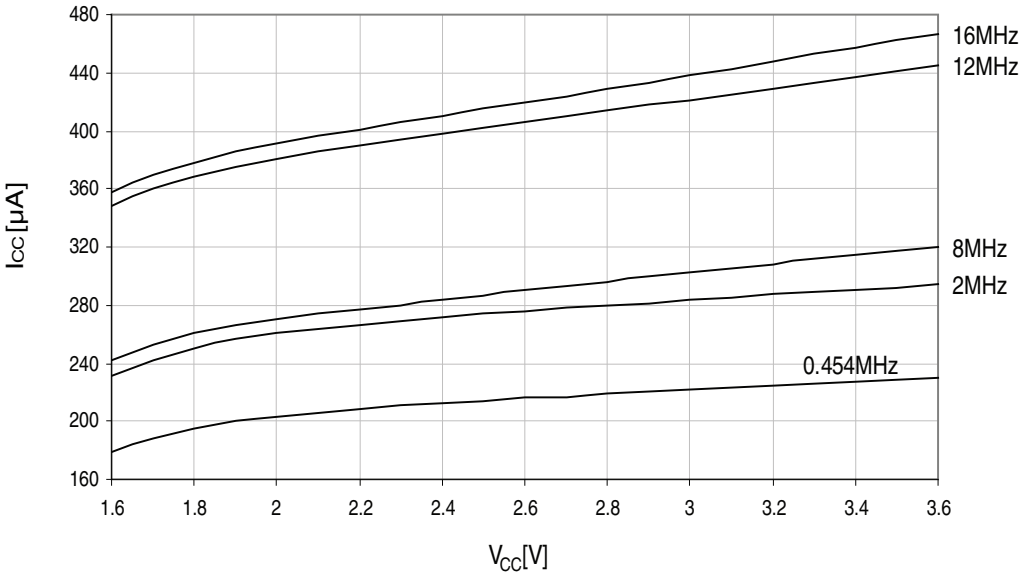


Figure 33-262. Standby Supply Current vs. V_{CC}

T = 25°C, running from different crystal oscillators



33.4.2 I/O Pin Characteristics

33.4.2.1 Pull-up

Figure 33-263. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *1.8V*

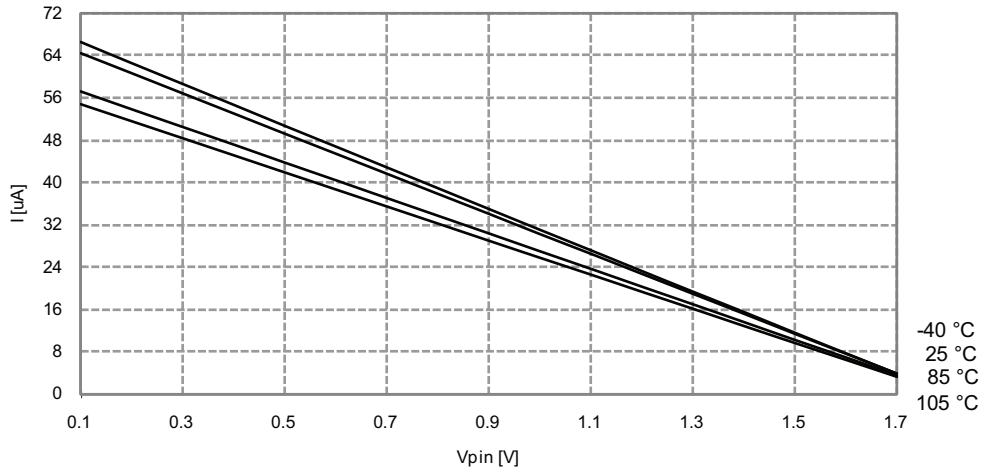
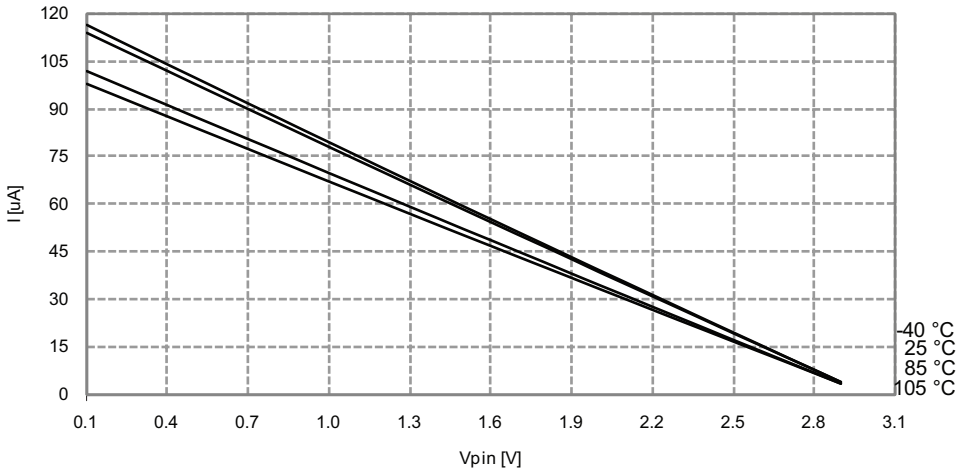


Figure 33-264. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *3.0V*



34.1.5 Rev. A/B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4 V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8x -64x gain is used
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA A Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD: BOD will be enabled at any reset
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Flash Power Reduction Mode can not be enabled when entering sleep
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Inverted I/O enable does not affect Analog Comparator Output
- TWIE is not available
- CRC generator module is not available
- ADC 1/x gain setting and VCC/2 reference setting is not available
- TOSC alternate pin locations is not available
- TWI SDAHOLD time configuration is not available
- Timer/Counter 2 is not available
- HIRES+ option is not available
- Alternate pin locations for digital peripherals are not available
- XOSCPWR high drive option for external crystal is not available
- PLL divide by two option is not available
- Real Time Counter non-prescaled 32kHZ clock options are not available
- PLL lock detection failure function is not available
- Non available functions and options
- Temperature sensor not calibrated
- Disabling the USART transmitter does not automatically set the TxD pin direction to output.

34.2 ATxmega64D4

34.2.1 Rev. D

- Temperature sensor not calibrated

1. **Temperature sensor not calibrated**

   Temperature sensor factory calibration not implemented.

   Problem fix/Workaround

   None.

34.2.2 Rev. B/C

Not sampled.

34.2.3 Rev. A

- ADC may have missing codes in SE unsigned mode at low temp and low V_{CC}
- Temperature sensor not calibrated

1. **ADC may have missing codes in SE unsigned mode at low temp and low V_{CC}**

   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   Problem fix/Workaround

   Use the ADC in SE signed mode.

2. **Temperature sensor not calibrated**

   Temperature sensor factory calibration not implemented.

   Problem fix/Workaround

   None.

34.3 ATxmega128D4

34.3.1 Rev. A

- Temperature sensor not calibrated

1. **Temperature sensor not calibrated**

   Temperature sensor factory calibration not implemented.

   Problem fix/Workaround

   None.

35.15 8135E – 02/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Updated Table 7-3 on page 18. No of Pages for ATxmega32D4: 32
3. Updated ”Alternate Port Functions” on page 29.
4. Updated ”ADC - 12-bit Analog to Digital Converter” on page 39.
5. Updated Figure 25-1 on page 50.
6. Updated ”Alternate Pin Functions” on page 48.
7. Updated ”Timer/Counter and AWEX functions” on page 46.
8. Added Table 31-17 on page 65.
9. Added Table 31-18 on page 66.
10. Changed Internal Oscillator Speed to ”Oscillators and Wake-up Time” on page 85.
11. Updated ”Errata” on page 90.

35.16 8135D – 12/09

1. Added ATxmega128D4 device and updated the datasheet accordingly.
2. Updated ”Electrical Characteristics” on page 58 with Max/Min numbers.
3. Added ”Flash and EEPROM Memory Characteristics” on page 61.
4. Updated Table 31-10 on page 64, Input hysteresis is in V and not in mV.
5. Added ”Errata” on page 90.

35.17 8135C – 10/09

1. Updated ”Features” on page 1 with Two Two-Wire Interfaces.
2. Updated ”Block Diagram and QFN/TQFP pinout” on page 3.
3. Updated ”Overview” on page 5.
4. Updated ”XMEGA D4 Block Diagram” on page 7.
5. Updated Table 13-1 on page 24.
6. Updated ”Overview” on page 35.
7. Updated Table 27-5 on page 49.
8. Updated ”Peripheral Module Address Map” on page 50.

35.18 8135B – 09/09

1. Added ”Electrical Characteristics” on page 58.
2. Added ”Typical Characteristics” on page 67.