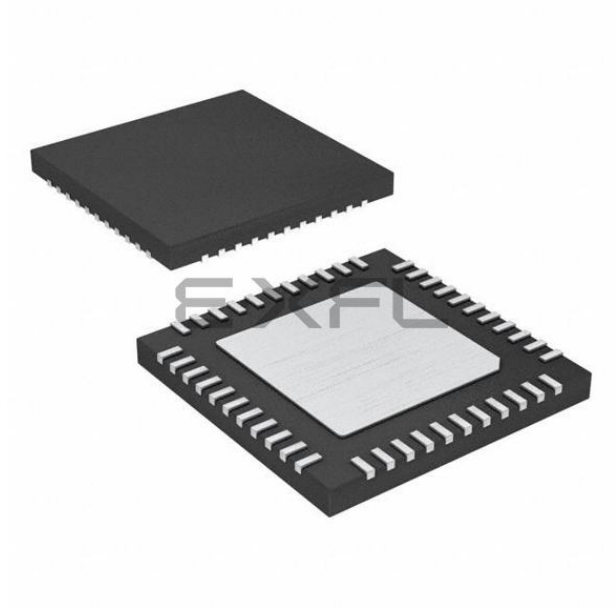

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16d4-mha2

28.1.6 Oscillators, Clock and Event

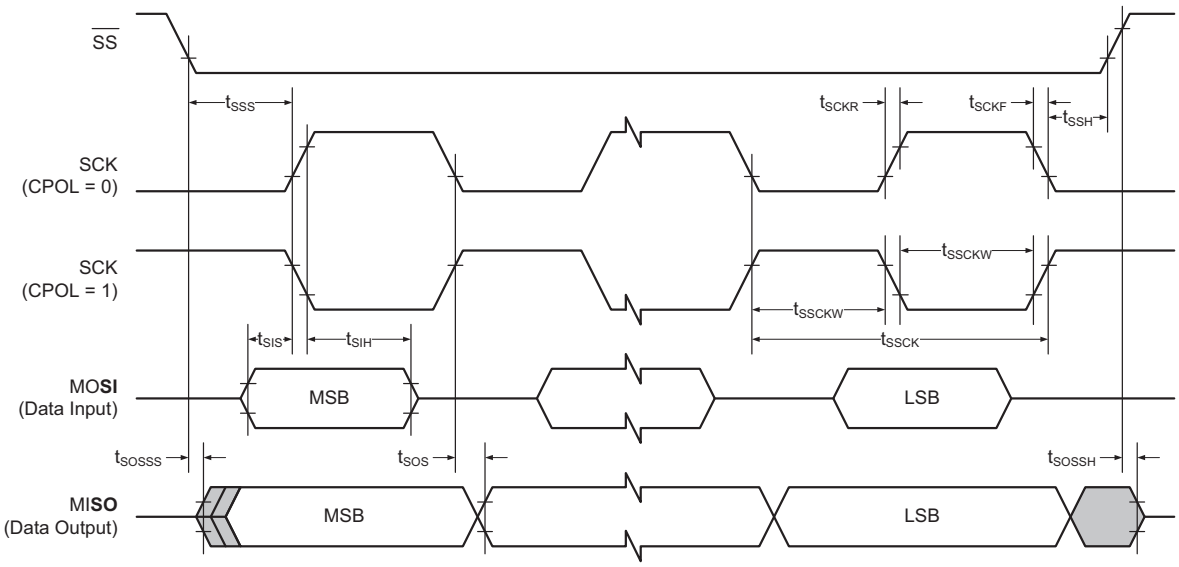
TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

28.1.7 Debug/System Functions

$\overline{\text{RESET}}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2[1][2]
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2[1][2]
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1[1][2]
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1[1][2]
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2[1][2]
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2[1][2]
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2[1]
ST	X, Rr	Store Indirect	(X) ← Rr	None	1[1]
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1[1]
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2[1]
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1[1]
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1[1]
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2[1]
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2[1]
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1[1]
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1[1]
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2[1]
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2[1]
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-

Figure 32-6. SPI Timing Requirements in Slave Mode



32.2.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-35. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-20		20	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4- 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.7		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		30	90	ns
					30		
	64-Level voltage scaler	Integral non-linearity (INL)			0.3	0.5	lsb

32.4.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-98. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

32.4.9 Brownout Detection Characteristics

Table 32-99. Brownout Detection Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

32.4.13.6 External Clock Characteristics

Figure 32-24.External Clock Drive Waveform

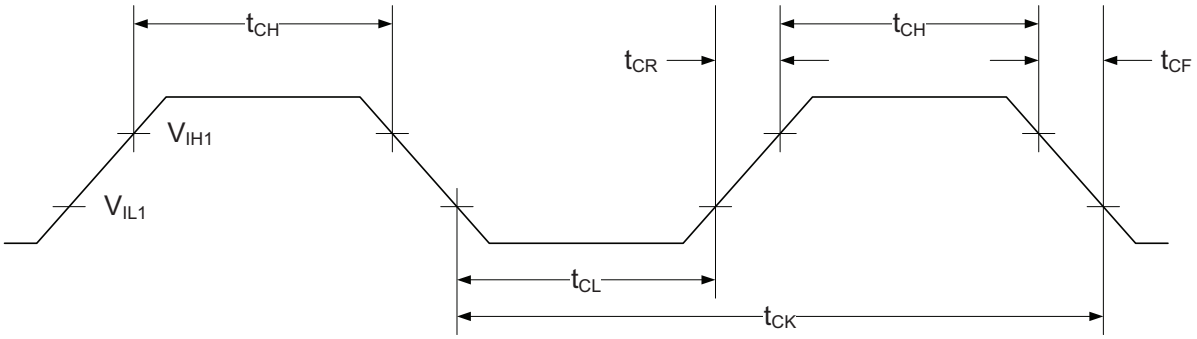


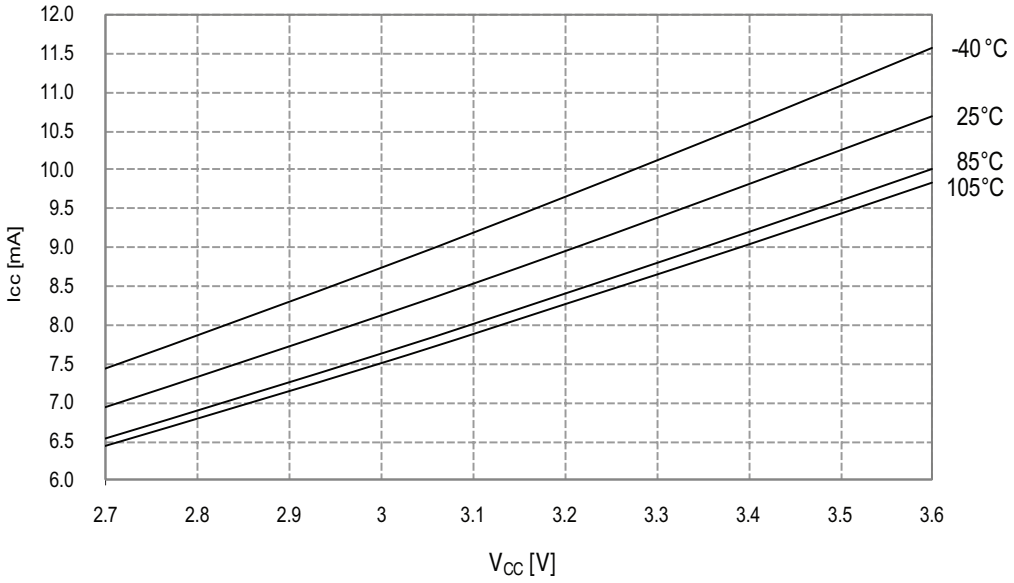
Table 32-109. External Clock Used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency[1]	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock high time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock low time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.

Figure 33-7. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.1.1.2 Idle Mode Supply Current

Figure 33-8. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

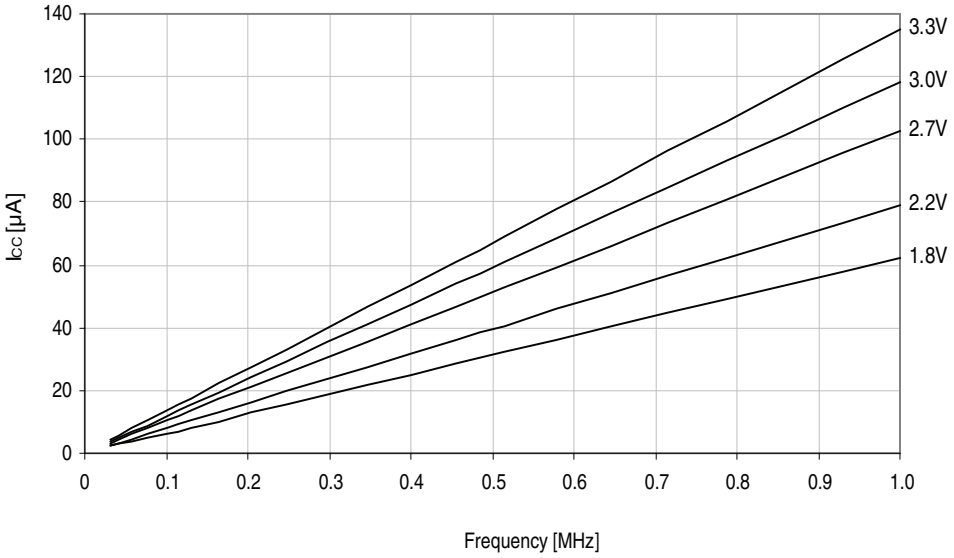


Figure 33-9. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

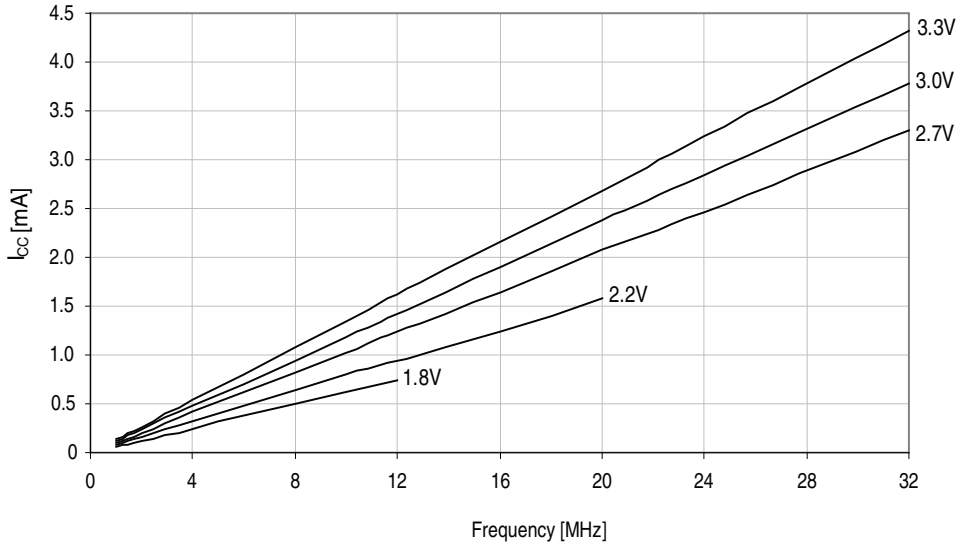


Figure 33-10. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

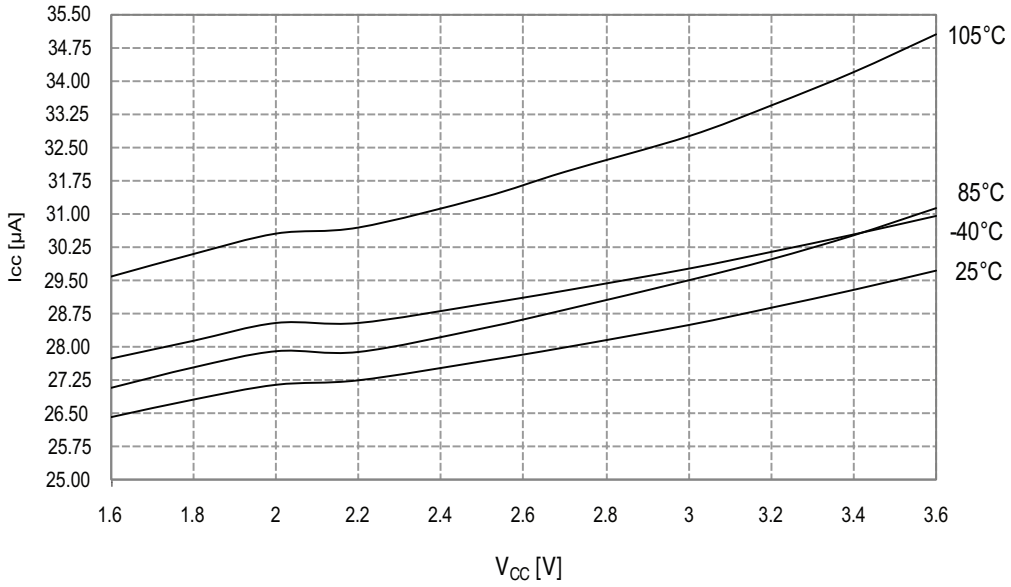
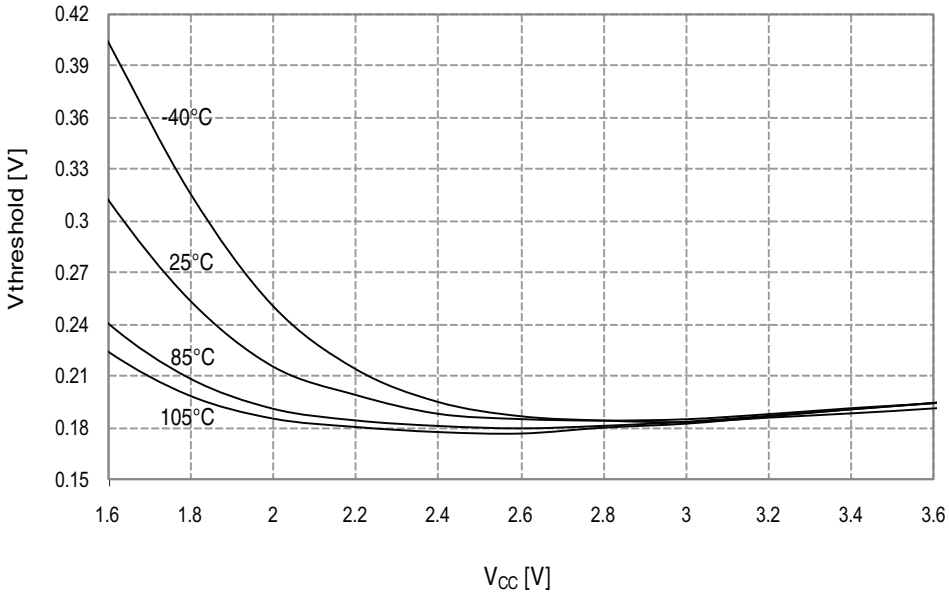


Figure 33-35. I/O Pin Input Hysteresis vs. V_{CC}



33.1.3 ADC Characteristics

Figure 33-36. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

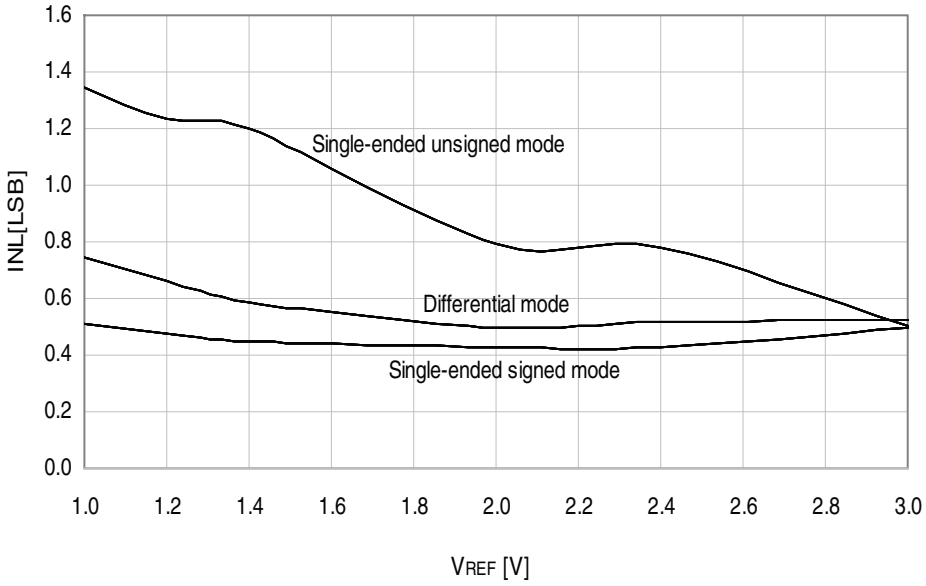


Figure 33-43. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 200ksps

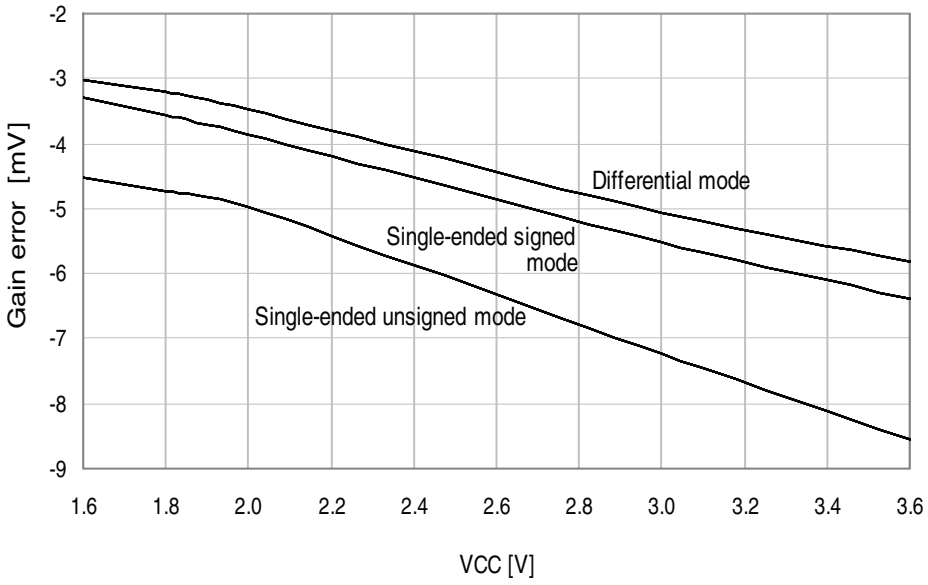


Figure 33-44. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps

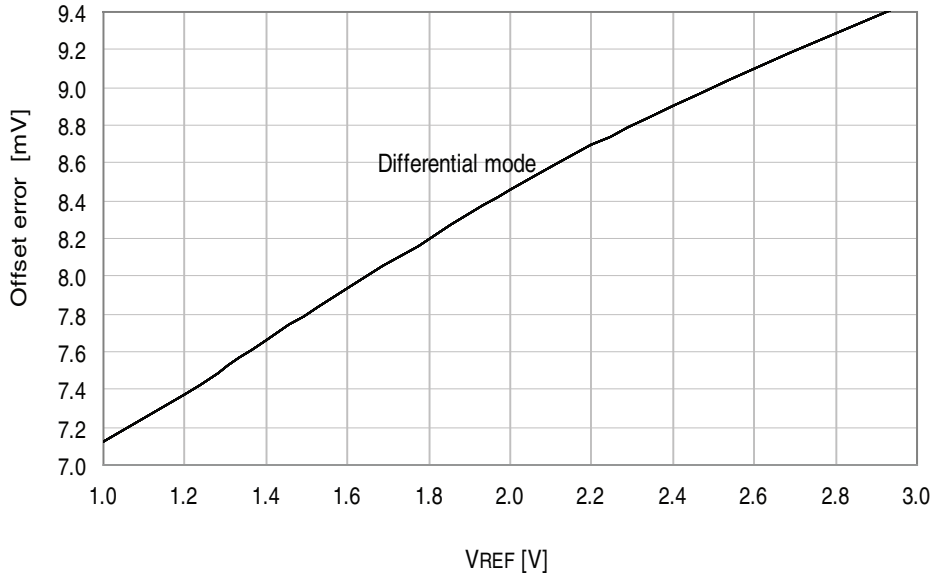
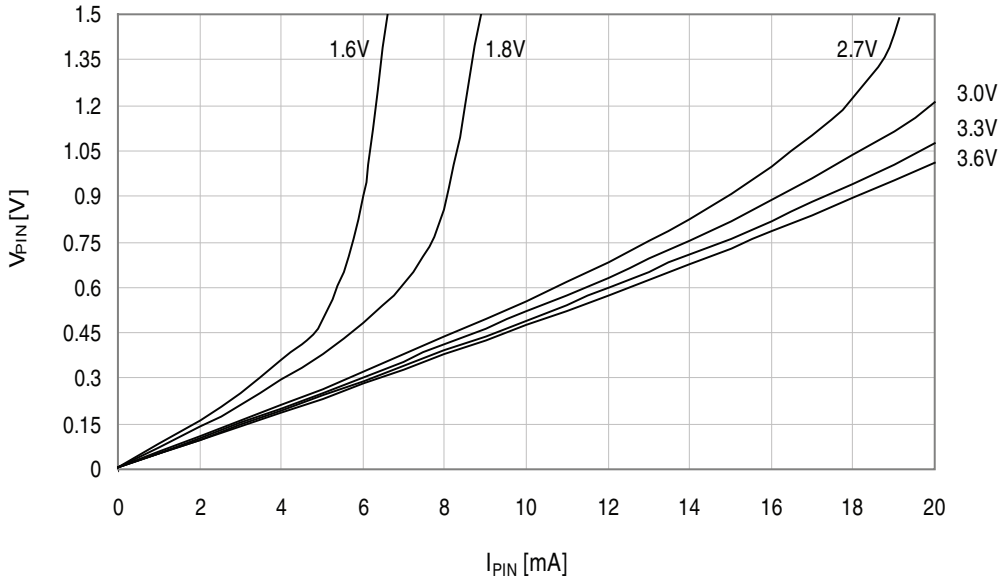


Figure 33-110. I/O Pin Output Voltage vs. Sink Current



33.2.2.3 Thresholds and Hysteresis

Figure 33-111. I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C

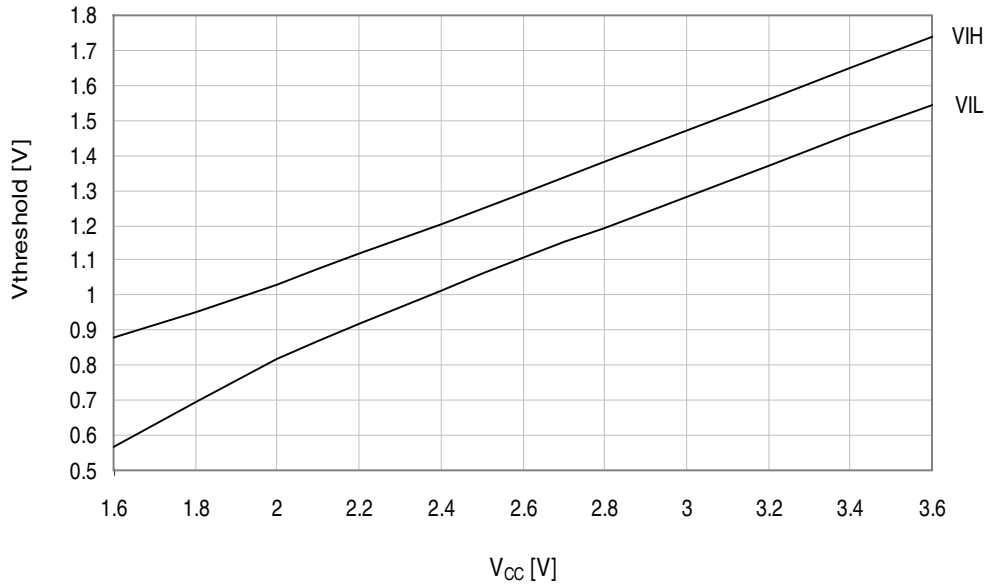
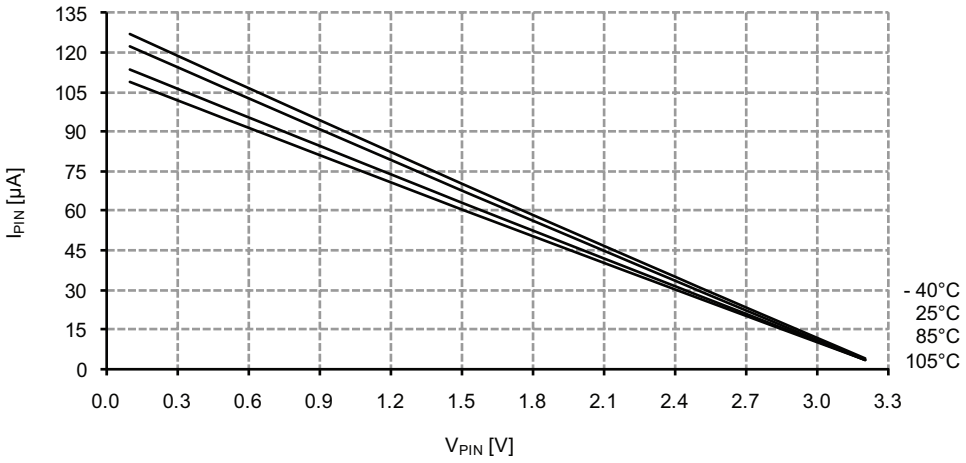


Figure 33-181. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



33.3.2.2 Output Voltage vs. Sink/Source Current

Figure 33-182. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V

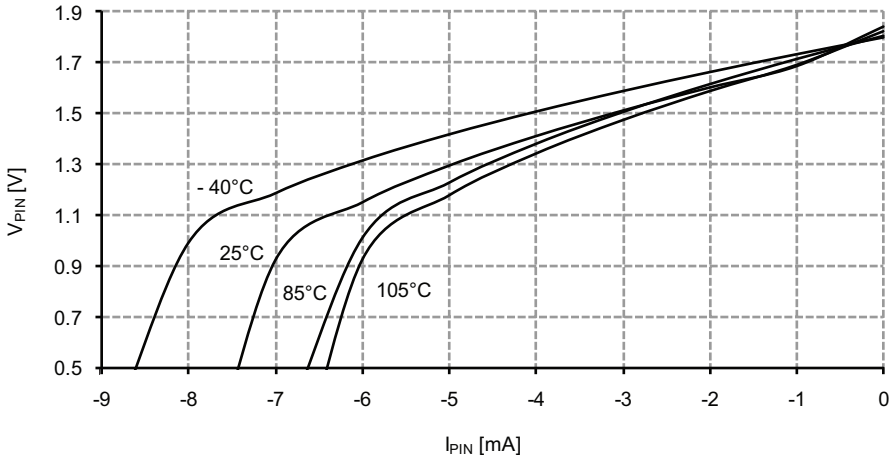


Figure 33-197. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

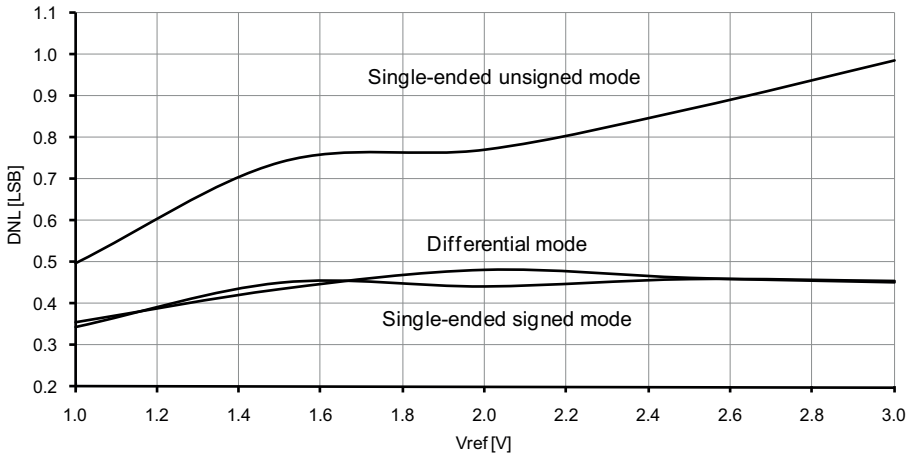
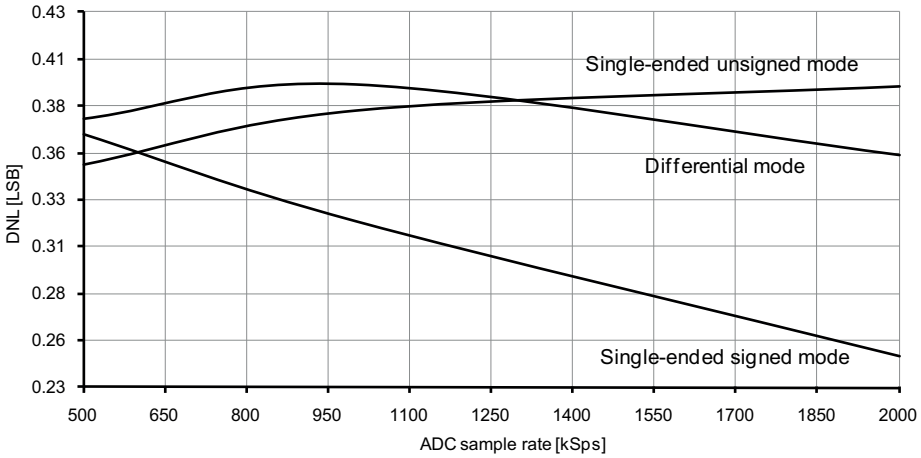


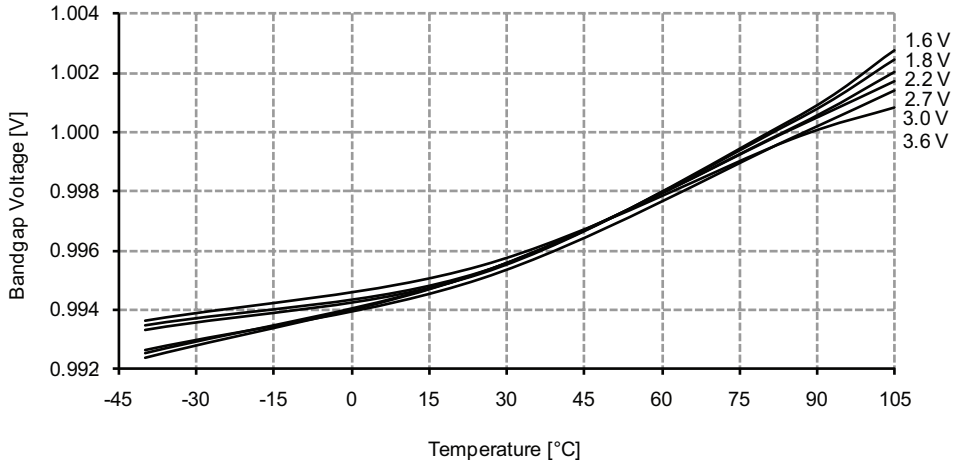
Figure 33-198. DNL Error vs. Sample rate

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external



33.3.6 Internal 1.0V Reference Characteristics

Figure 33-217. ADC/DAC Internal 1.0V Reference vs. Temperature



33.3.7 BOD Characteristics

Figure 33-218. BOD Thresholds vs. Temperature

BOD level = 1.6V

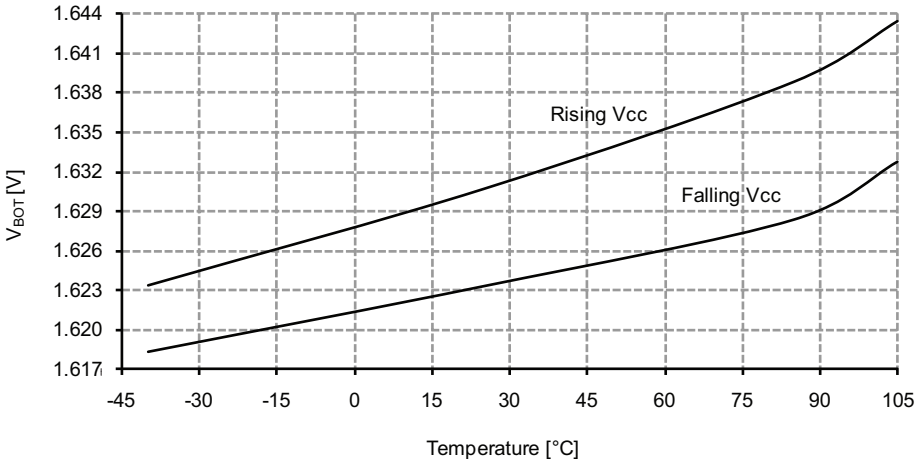


Figure 33-271. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

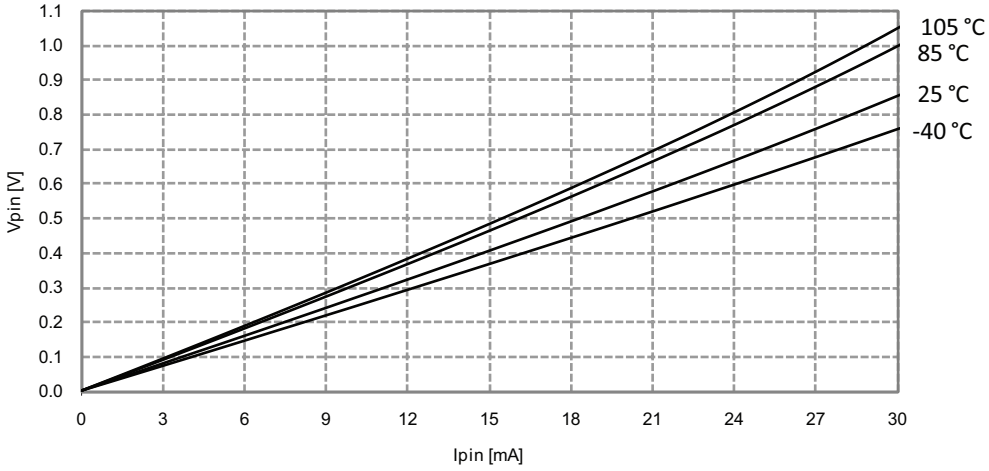


Figure 33-272. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

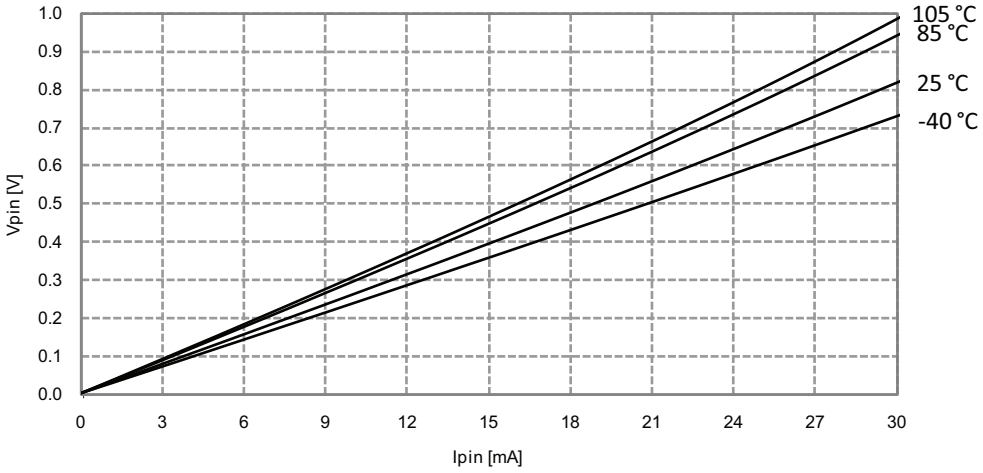


Figure 33-319. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

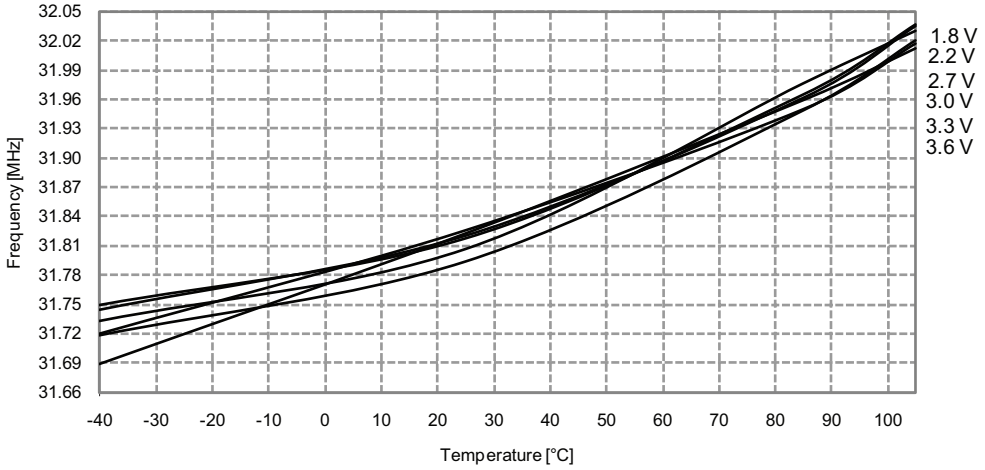
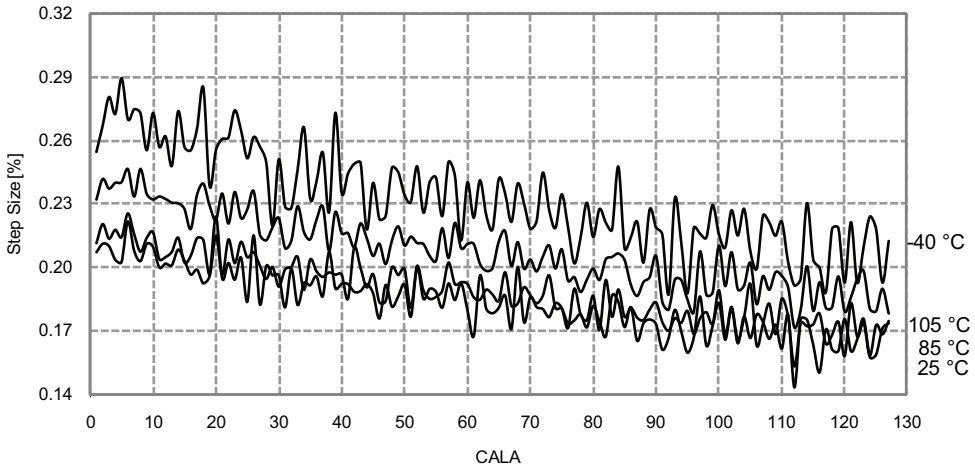


Figure 33-320. 32MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V



1x gain:	2.4V
2x gain:	1.2V
4x gain:	0.6v
8x gain:	300mV
16x gain:	150mV
32x gain:	75mV
64x gain:	38mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

5. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. **ADC propagation delay is not correct when 8x -64x gain is used**

The propagation delay will increase by only one ADC clock cycle for 8x and 16x gain setting, and 32x and 64x gain settings.

Problem fix/Workaround

None.

7. **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

8. **Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

9. **Configuration of PGM and CWCM not as described in XMEGA A Manual**

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Configure the analog comparator setup to give an inverted result, or use an external inverter to change polarity of Analog Comparator Output.

27. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE.
- TWI SDAHOLD option in the TWI CTRL register is one bit.
- CRC generator module.
- ADC 1/2x gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register.
- ADC V_{CC}/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register.
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register.
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register.
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register.
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers.
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register.
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register.
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register.
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register.
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register.
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register.
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register.
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory.

Problem fix/Workaround

None.

28. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/Workaround

None.

29. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/Workaround

The TxD pin direction can be set to input using the Port DIR register. Be advised that setting the Port DIR register to input will be immediate. Ongoing transmissions will be truncated.

35. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

35.1 8135S – 09/2016

1.	Updated “Instruction Set Summary” on page 56. Removed “DES” instruction.
2.	Updated “Gain Stage Characteristics” : Table 32-11 on page 72, Table 32-39 on page 91Table 32-67 on page 110 and Table 32-96 on page 131. “Offset Error, input referred” is changed to “Offset Error, output referred.

35.2 8135R – 02/2015

1.	Updated Figure 25-1 on page 45
2.	Updated the “Packaging information” on page 61. Replaced “44M1” on page 62 by a correct package.
3.	Updated tables Table 32-8 on page 70and Table 32-36 on page 89 with information on fixed voltage offset.
4.	Updated use of capitals in heading, table headings and figure titles.

35.3 8135Q – 09/2014

1.	Updated the “Ordering Information” on page 2. Added ordering information for ATxmega16D4/32D4/64D4/128D4 @ 105°C.
2.	Updated the Application table section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 13
3.	Updated Table 32-4 on page 66, Table 32-33 on page 86, Table 32-60 on page 104 and Table 32-89 on page 125. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
4.	Updated Table 32-17 on page 74, Table 32-45 on page 93, Table 32-73 on page 112 and Table 32-102 on page 133. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
5.	Changed Vcc to AVcc in Figure 25-1 on page 45 and in the text in Section 25. “ADC – 12-bit Analog to Digital Converter” on page 44 and in Section 26. “AC – Analog Comparator” on page 46
6.	Changed unit parameter for $t_{SU;DAT}$ to ns in Table 32-28 on page 82, Table 32-56 on page 101, Table 32-85 on page 121 and Table 32-114 on page 142.
7.	Added ERRATA information on disabling of USART transmitter to Section 34.1 “ATxmega16D4 / ATxmega32D4” on page 308.
8.	Updated the typical characteristics of “ATxmega64D4” and “ATxmega128D4” with characterizations @105°C

35.4 8135P – 01/2014

1.	Updated the typical characteristics of “ATxmega16D4” and “ATxmega32D4” with characterizations @ 105°C

35.9 8135K – 06/2012

1. ATxmega64D4-CU is added in “Ordering Information” on page 2

35.10 8135J – 12/10

1. Datasheet status changed to complete: Preliminary removed from the front page.
2. Updated all tables in the “Electrical Characteristics” on page 64.
3. Replaced Table 31-11 on page 64.
4. Replaced Table 31-17 on page 65 and added the figure ”TOSC input capacitance” on page 66.
5. Updated ERRATA ADC (ADC has increased INL for some operating conditions).
6. Updated ERRATA ”rev. A/B” on page 90 with TWIE (TWIE is not available).
7. Updated the last page with Atmel new Brand Style Guide.

35.11 8135I – 10/10

1. Updated Table 31-1 on page 58.

35.12 8135H – 09/10

1. Updated ”Errata” on page 90.

35.13 8135G – 08/10

1. Updated the Footnote 3 of ”Ordering Information” on page 2.
2. All references to CRC removed. Updated Figure 3-1 on page 7.
3. Updated ”Features” on page 26. Event Channel 0 output on port pin 7.
4. Updated ”DC Characteristics” on page 58 by adding Icc for Flash/EEPROM Programming.
5. Added AVCC in ”ADC Characteristics” on page 62.
6. Updated Start up time in ”ADC Characteristics” on page 62.
7. Updated and fixed typo in “Errata” section.

35.14 8135F – 02/10

1. Added ”PDI Speed” on page 89.