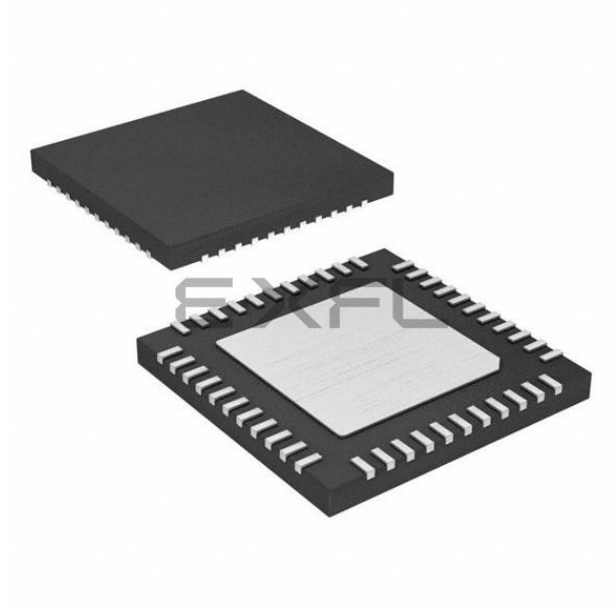

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16d4-mhr

Table 13-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x056	PORTE_INT_base	Port E Interrupt base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI on port D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base

28.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

28.1.7 Debug/System Functions

$\overline{\text{RESET}}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

28.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 28-1. Port A - Alternate Functions

PORT A	PIN#	INTERRUPT	ADCA POS/GAINPOS	ADCA NEG	ADCA GAINNEG	ACAPOS	ACANEG	ACAOUT	REFA
GND	38								
AVCC	39								
PA0	40	SYNC	ADC0	ADC0		AC0	AC0		AREF
PA1	41	SYNC	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	AC6			
PA7	3	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 28-2. Port B - Alternate Functions

PORT B	PIN#	INTERRUPT	ADCAPOS/GAINPOS	REFB
PB0	4	SYNC	ADC8	AREF
PB1	5	SYNC	ADC9	
PB2	6	SYNC/ASYNC	ADC10	
PB3	7	SYNC	ADC11	

29. Peripheral Module Address Map

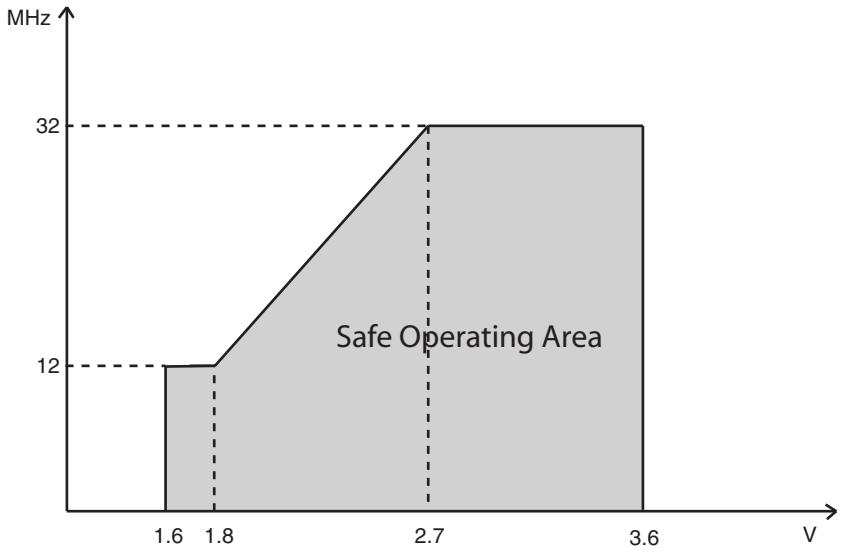
The address maps show the base address for each peripheral and module in Atmel AVR XMEGA D4. For complete register description and summary for each peripheral module, refer to the XMEGA D manual.

Table 29-1. Peripheral Module Address Map

Base address	Name	Description
0x0000	GPIO	General purpose IO registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock control
0x0048	SLEEP	Sleep controller
0x0050	OSC	Oscillator control
0x0060	DFLLRC32M	DFLL for the 32 MHz internal RC oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC oscillator
0x0070	PR	Power reduction
0x0078	RST	Reset controller
0x0080	WDT	Watch-dog timer
0x0090	MCU	MCU control
0x00A0	PMIC	Programmable multilevel interrupt controller
0x00B0	PORTCFG	Port configuration
0x0180	EVSYS	Event system
0x00D0	CRC	CRC module
0x01C0	NVM	Nonvolatile memory (NVM) controller
0x0200	ADCA	Analog to digital converter on port A
0x0380	ACA	Analog comparator pair on port A
0x0400	RTC	Real time counter
0x0480	TWIC	Two wire interface on port C
0x04A0	TWIE	Two wire interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-15 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-1. Maximum Frequency vs. V_{CC}



32.1.3 Current Consumption

Table 32-4. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		200		
			V_{CC} = 3.0V		410		
		2MHz, Ext. Clk	V_{CC} = 1.8V		350	600	
			V_{CC} = 3.0V		0.75	1.4	mA
		32MHz, Ext. Clk			7.5	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.0		µA
			V_{CC} = 3.0V		2.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		42		
			V_{CC} = 3.0V		85		
		2MHz, Ext. Clk	V_{CC} = 1.8V		85	225	
			V_{CC} = 3.0V		170	350	
		32MHz, Ext. Clk			2.7	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			2.0	4.5	
		T = 105°C			0.1	7.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.4	10	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.5		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance	XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		Ω
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				8.3		
C_{LOAD}	Parasitic capacitance load				3.5		

32.1.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-26. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: See Figure 32-4 for definition.

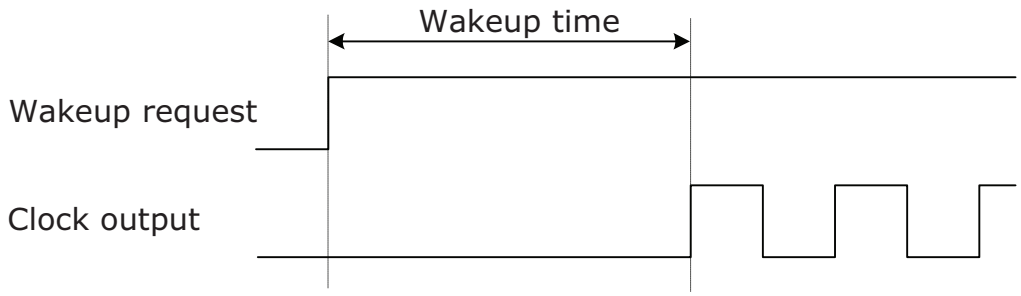
32.2.4 Wake-up Time from Sleep Modes

Table 32-34. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		5.0		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-9. Wake-up Time Definition



32.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 32-51. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency[1]	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.2.13.6External Clock Characteristics

Figure 32-10.External Clock Drive Waveform

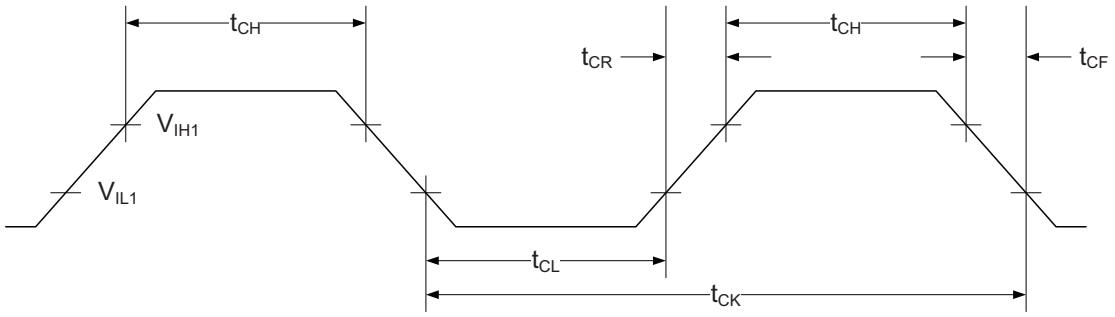


Table 32-52. External Clock[1]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency[2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7.0			
$t_{CH/CL}$	Clock high/low time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
$V_{IL/IH}$	Low/high level input voltage		See Table 32-7 on page 69			V
Δt_{CK}	Reduction in period time from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-67. Gain Stage Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1		Clk_{ADC} cycles
	Sample rate	Same as ADC		14		200	kHz
INL (1)	Integral non-linearity	50ksps	All gain settings		±1.5	±4	lsb
	Gain error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		
	Offset error, output referred	1x gain, normal mode			-2		mV
		8x gain, normal mode			-5		
		64x gain, normal mode			-4		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

32.3.7 Analog Comparator Characteristics

Table 32-68. Analog Comparator Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
V_{off}	Input offset voltage				<±10		mV
I_{lk}	Input leakage current				<1		nA
	Input voltage range			-0.1		AV_{CC}	V
	AC startup time				100		µs
V_{hys1}	Hysteresis, none				0		mV
V_{hys2}	Hysteresis, small				13		
V_{hys3}	Hysteresis, large				30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		30	90	ns
					30		
	64-Level voltage scaler	Integral non-linearity (INL)			0.3	0.5	lsb

Table 32-74. Programming Time

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
	Chip erase	64KB Flash, EEPROM[2] and SRAM erase		55		ms
	Flash	Page erase		4		
		Page write		4		
		Atomic Page Erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic Page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.3.13 Clock and Oscillator Characteristics

32.3.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 32-75. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.3.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 32-76. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.21		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = safety factor				$min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

32.4.15 Two-Wire Interface Characteristics

Table 32-114 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-28.

Figure 32-28.Two-wire Interface Bus Timing

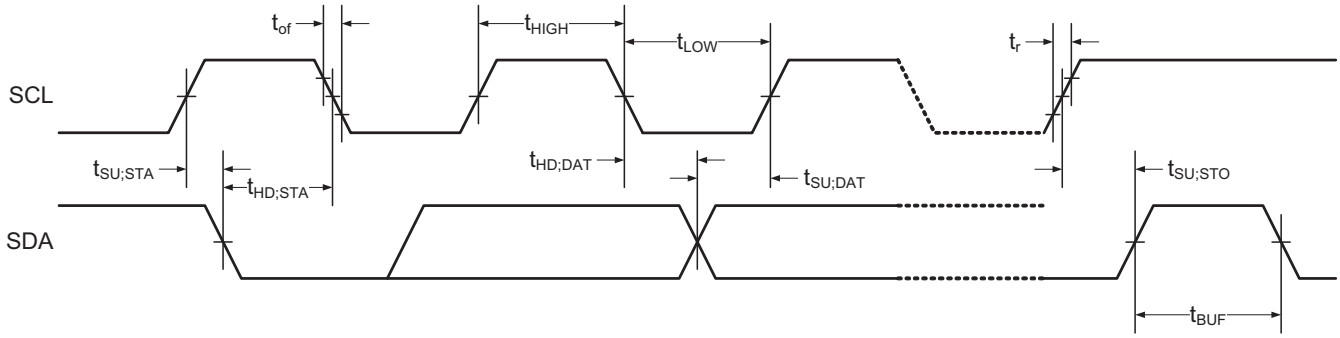


Table 32-114. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3*V_{CC}$	
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05*V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	

33.2.1.3 Power-down Mode Supply Current

Figure 33-94. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

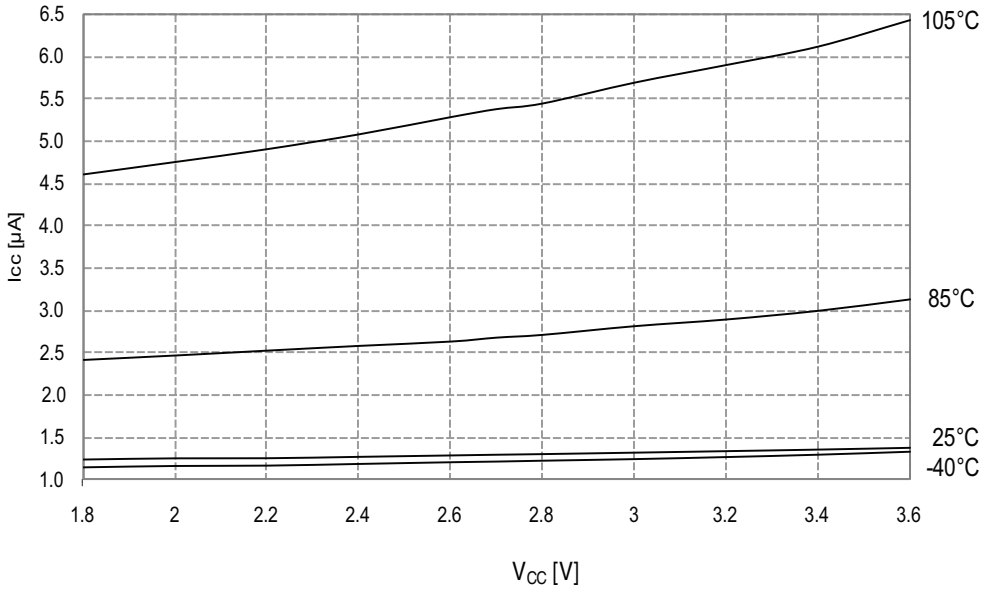


Figure 33-95. Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

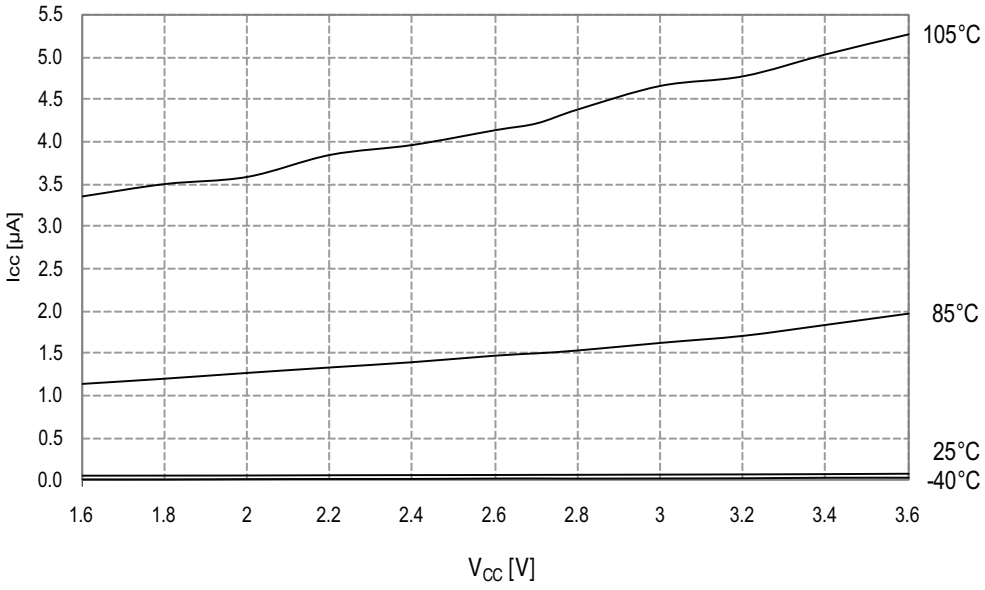
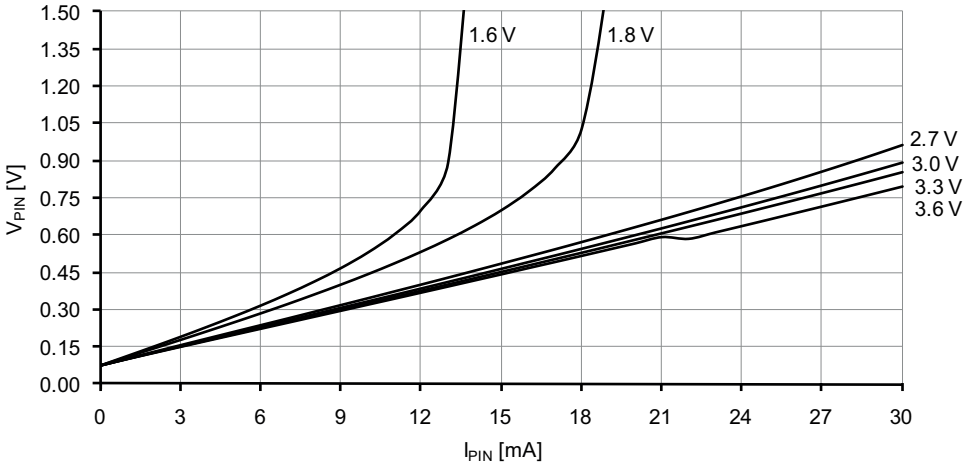


Figure 33-189. I/O Pin Output Voltage vs. Sink Current



33.3.2.3 Thresholds and Hysteresis

Figure 33-190. I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C

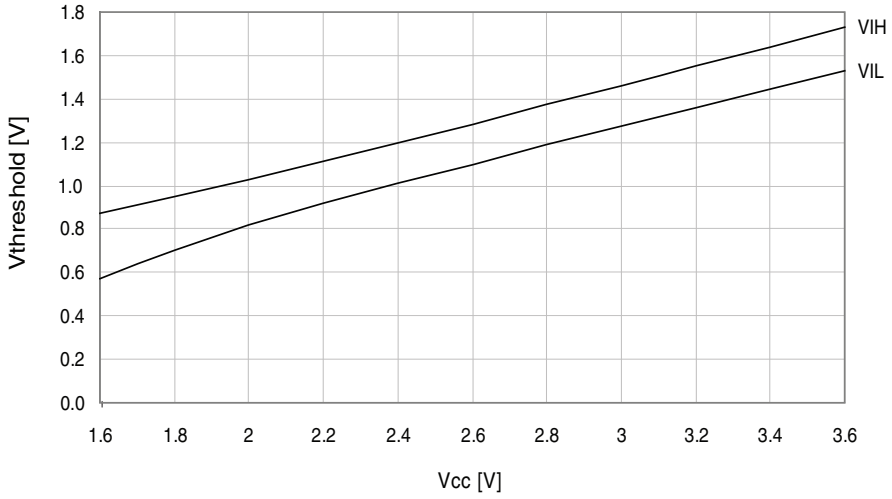


Figure 33-213. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis

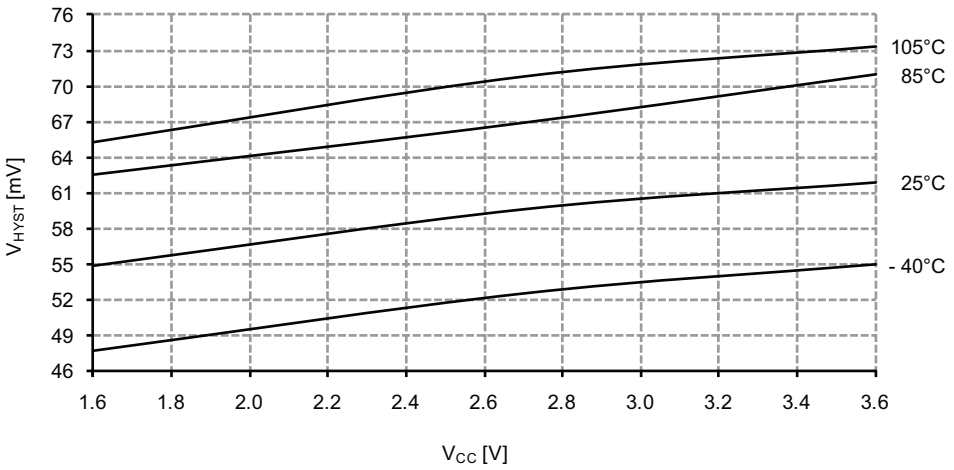


Figure 33-214. Analog Comparator Current Source vs. Calibration Value

Temperature = 25°C

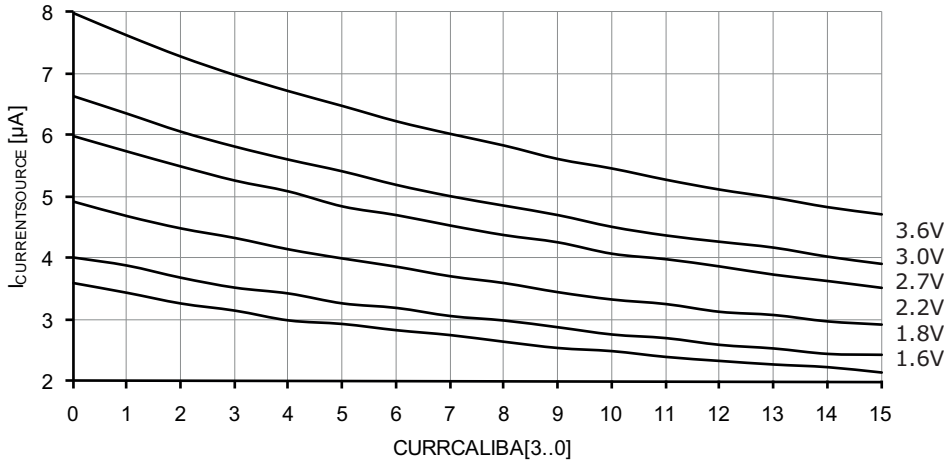
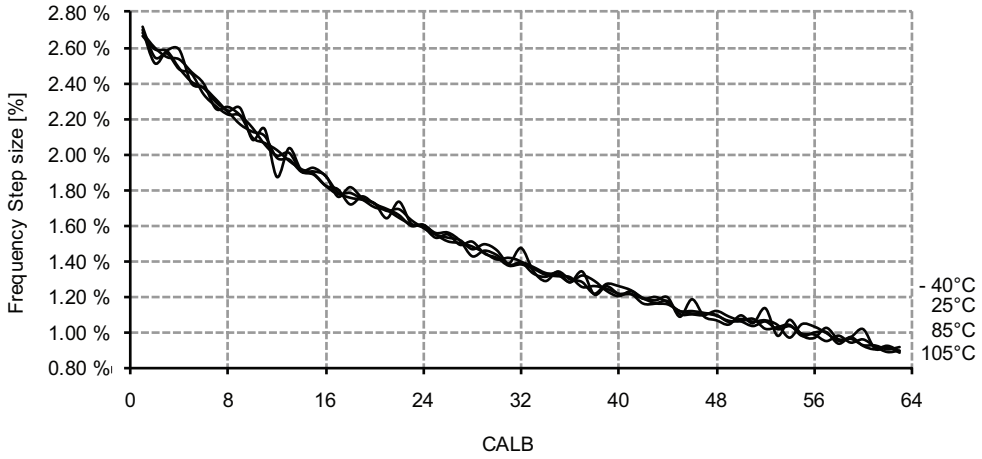


Figure 33-237. 32MHz Internal Oscillator CALB Calibration Step Size

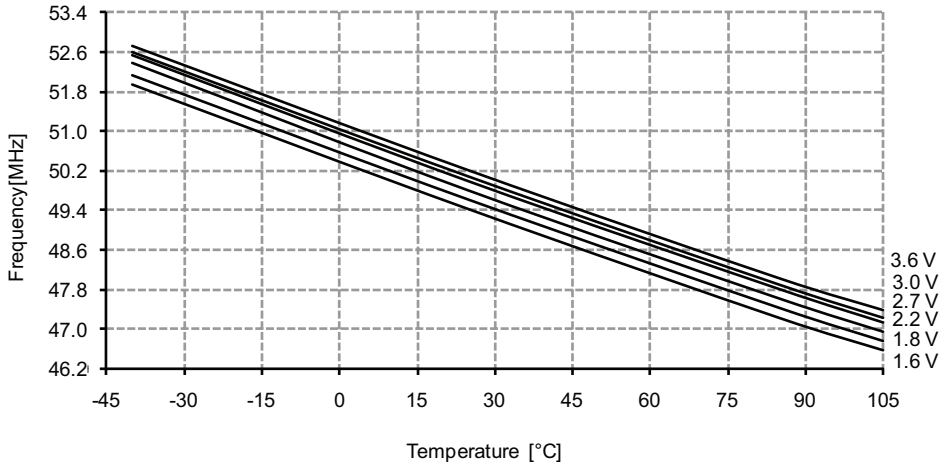
V_{CC} = 3.0V



33.3.10.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 33-238. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



33.4.1.3 Power-down Mode Supply Current

Figure 33-257. Power-down Mode Supply Current vs. Temperature

All functions disabled

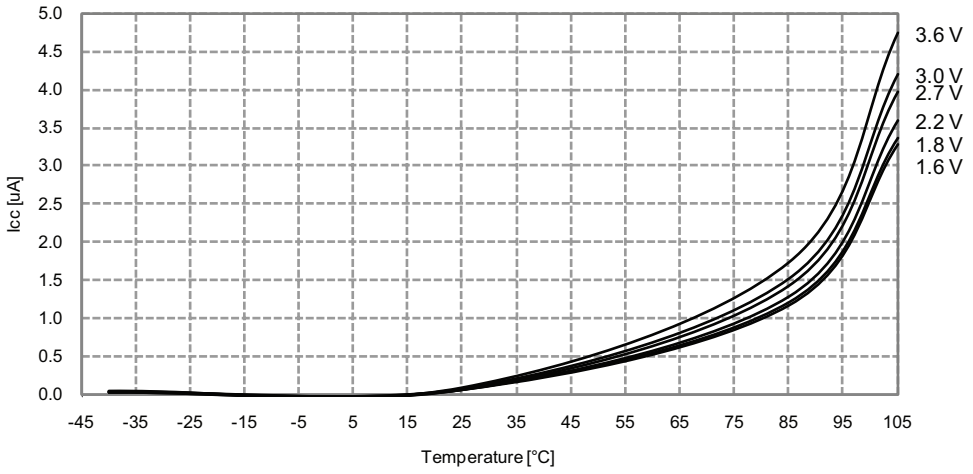


Figure 33-258. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

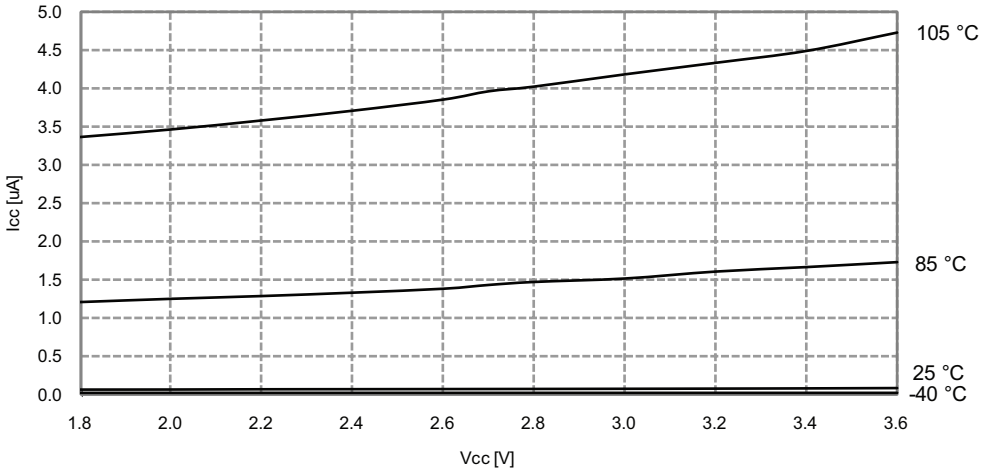
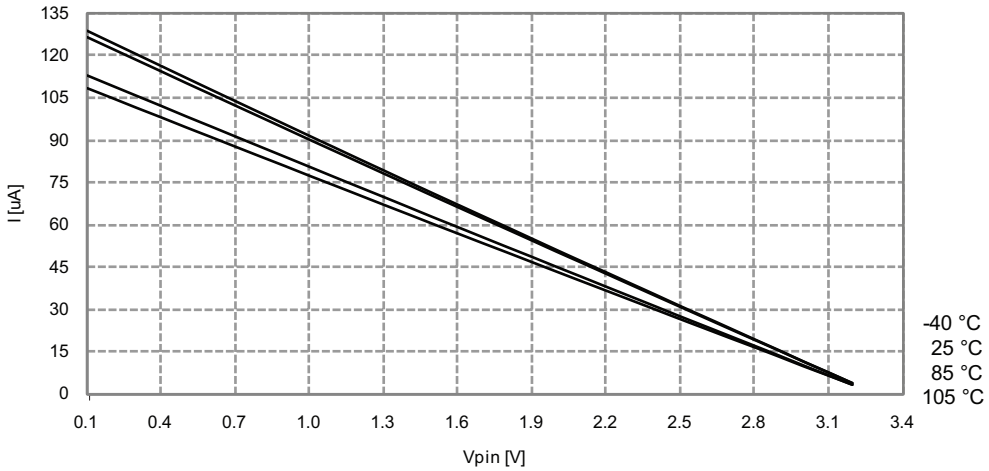


Figure 33-265. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



33.4.2.2 Output Voltage vs. Sink/Source Current

Figure 33-266. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V

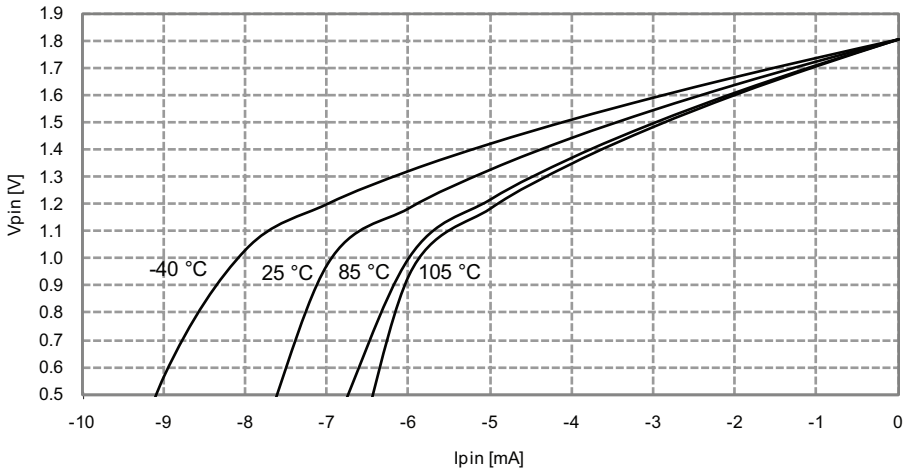
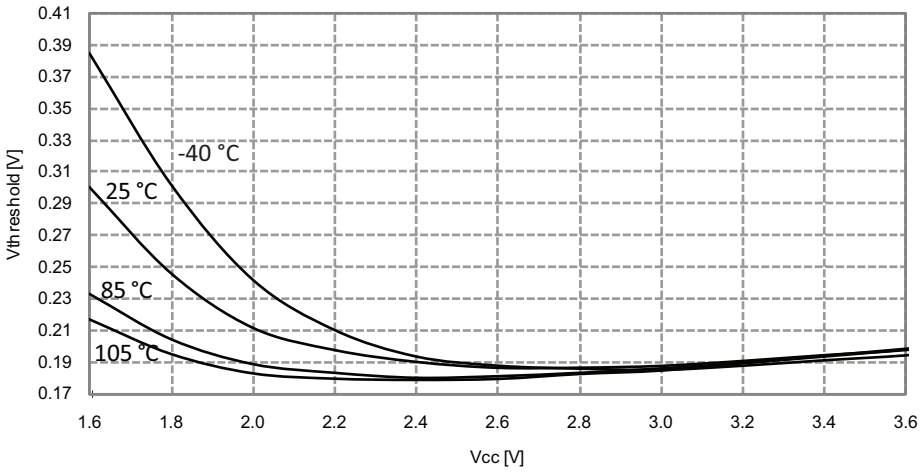


Figure 33-277. I/O Pin Input Hysteresis vs. V_{CC}



33.4.3 ADC Characteristics

Figure 33-278. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference