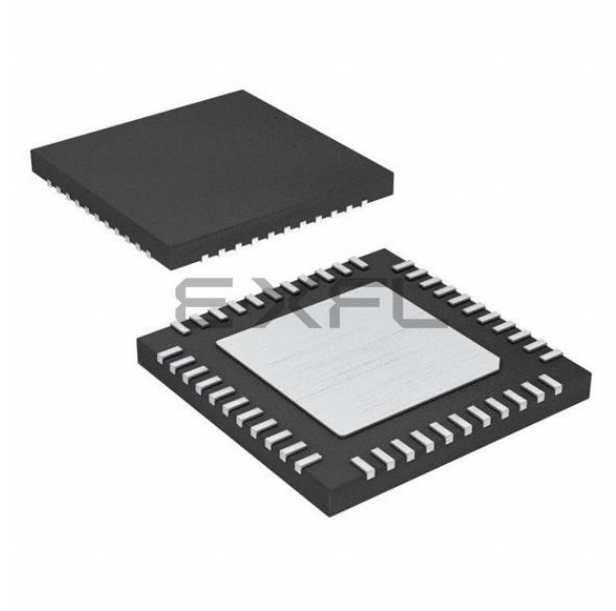

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16d4-mnr

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

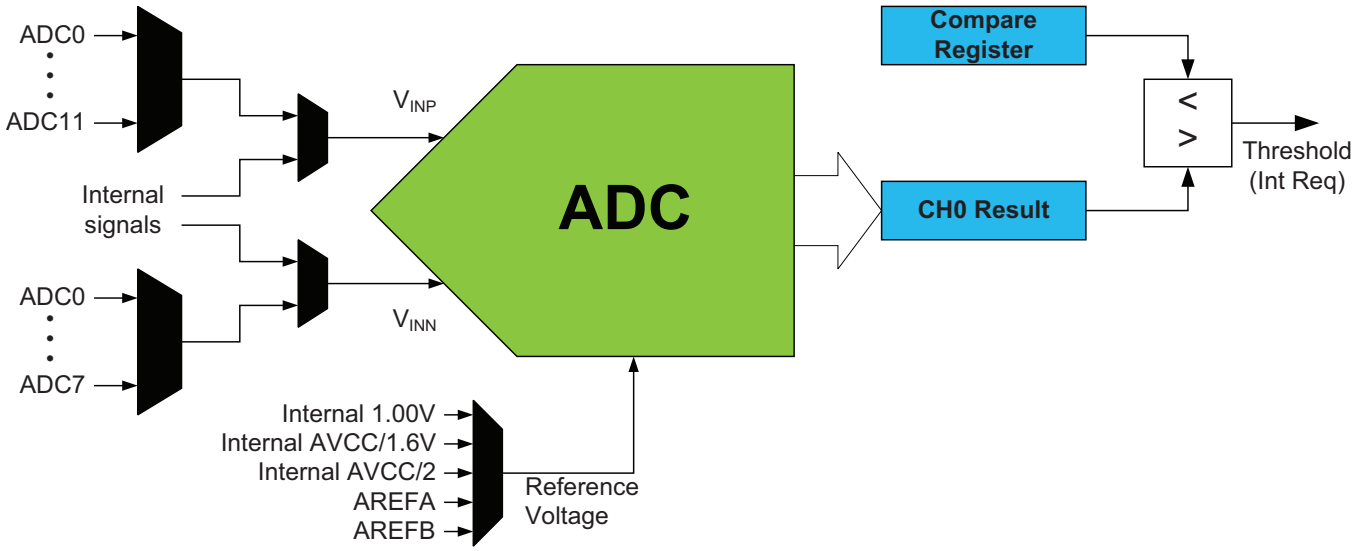
10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, and asynchronous port interrupts.

Figure 25-1. ADC overview



The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 5.0µs for 12-bit to 3.6µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

Notation of this peripheral is ADCA. The PORTA has ADCA inputs 0..7 and PORTB has ADCA inputs 8..11.

26. AC – Analog Comparator

26.1 Features

- Two Analog Comparators (ACs)
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

26.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

The important property of the analog comparator's dynamic behavior is the hysteresis. It can be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

32. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

32.1 ATxmega16D4

32.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 32-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 32-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-2. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-3. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

32.1.11 Power-on Reset Characteristics

Table 32-16. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.1.12 Flash and EEPROM Memory Characteristics

Table 32-17. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 32-18. Programming Time

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip erase(2)	16KB Flash, EEPROM		45		ms
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.

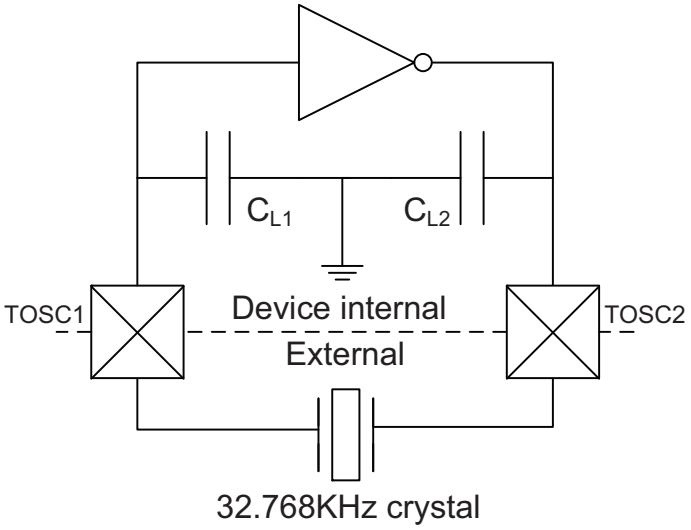
32.2.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-54. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: See Figure 32-11 for definition.

Figure 32-11.TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.3.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-63. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH}(1)/ I_{OL}(2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.7 - 3.6V		2		V_{CC}+0.3	V
		V_{CC} = 2.0 - 2.7V		0.7*V_{CC}		V_{CC}+0.3	
		V_{CC} = 1.6 - 2.0V		0.7*V_{CC}		V_{CC}+0.3	
V_{IL}	Low level input voltage	V_{CC} = 2.7- 3.6V		-0.3		0.3*V_{CC}	
		V_{CC} = 2.0 - 2.7V		-0.3		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.0V		-0.3		0.3*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.0 - 3.6V	I_{OH} = -2mA	2.4	0.94*V_{CC}		
		V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.0 - 3.6V	I_{OL} = 2mA		0.05*V_{CC}	0.4	
		V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current	T = 25°C			<0.001	0.1	µA
R_P	Pull/Buss keeper resistor				24		kΩ
t_r	Rise time	No load			4		ns

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC must not exceed 200mA.
   The sum of all I_{OH} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all I_{OH} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC must not exceed 200mA.
   The sum of all I_{OL} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all I_{OL} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

32.4 ATxmega128D4

32.4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 32-86 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-86. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.4.2 General Operating Ratings

The device must operate within the ratings listed in Table 32-87 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-87. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-88. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

32.4.6 ADC Characteristics

Table 32-93. Power Supply, Reference and Input Range

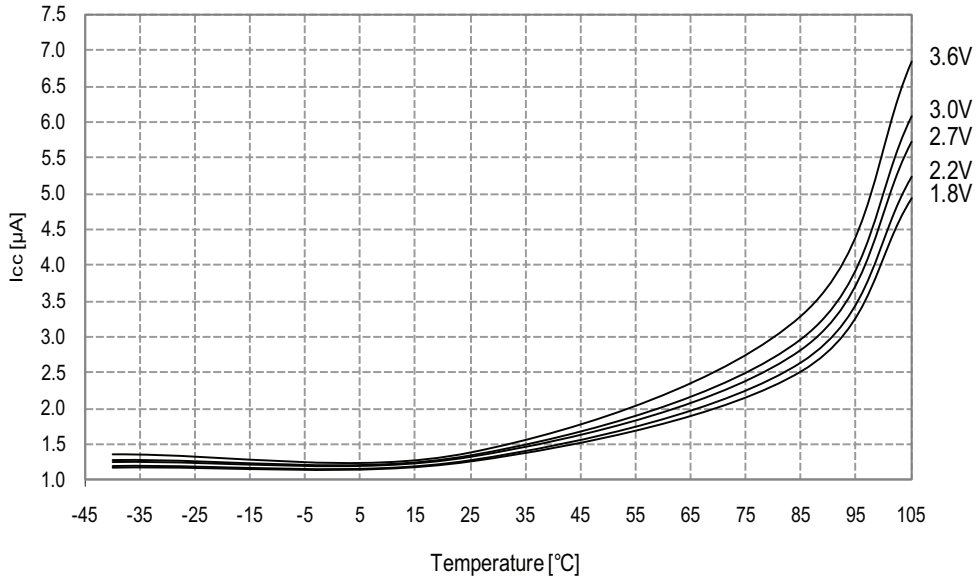
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			190		lsb

Table 32-94. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		1400	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	14		200	ksps
		CURRLIMIT = LOW	14		150	
		CURRLIMIT = MEDIUM	14		100	
		CURRLIMIT = HIGH			50	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0, 1, 2 or 3	5	7	10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	
		After ADC flush		1	1	

Figure 33-17. Power-down Mode Supply Current vs. Temperature

Watchdog and sampled BOD enabled and running from internal ULP oscillator



33.1.1.4 Power-save Mode Supply Current

Figure 33-18. Power-save Mode Supply Current vs.V_{CC}

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC

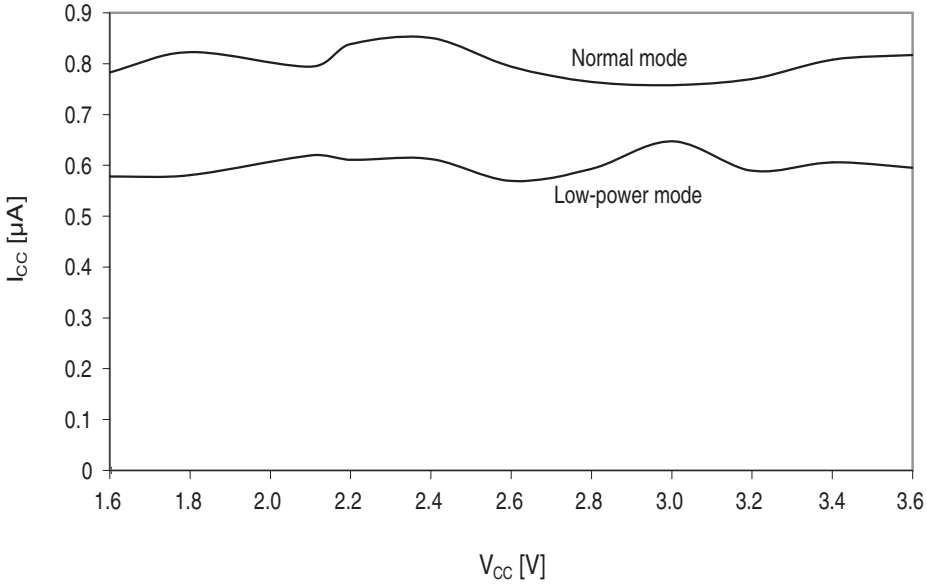


Figure 33-25. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

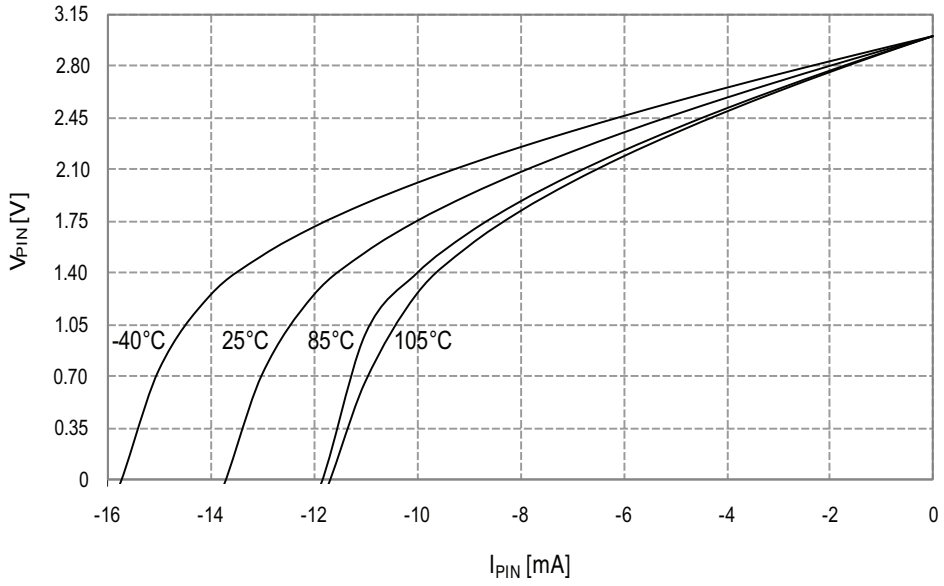


Figure 33-26. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

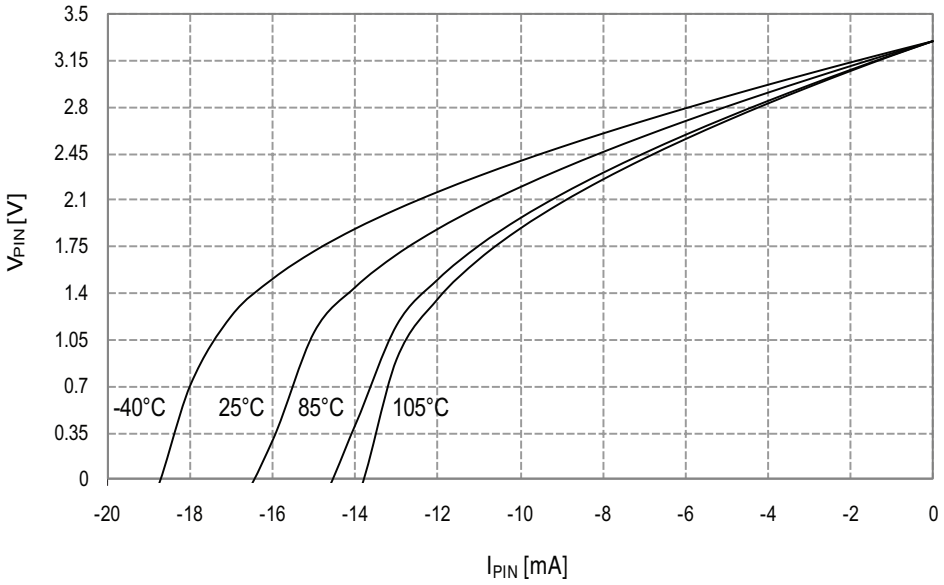
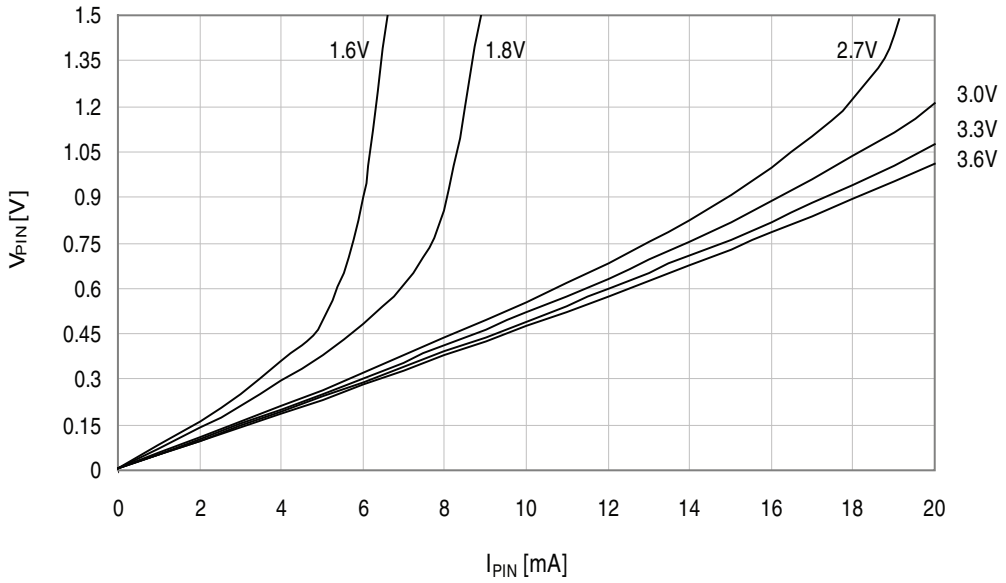


Figure 33-31. I/O Pin Output Voltage vs. Sink Current



33.1.2.3 Thresholds and Hysteresis

Figure 33-32. I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C

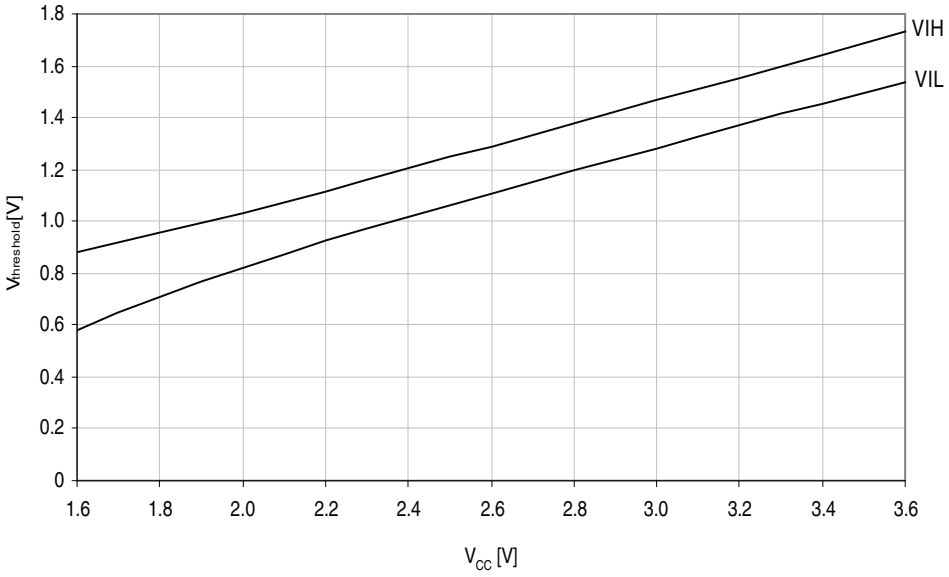
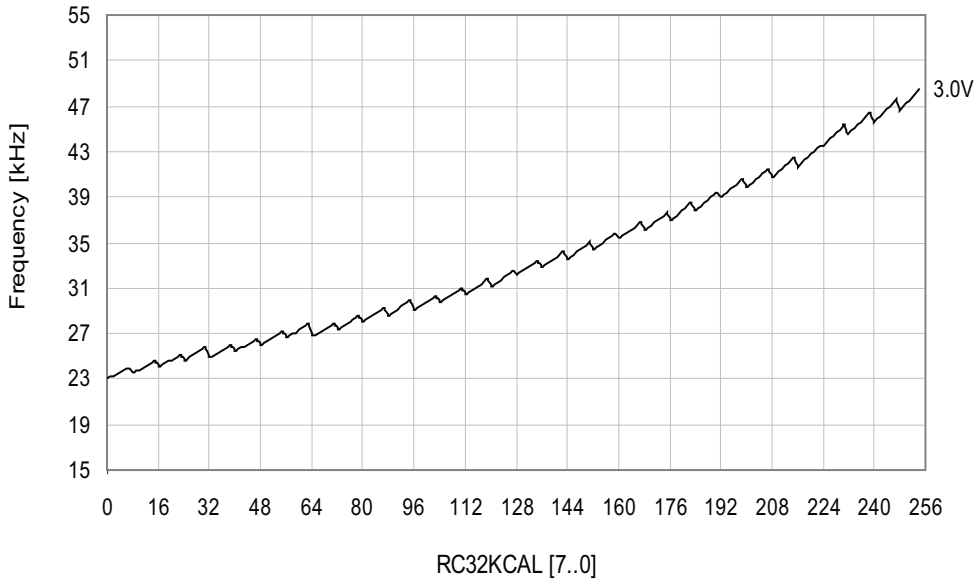


Figure 33-146. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

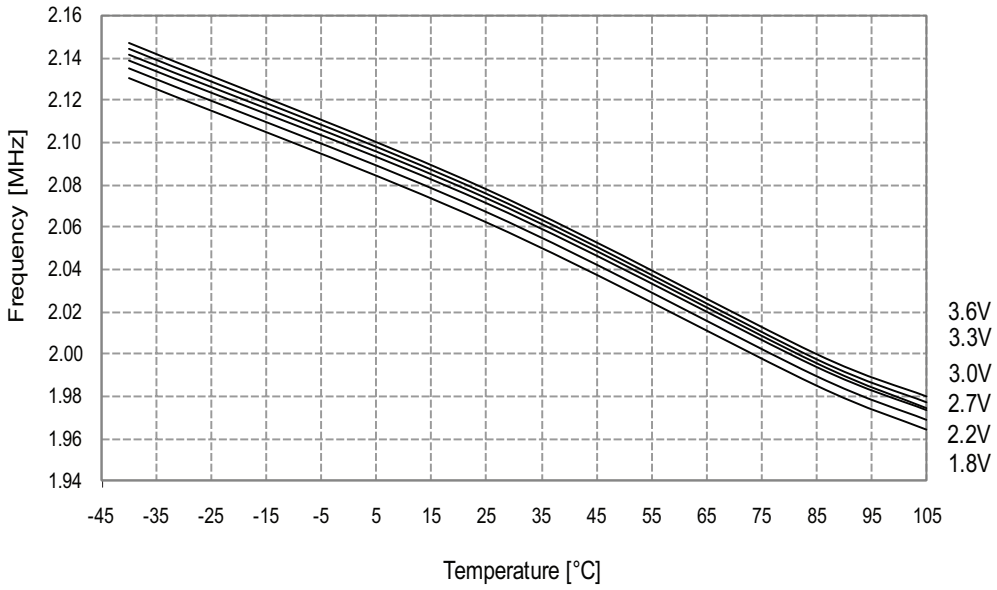
V_{CC} = 3.0V, T = 25°C



33.2.9.3 2MHz Internal Oscillator

Figure 33-147. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



33.3 ATxmega64D4

33.3.1 Current Consumption

33.3.1.1 Active Mode Supply Current

Figure 33-159. Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

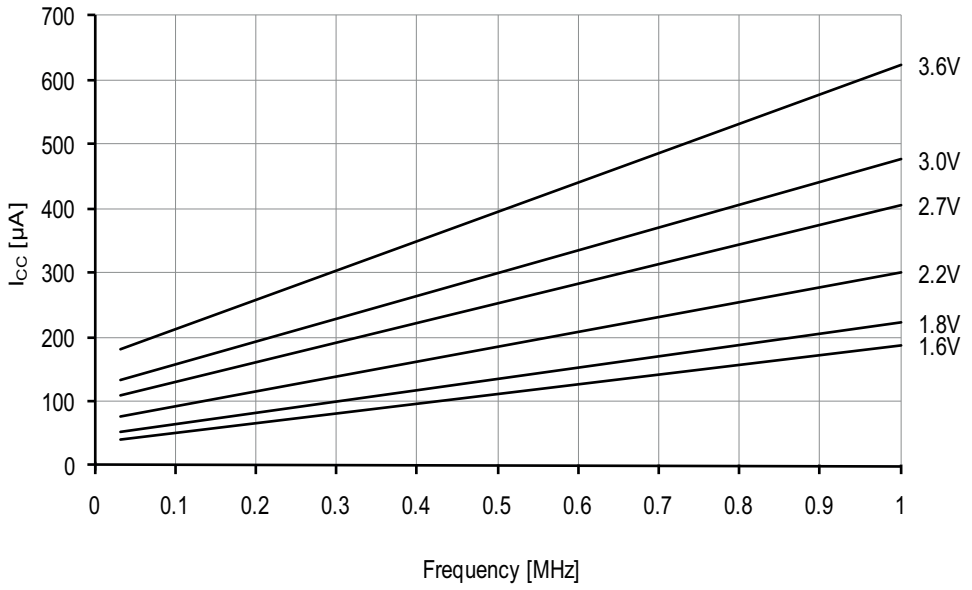
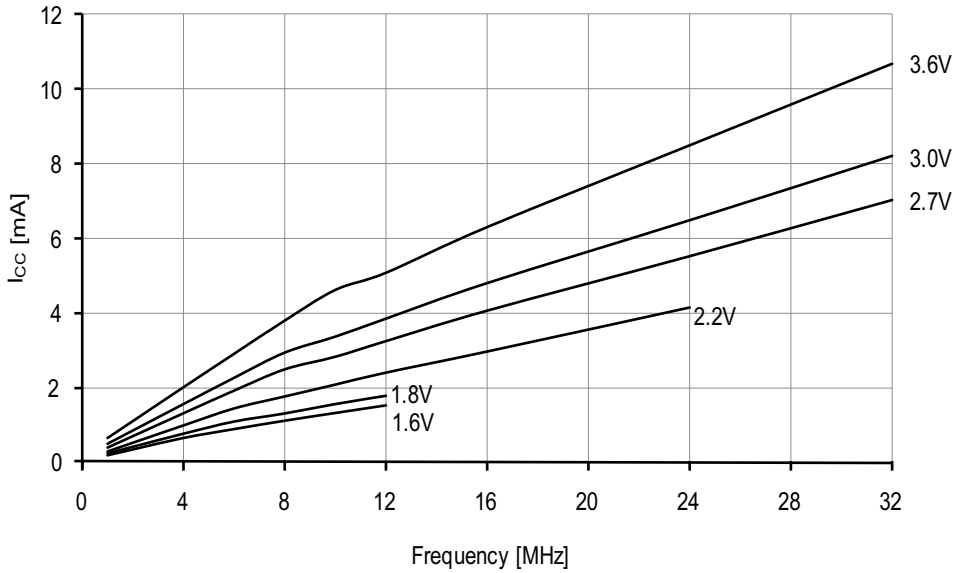


Figure 33-160. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C



33.4 ATxmega128D4

33.4.1 Current Consumption

33.4.1.1 Active Mode Supply Current

Figure 33-243. Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

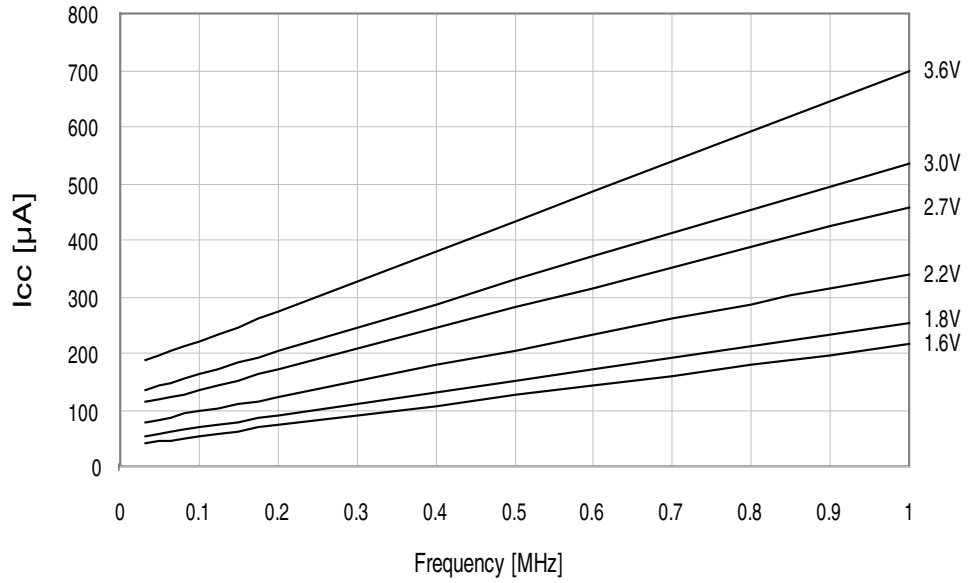
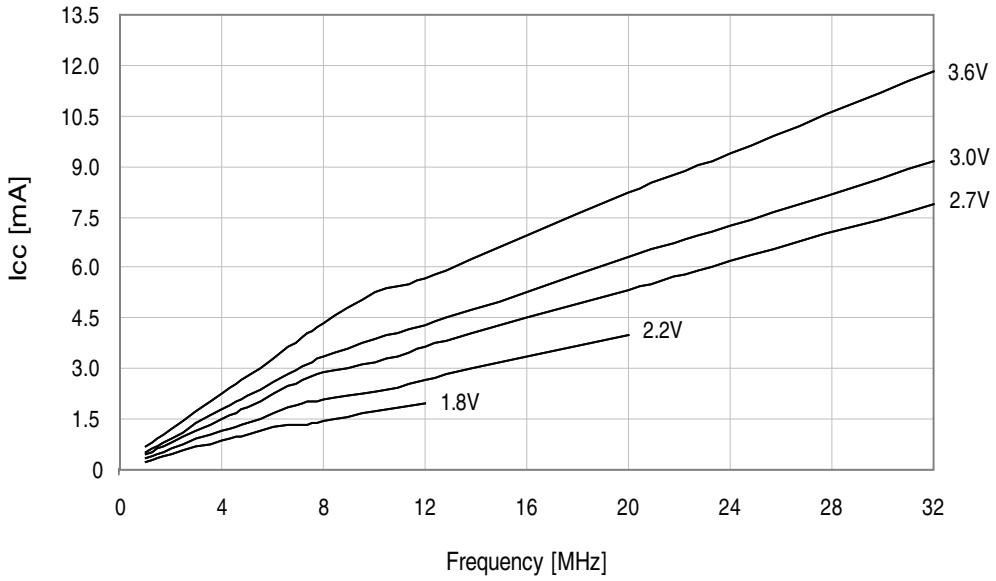


Figure 33-244. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C



33.4.2 I/O Pin Characteristics

33.4.2.1 Pull-up

Figure 33-263. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *1.8V*

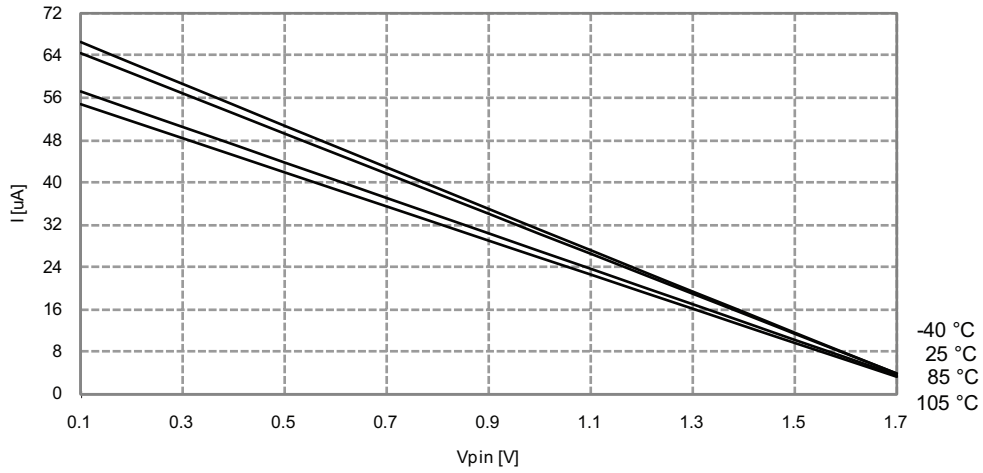


Figure 33-264. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *3.0V*

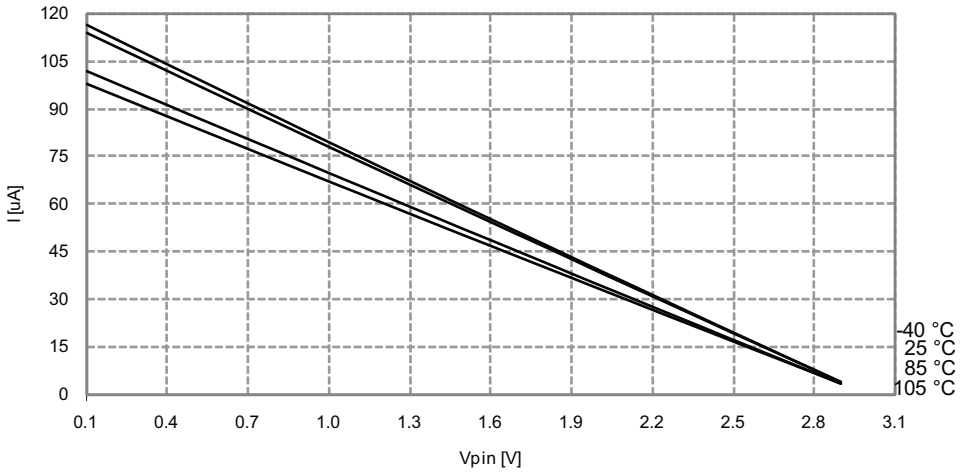
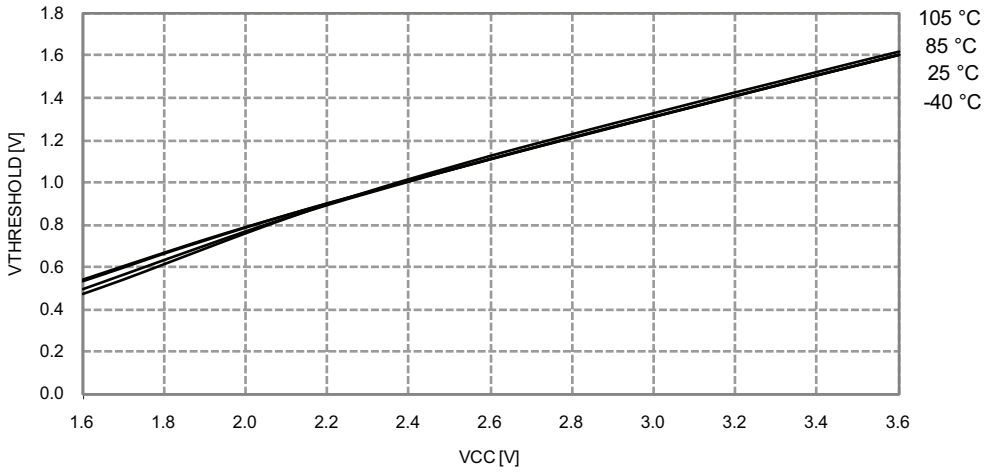


Figure 33-309. Reset Pin Input Threshold Voltage vs. V_{CC}

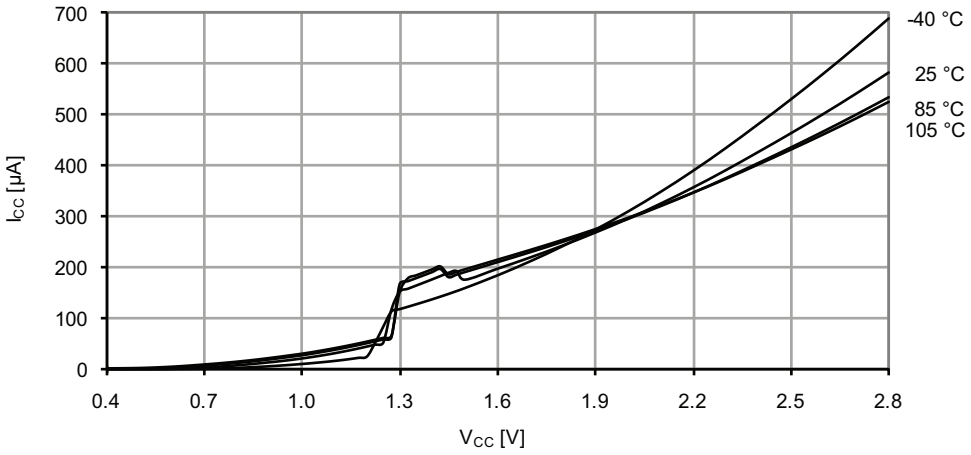
V_{IL} - Reset pin read as "0"



33.4.9 Power-on Reset Characteristics

Figure 33-310. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode



1x gain:	2.4V
2x gain:	1.2V
4x gain:	0.6v
8x gain:	300mV
16x gain:	150mV
32x gain:	75mV
64x gain:	38mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

5. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. **ADC propagation delay is not correct when 8x -64x gain is used**

The propagation delay will increase by only one ADC clock cycle for 8x and 16x gain setting, and 32x and 64x gain settings.

Problem fix/Workaround

None.

7. **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

8. **Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

9. **Configuration of PGM and CWCM not as described in XMEGA A Manual**

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

35. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

35.1 8135S – 09/2016

1.	Updated “Instruction Set Summary” on page 56. Removed “DES” instruction.
2.	Updated “Gain Stage Characteristics” : Table 32-11 on page 72, Table 32-39 on page 91Table 32-67 on page 110 and Table 32-96 on page 131. “Offset Error, input referred” is changed to “Offset Error, output referred.

35.2 8135R – 02/2015

1.	Updated Figure 25-1 on page 45
2.	Updated the “Packaging information” on page 61. Replaced “44M1” on page 62 by a correct package.
3.	Updated tables Table 32-8 on page 70and Table 32-36 on page 89 with information on fixed voltage offset.
4.	Updated use of capitals in heading, table headings and figure titles.

35.3 8135Q – 09/2014

1.	Updated the “Ordering Information” on page 2. Added ordering information for ATxmega16D4/32D4/64D4/128D4 @ 105°C.
2.	Updated the Application table section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 13
3.	Updated Table 32-4 on page 66, Table 32-33 on page 86, Table 32-60 on page 104 and Table 32-89 on page 125. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
4.	Updated Table 32-17 on page 74, Table 32-45 on page 93, Table 32-73 on page 112 and Table 32-102 on page 133. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
5.	Changed Vcc to AVcc in Figure 25-1 on page 45 and in the text in Section 25. “ADC – 12-bit Analog to Digital Converter” on page 44 and in Section 26. “AC – Analog Comparator” on page 46
6.	Changed unit parameter for $t_{SU;DAT}$ to ns in Table 32-28 on page 82, Table 32-56 on page 101, Table 32-85 on page 121 and Table 32-114 on page 142.
7.	Added ERRATA information on disabling of USART transmitter to Section 34.1 “ATxmega16D4 / ATxmega32D4” on page 308.
8.	Updated the typical characteristics of “ATxmega64D4” and “ATxmega128D4” with characterizations @105°C

35.4 8135P – 01/2014

1.	Updated the typical characteristics of “ATxmega16D4” and “ATxmega32D4” with characterizations @ 105°C