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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d4-an

Table 7-3. Number of Bytes and Pages in the EEPROM

Devices	EEPROM	Page Size	E2BYTE	E2PAGE	No of Pages
	Size	bytes			
ATxmega16D4	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega32D4	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega64D4	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128D4	2K	32	ADDR[4:0]	ADDR[10:5]	64

29. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA D4. For complete register description and summary for each peripheral module, refer to the XMEGA D manual.

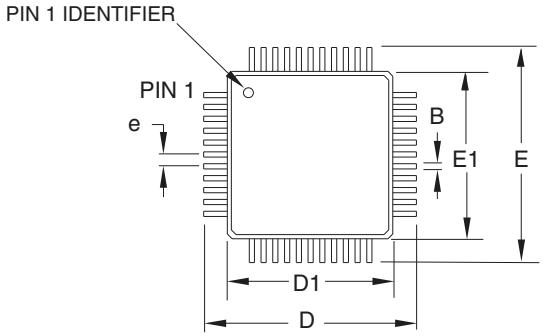
Table 29-1. Peripheral Module Address Map

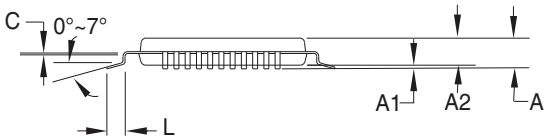
Base address	Name	Description
0x0000	GPIO	General purpose IO registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock control
0x0048	SLEEP	Sleep controller
0x0050	OSC	Oscillator control
0x0060	DFLLRC32M	DFLL for the 32 MHz internal RC oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC oscillator
0x0070	PR	Power reduction
0x0078	RST	Reset controller
0x0080	WDT	Watch-dog timer
0x0090	MCU	MCU control
0x00A0	PMIC	Programmable multilevel interrupt controller
0x00B0	PORTCFG	Port configuration
0x0180	EVSYS	Event system
0x00D0	CRC	CRC module
0x01C0	NVM	Nonvolatile memory (NVM) controller
0x0200	ADCA	Analog to digital converter on port A
0x0380	ACA	Analog comparator pair on port A
0x0400	RTC	Real time counter
0x0480	TWIC	Two wire interface on port C
0x04A0	TWIE	Two wire interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3[(1)]
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3[(1)]
CALL	k	call Subroutine	PC ← k	None	3 / 4[(1)]
RET		Subroutine Return	PC ← STACK	None	4 / 5[(1)]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[(1)]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1

31. Packaging information

31.1 44A





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	0.37	0.45	
C	0.09	(0.17)	0.20	
L	0.45	0.60	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

06/02/2014

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)	44A	C

Table 32-11. Gain Stage Characteristics

R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC}- 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain Error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		10		
	Offset Error, output referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-150		

32.1.7 Analog Comparator Characteristics

Table 32-12. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage	V_{CC}=1.6V - 3.6V		<±10		mV
I_{lk}	Input leakage current	V_{CC}=1.6V - 3.6V		<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none	V_{CC}=1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC}=1.6V - 3.6V		11		
V_{hys3}	Hysteresis, large	V_{CC}=1.6V - 3.6V		26		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		16	90	ns
		V_{CC}=1.6V - 3.6V		16		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

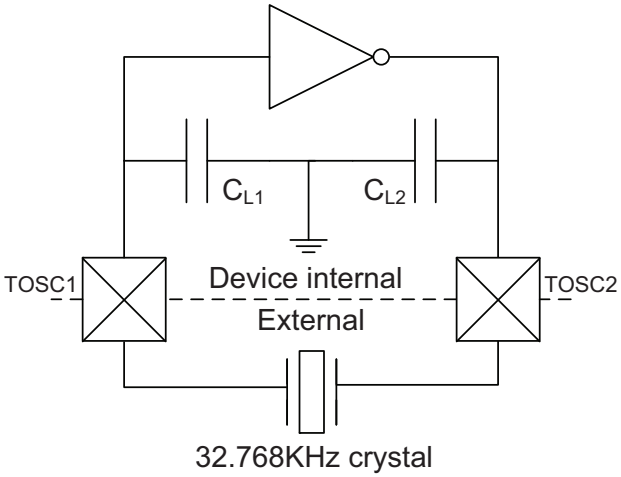
32.3.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-83. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC}	Parasitic capacitance	Normal mode		4.7		pF
		Low power mode		5.2		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: 1. See Figure 32-18 on page 118 for definition.

Figure 32-18.TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		30	90	ns
					30		
	64-Level voltage scaler	Integral non-linearity (INL)			0.3	0.5	lsb

32.4.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-98. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

32.4.9 Brownout Detection Characteristics

Table 32-99. Brownout Detection Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

33.1.1.5 Standby Mode Supply Current

Figure 33-19. Standby Supply Current vs. V_{CC}

Standby, f_{SYS} = 1MHz

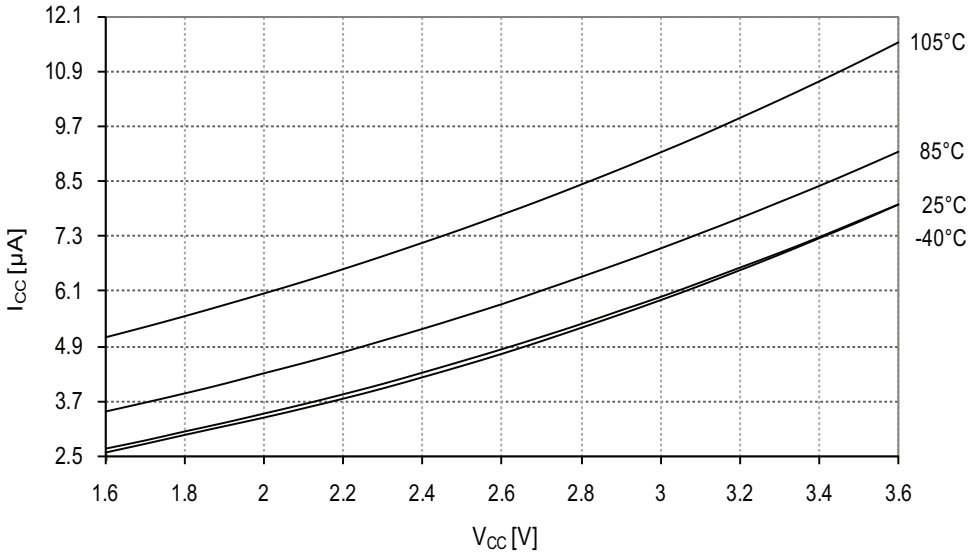


Figure 33-20. Standby Supply Current vs. V_{CC}

25°C, running from different crystal oscillators

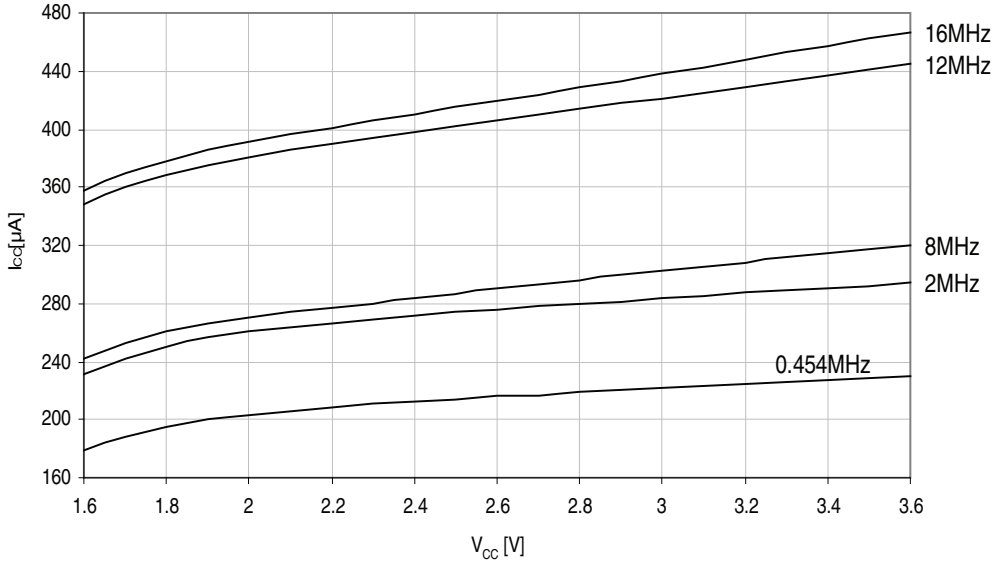


Figure 33-59. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.0V

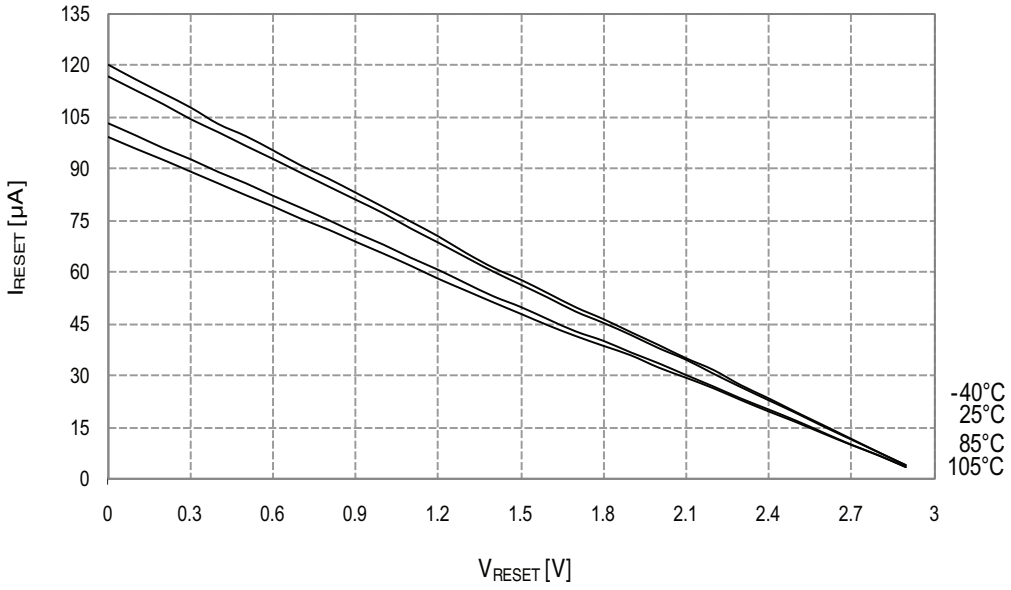
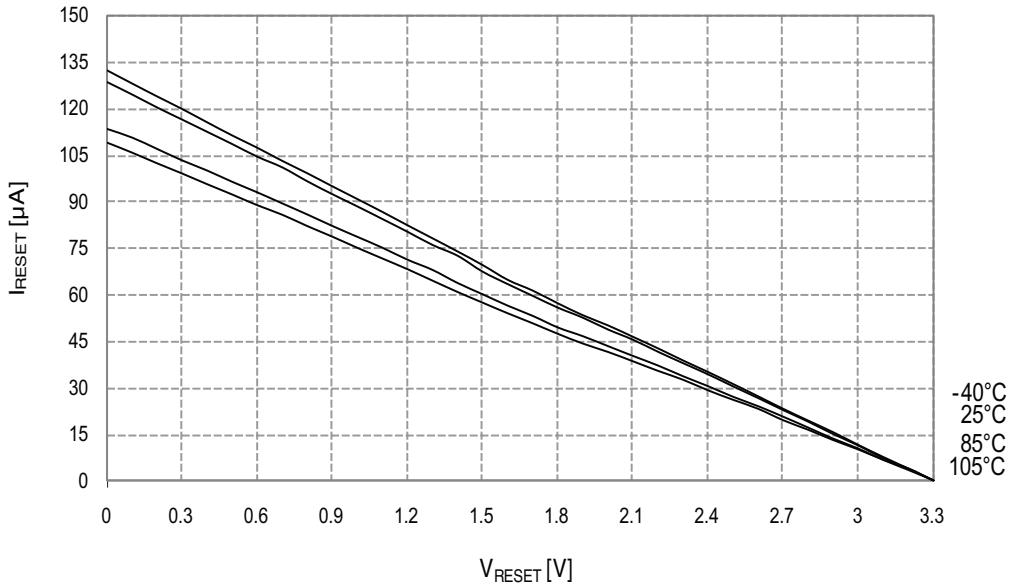


Figure 33-60. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V



33.1.8 Power-on Reset Characteristics

Figure 33-63. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode

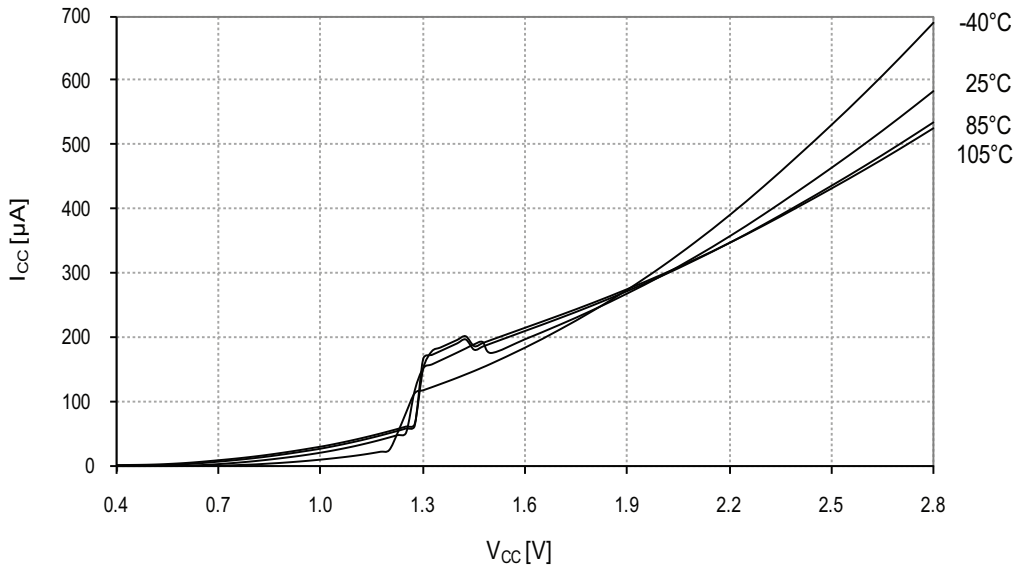


Figure 33-64. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in sampled mode

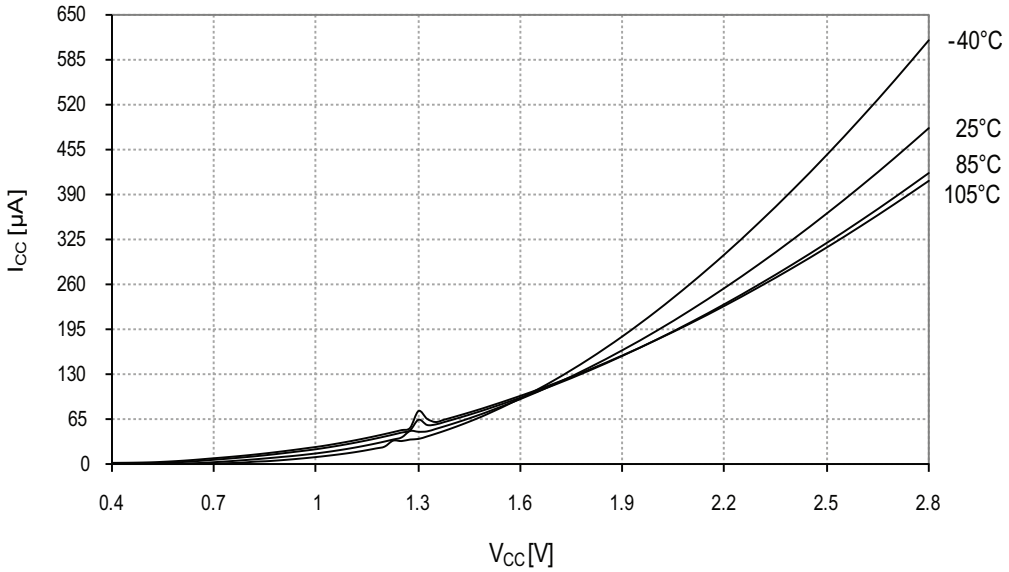
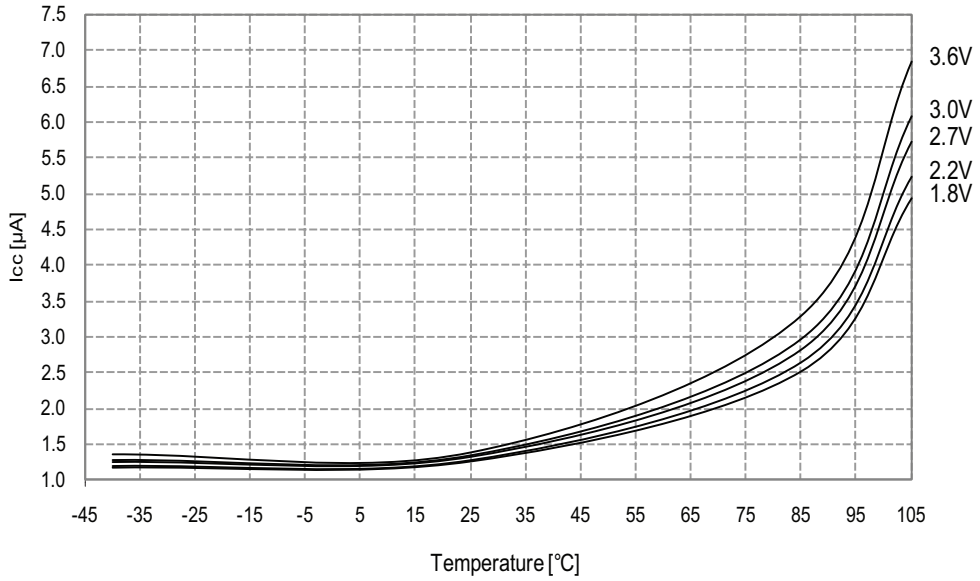


Figure 33-96. Power-down Mode Supply Current vs. Temperature

Watchdog and sampled BOD enabled and running from internal ULP oscillator



33.2.1.4 Power-save Mode Supply Current

Figure 33-97. Power-save Mode Supply Current vs.V_{CC}

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC

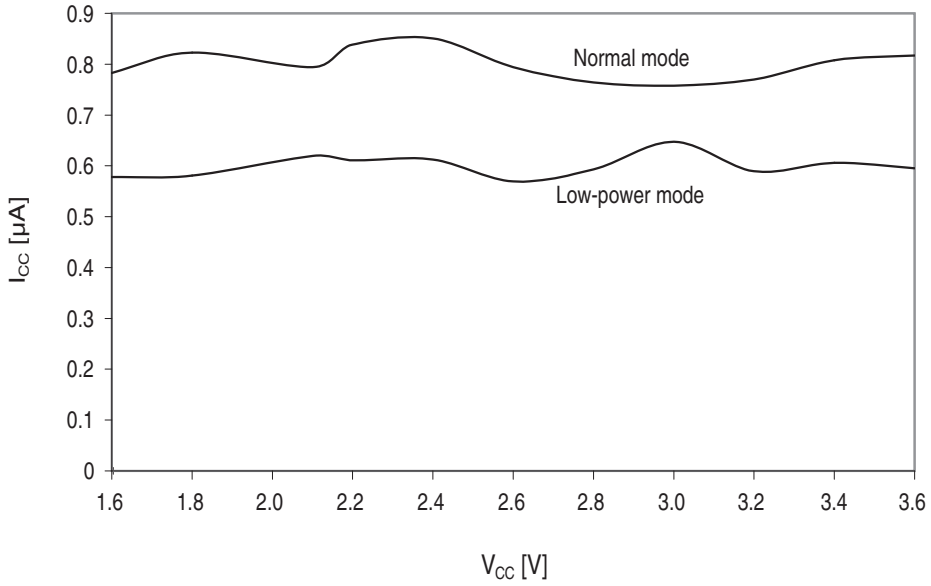
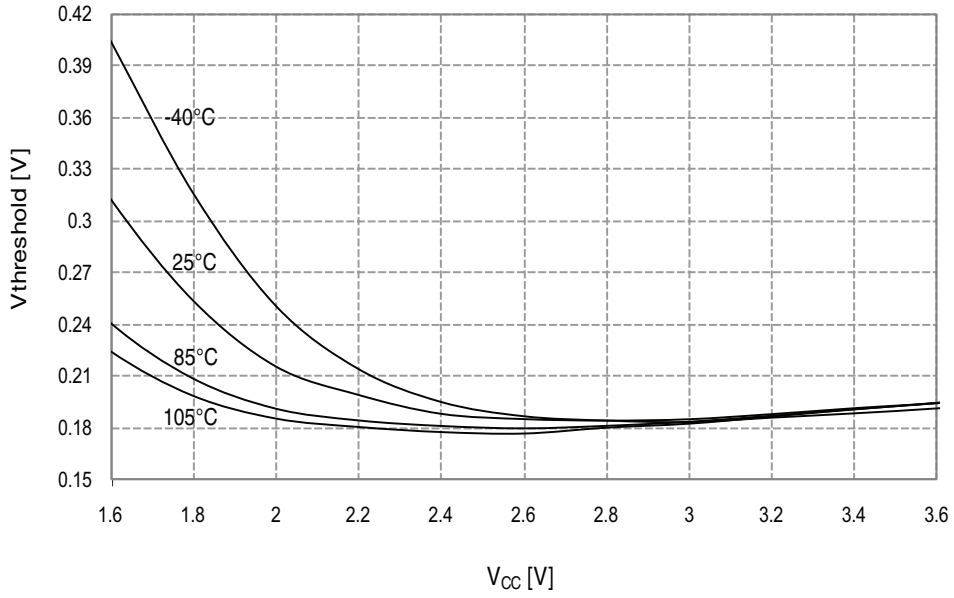


Figure 33-114. I/O Pin Input Hysteresis vs. V_{CC}



33.2.3 ADC Characteristics

Figure 33-115. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

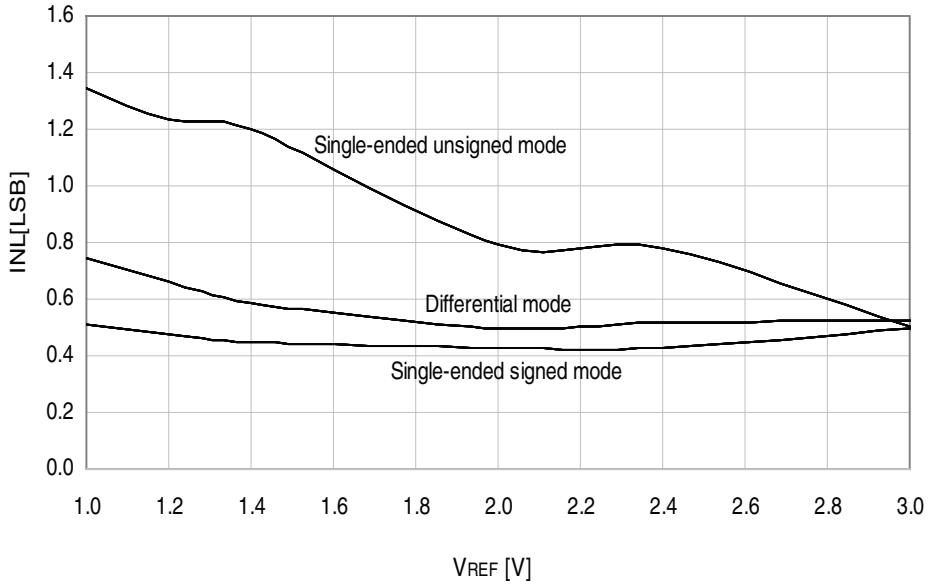


Figure 33-128. Analog Comparator Hysteresis vs. V_{CC}

Low power, small hysteresis

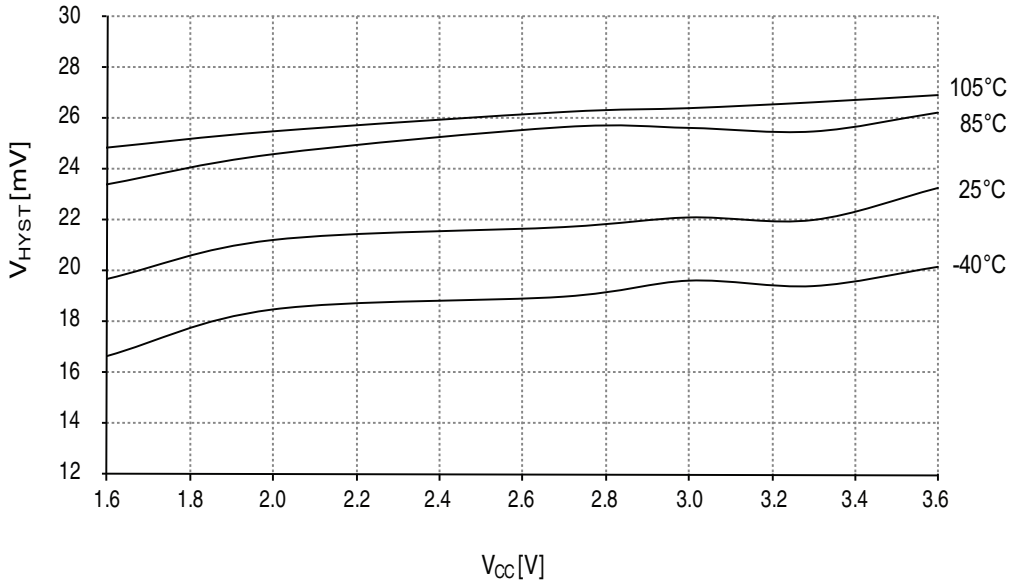


Figure 33-129. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis

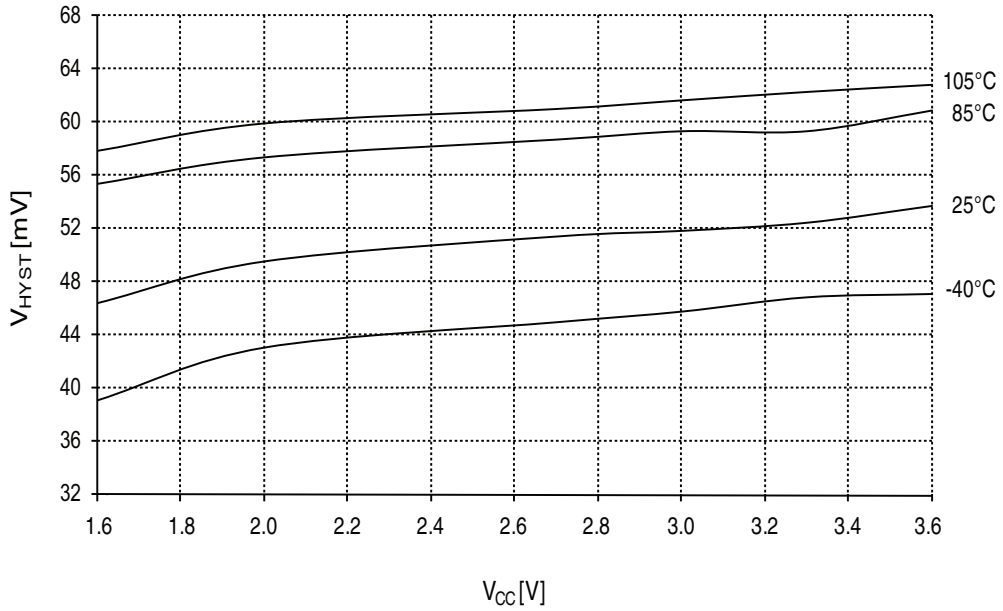


Figure 33-130. Analog Comparator Current Source vs. Calibration Value

T = 25°C

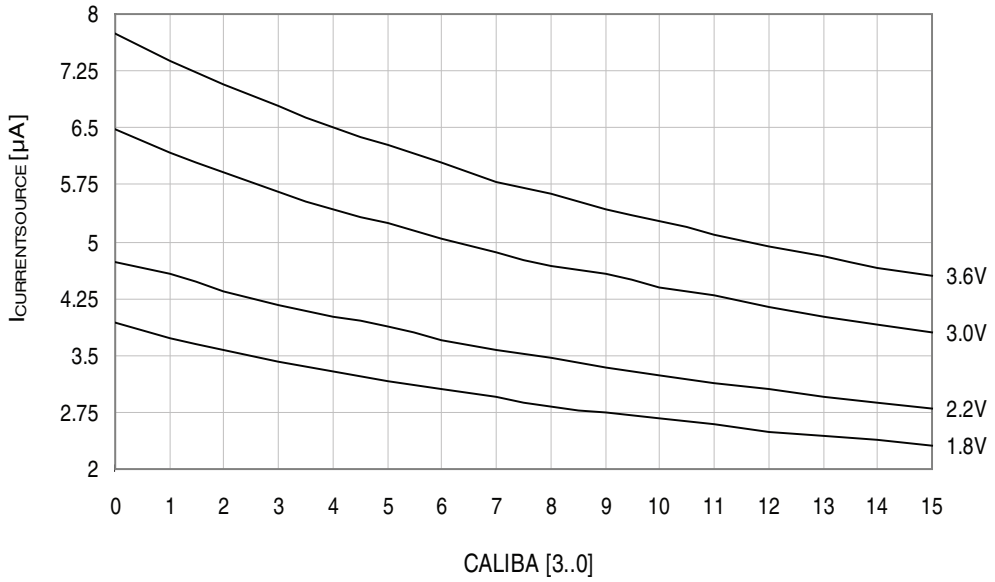
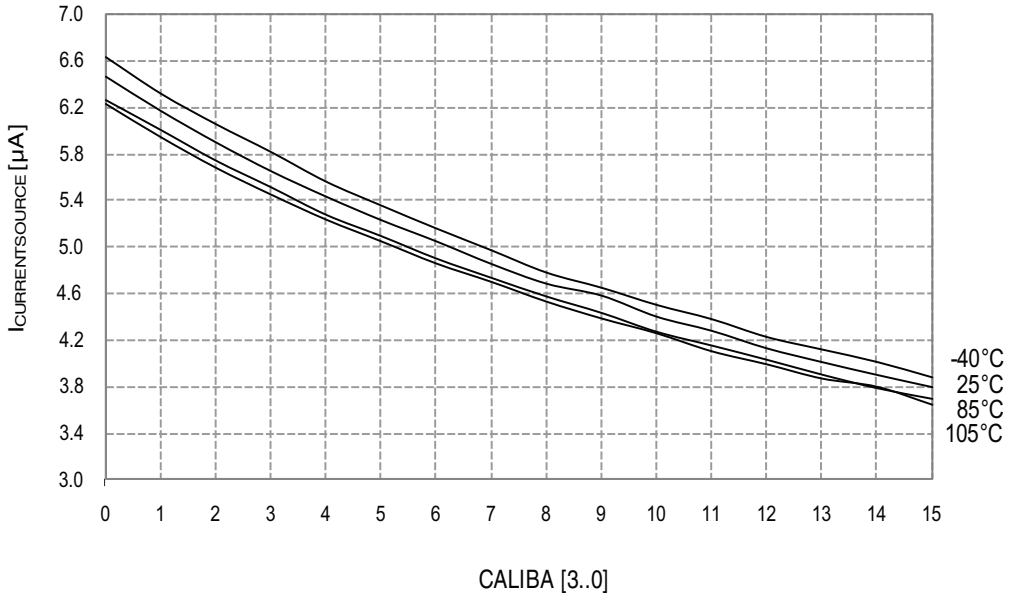


Figure 33-131. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V



33.4.1.3 Power-down Mode Supply Current

Figure 33-257. Power-down Mode Supply Current vs. Temperature

All functions disabled

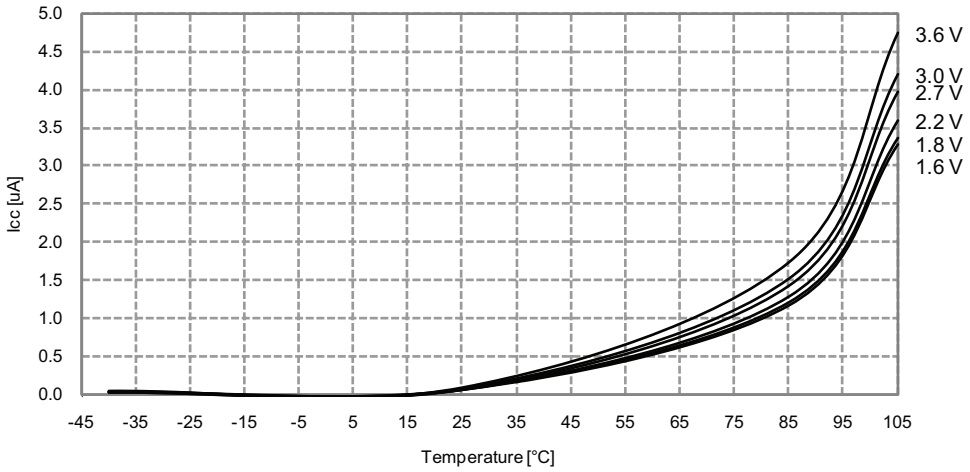


Figure 33-258. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

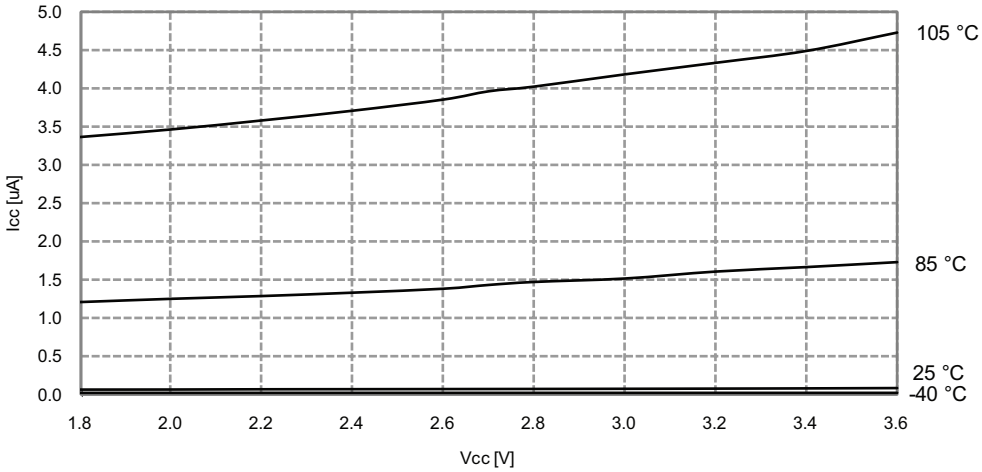


Figure 33-271. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

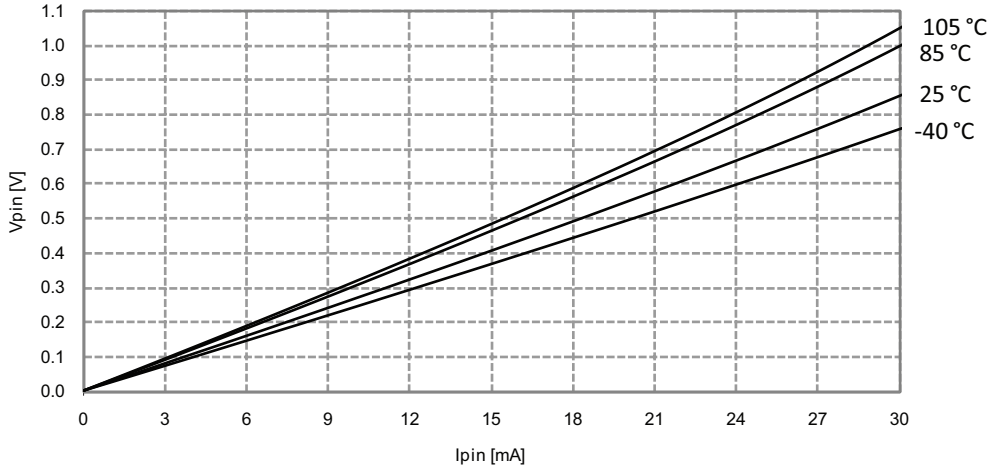


Figure 33-272. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

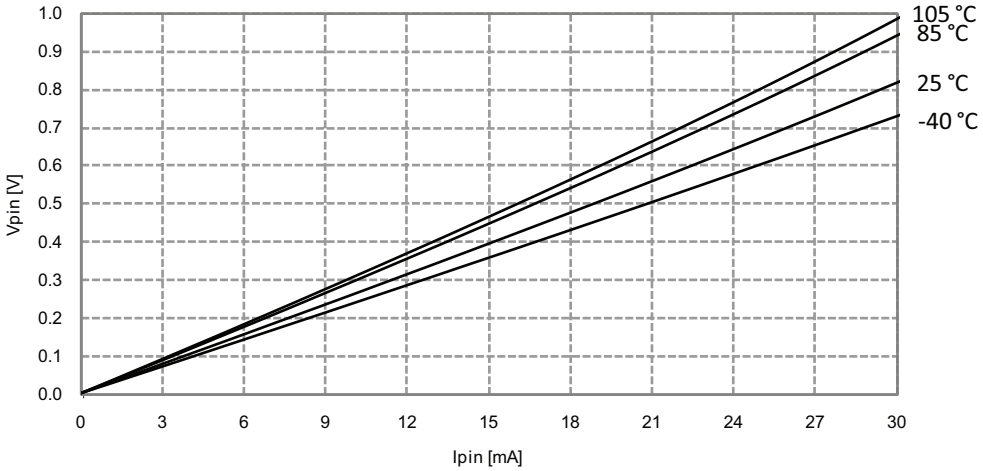
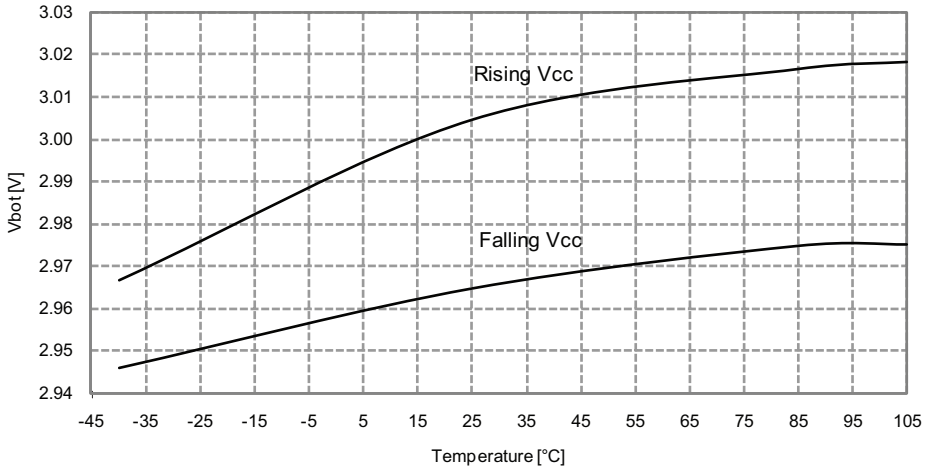


Figure 33-303. BOD Thresholds vs. Temperature

BOD level = 3.0V



33.4.8 External Reset Characteristics

Figure 33-304. Minimum Reset Pin Pulse Width vs. V_{CC}

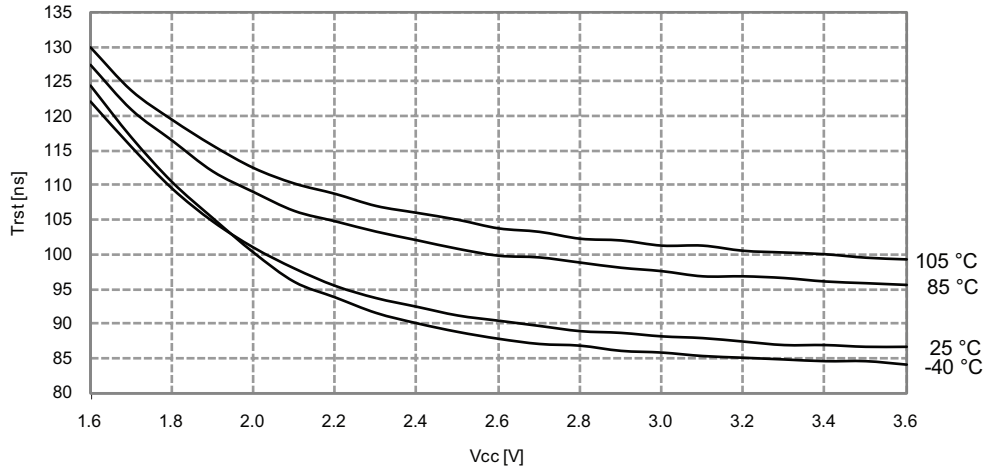
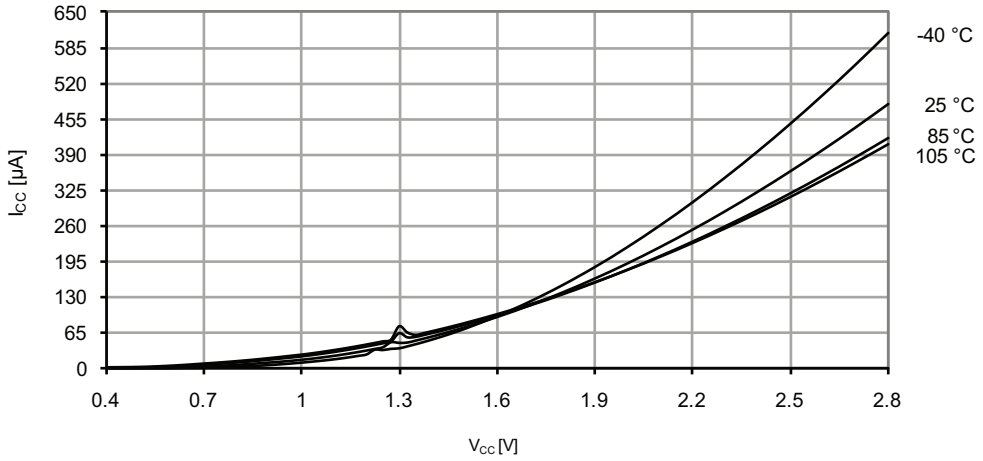


Figure 33-311. Power-on Reset Current Consumption vs. V_{CC}

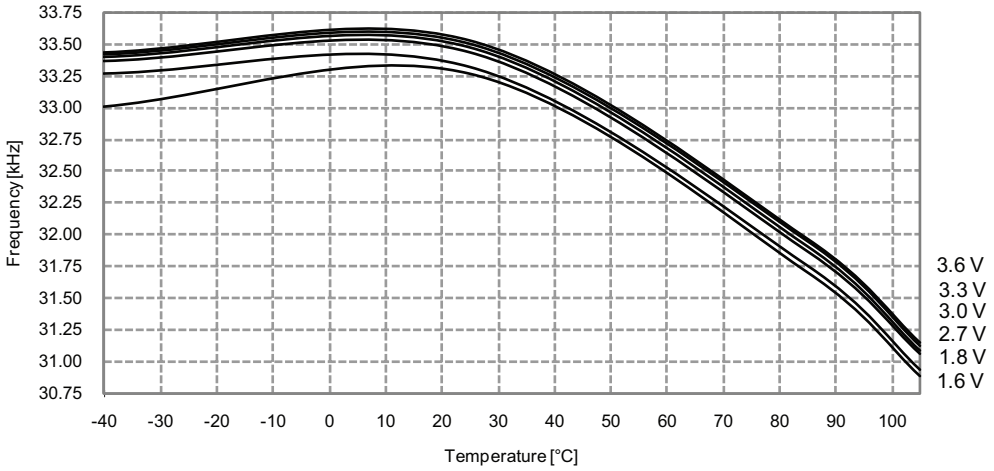
BOD level = 3.0V, enabled in sampled mode



33.4.10 Oscillator Characteristics

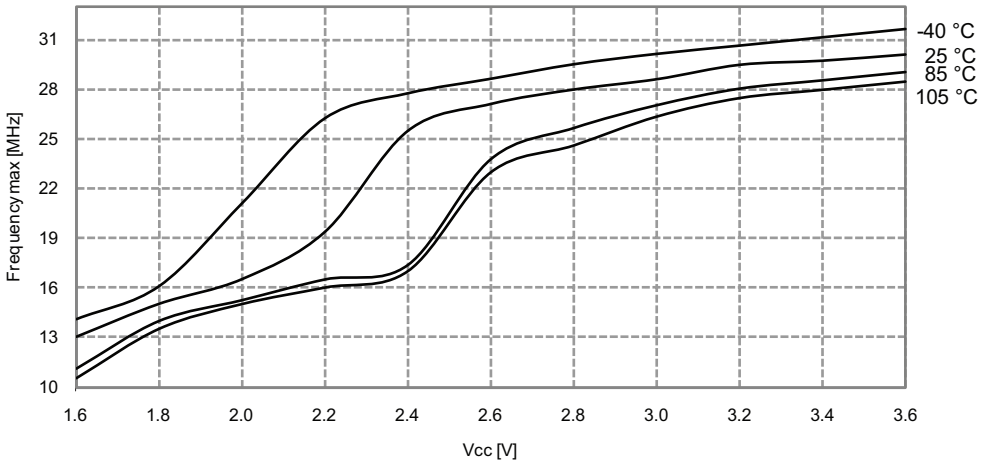
33.4.10.1 Ultra Low-Power Internal Oscillator

Figure 33-312. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



33.4.12 PDI Characteristics

Figure 33-325. Maximum PDI Frequency vs. V_{CC}



Problem fix/Workaround

Table 34-1. Configure PWM and CWCM According to this Table

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

10 PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

11. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

12. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC and Analog Comparator.

Problem fix/Workaround

If the bandgap is used as reference for either the ADC or the Analog Comparator, the BOD must not be set in sampled mode.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.