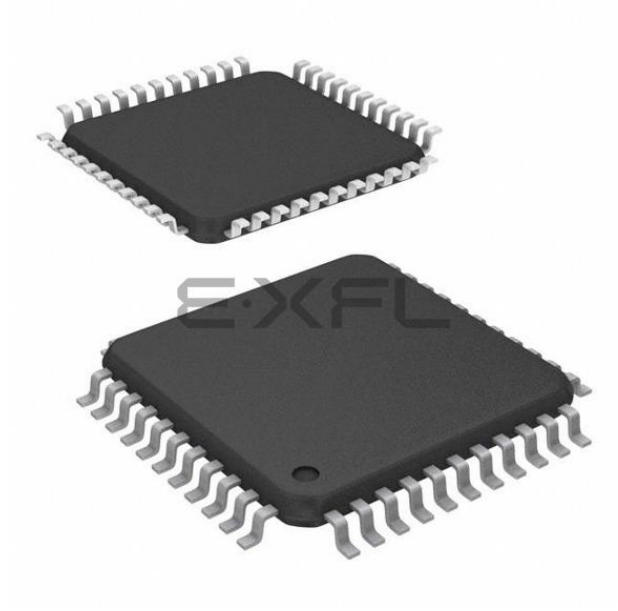

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What is "Embedded - Microcontrollers"?

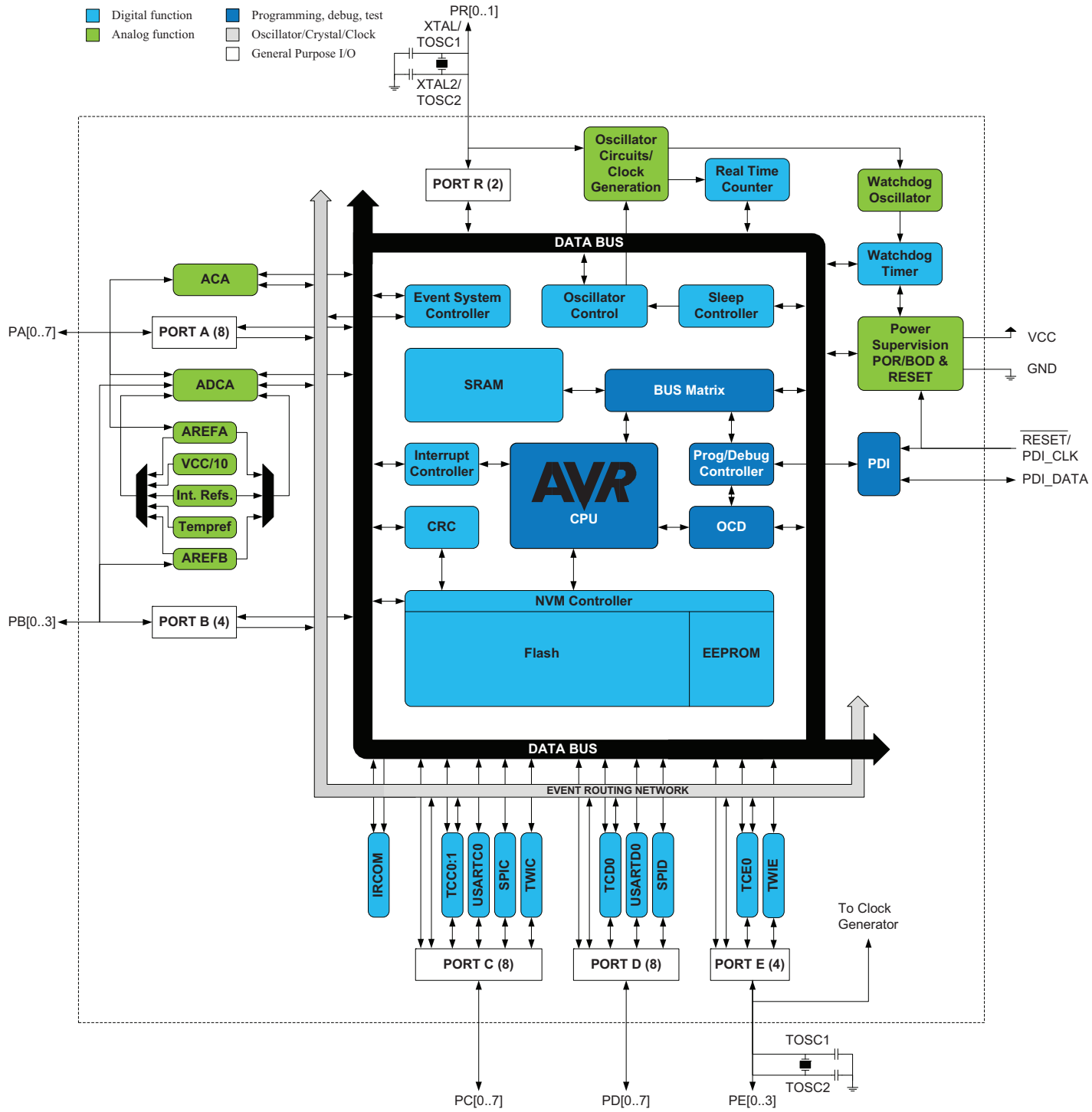
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d4-anr

3.1 Block Diagram

Figure 3-1. XMEGA D4 Block Diagram



6. AVR CPU

6.1 Features

- 8/16-bit, high-performance Atmel AVR RISC CPU
  - 137 instructions
  - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Stack pointer accessible in I/O memory space
- Direct addressing of up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8-, 16-, and 32-bit arithmetic
- Configuration change protection of system-critical features

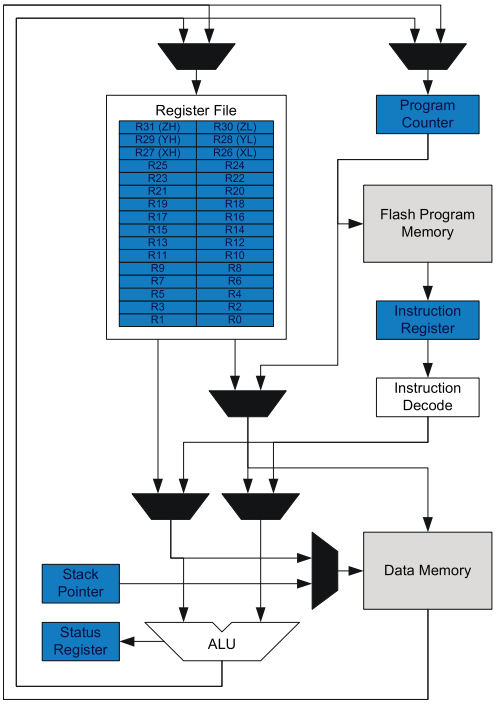
6.2 Overview

All Atmel AVR XMEGA devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program in the flash memory. Interrupt handling is described in a separate section, refer to “Interrupts and Programmable Multilevel Interrupt Controller” on page 27.

6.3 Architectural Overview

In order to maximize performance and parallelism, the AVR CPU uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This enables instructions to be executed on every clock cycle. For details of all AVR instructions, refer to http://www.atmel.com/avr.

Figure 6-1. Block Diagram of the AVR CPU Architecture



1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

9.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

9.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

9.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

9.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

9.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz.

9.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

9.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

22. USART

22.1 Features

- Two identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
  - Synchronous clock rates up to 1/2 of the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits
- Fractional baud rate generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
  - Odd or even parity generation and parity check
  - Data overrun and framing error detection
  - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
  - Transmit complete
  - Transmit data register empty
  - Receive complete
- Multiprocessor communication mode
  - Addressing scheme to address a specific devices on a multidevice bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
  - Double buffered operation
  - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

22.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

PORTC and PORTD each has one USART. Notation of these peripherals are USARTC0 and USARTD0 respectively.

25. ADC – 12-bit Analog to Digital Converter

25.1 Features

- One Analog to Digital Converters (ADC)
- 12-bit resolution
- Up to 200 thousand samples per second
  - Down to 3.6µs conversion time with 8-bit resolution
  - Down to 5.0µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 12 single-ended inputs
  - 12x4 differential inputs without gain
  - 12x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Three internal inputs
  - Internal temperature sensor
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional interrupt/event on compare result

25.2 Overview

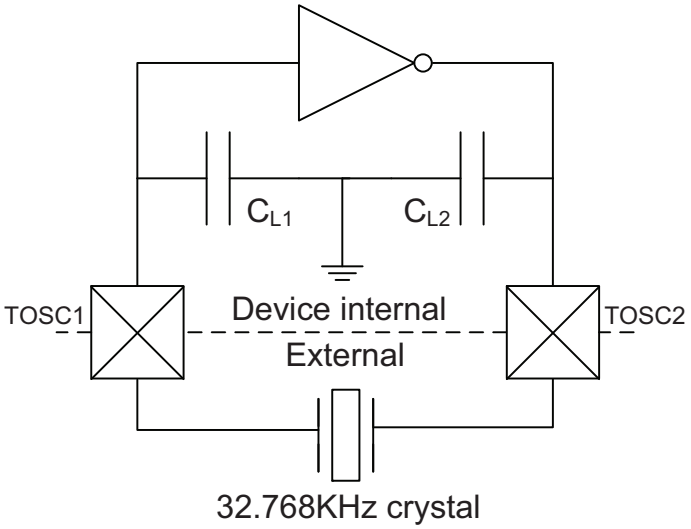
The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to 200 thousand samples per second (ksps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

The ADC measurements can either be started by application software or an incoming event from another peripheral in the device. The ADC measurements can be started with predictable timing, and without software intervention.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The AV_{CC}/10 and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

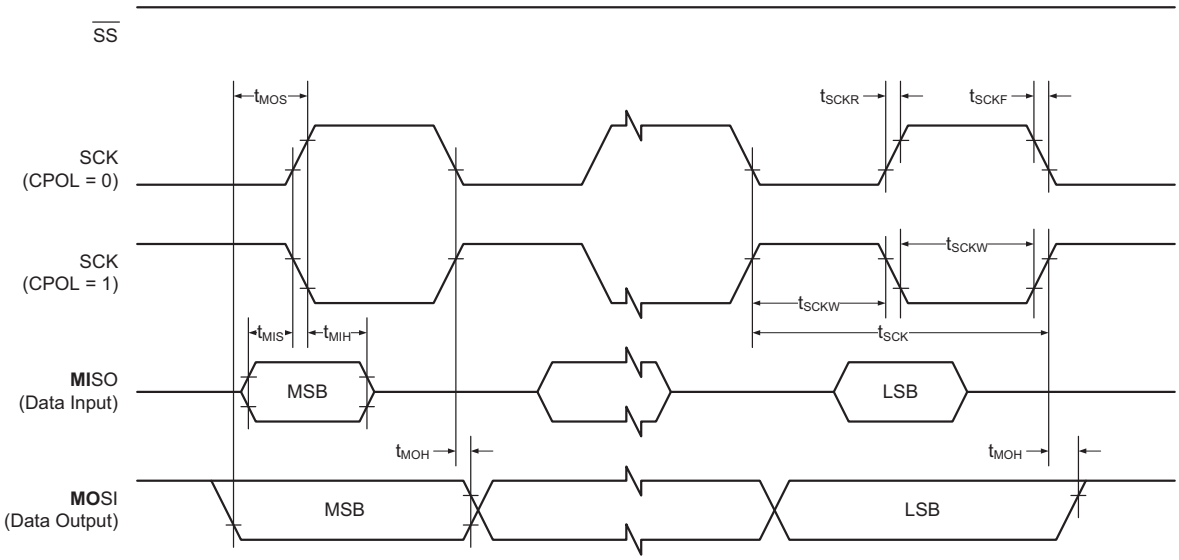
Figure 32-4. TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.1.14 SPI Characteristics

Figure 32-5. SPI Timing Requirements in Master Mode



32.3.3 Current Consumption

Table 32-60. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		68		µA
			V_{CC} = 3.0V		145		
		1MHz, Ext. Clk	V_{CC} = 1.8V		260		
			V_{CC} = 3.0V		540		
		2MHz, Ext. Clk	V_{CC} = 1.8V		460	600	
			V_{CC} = 3.0V		0.96	1.4	mA
		32MHz, Ext. Clk			9.8	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.4		µA
			V_{CC} = 3.0V		3.9		
		1MHz, Ext. Clk	V_{CC} = 1.8V		62		
			V_{CC} = 3.0V		118		
		2MHz, Ext. Clk	V_{CC} = 1.8V		125	225	
			V_{CC} = 3.0V		240	350	
		32MHz, Ext. Clk			3.8	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.2	4.5	
		T = 105°C			0.1	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and sampled BOD enabled, T = 85°C			2.4	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.3	8.0	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3	
			V_{CC} = 3.0V		1.0	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		320		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

32.3.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 32-77. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.22		

32.3.13.4 32kHz Internal ULP Oscillator Characteristics

Table 32-78. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%
	Accuracy		-30		30	

32.3.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 32-79. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency(1)	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.3.14 SPI Characteristics

Figure 32-19.SPI Timing Requirements in Master Mode

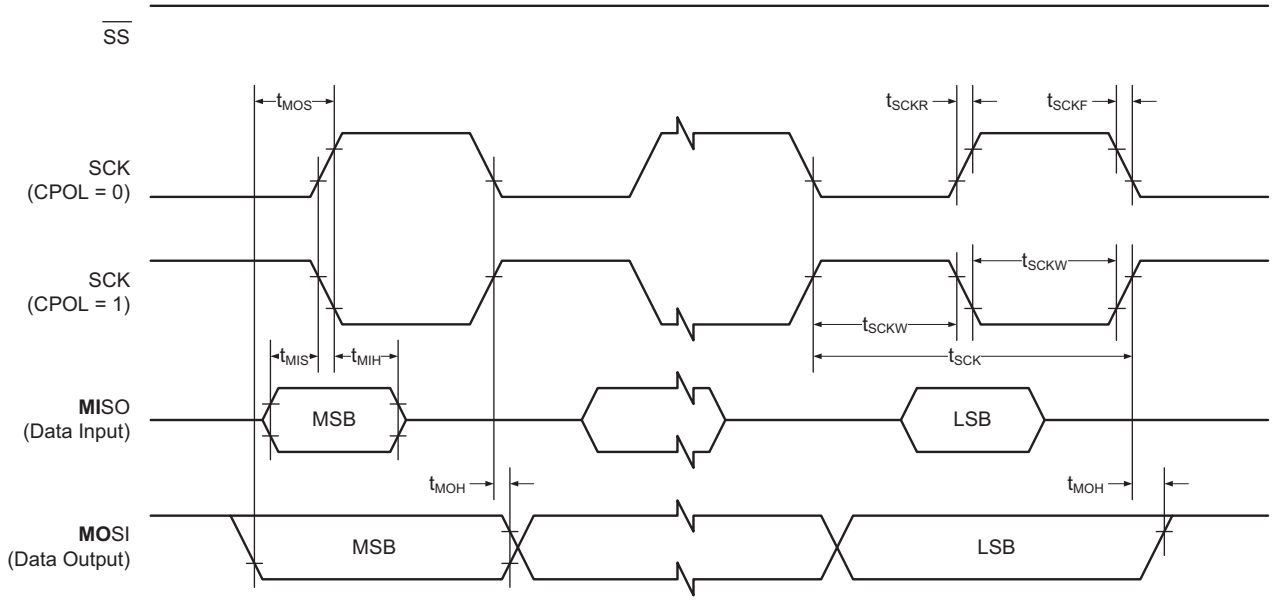


Figure 32-20.SPI Timing Requirements in Slave Mode

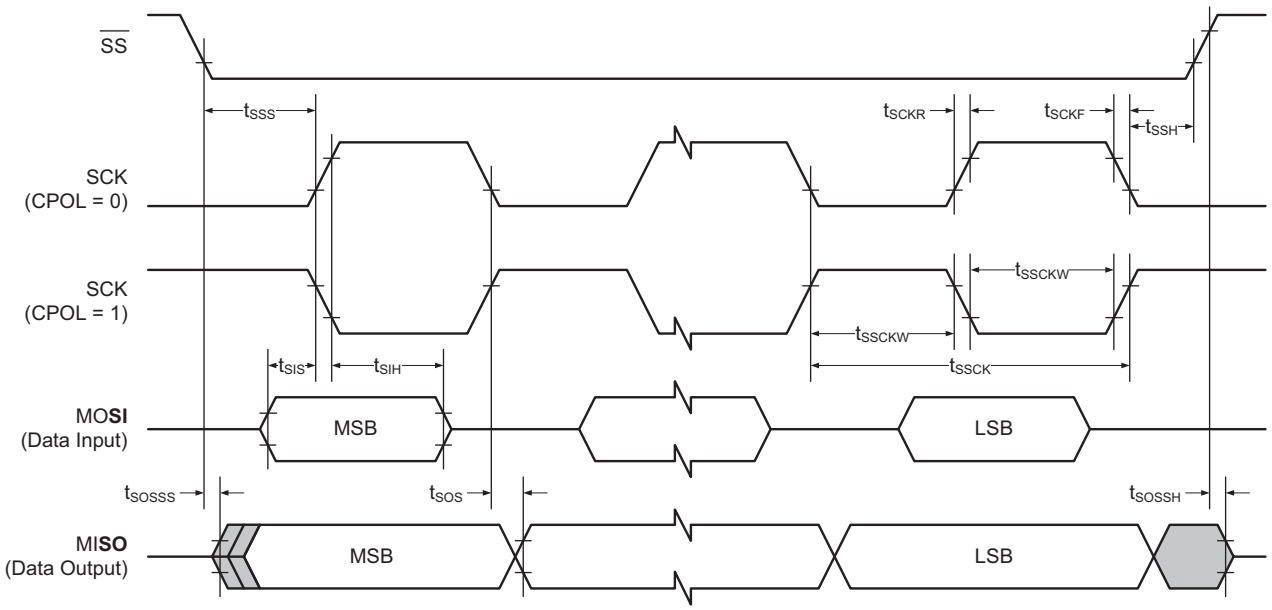


Table 32-90. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				29		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		
		DFLL enabled with 32.768kHz int. osc. as reference			440		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			320		
	Watchdog Timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				260		
	Temperature sensor				250		
	ADC	150ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	AC	High Speed mode			330		µA
		Low power mode			130		
	Timer/Counter				16		
	USART	Rx and Tx enabled, 9600 BAUD			2.5		
	Flash memory and EEPROM programming				4.0	8.0	mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

33.1.1.5 Standby Mode Supply Current

Figure 33-19. Standby Supply Current vs. V_{CC}

Standby, f_{SYS} = 1MHz

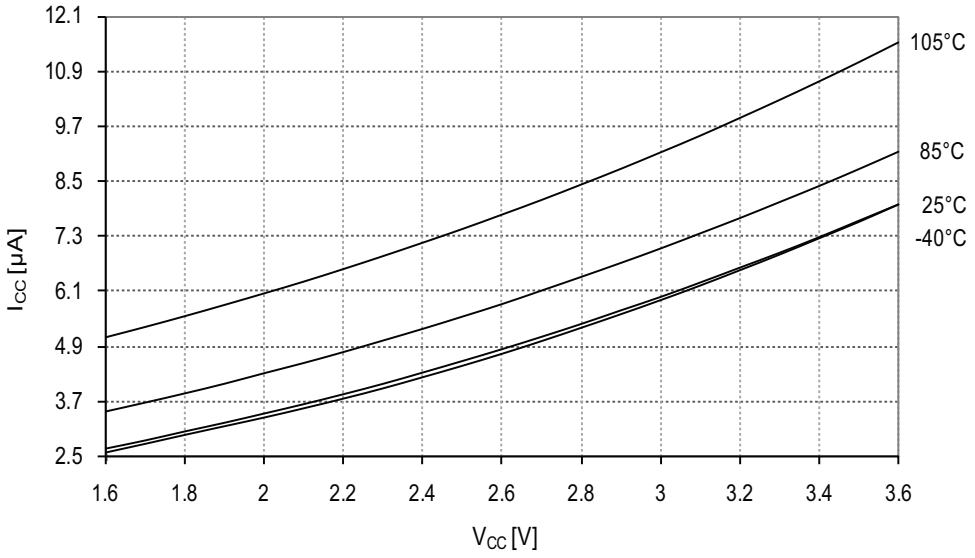
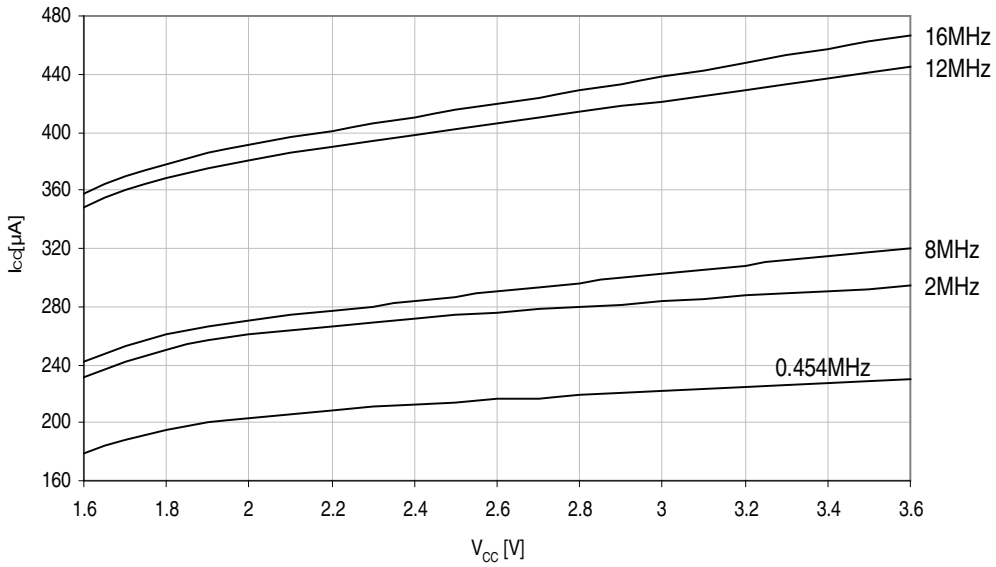


Figure 33-20. Standby Supply Current vs. V_{CC}

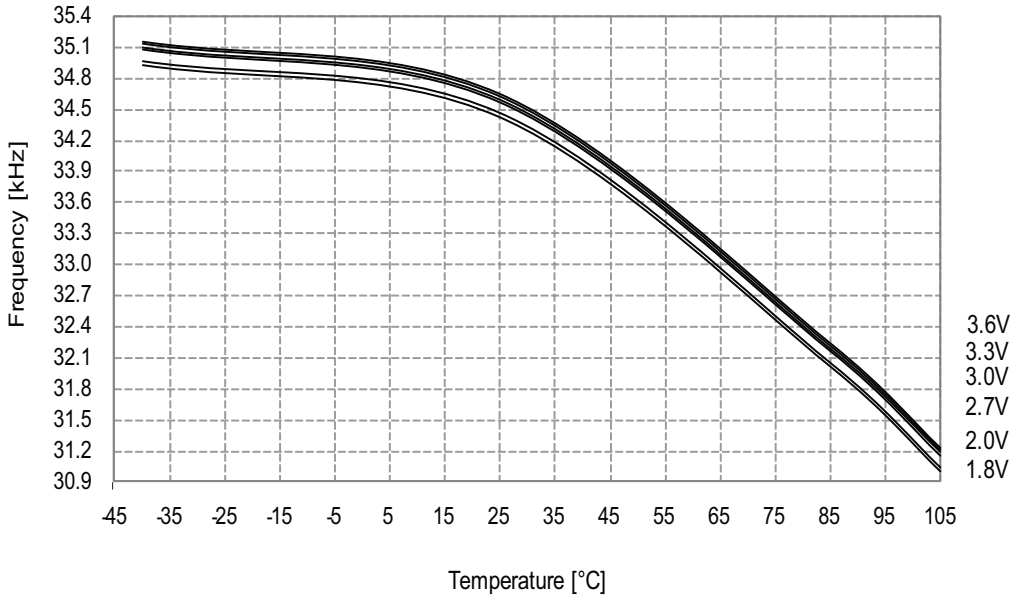
25°C, running from different crystal oscillators



33.1.9 Oscillator Characteristics

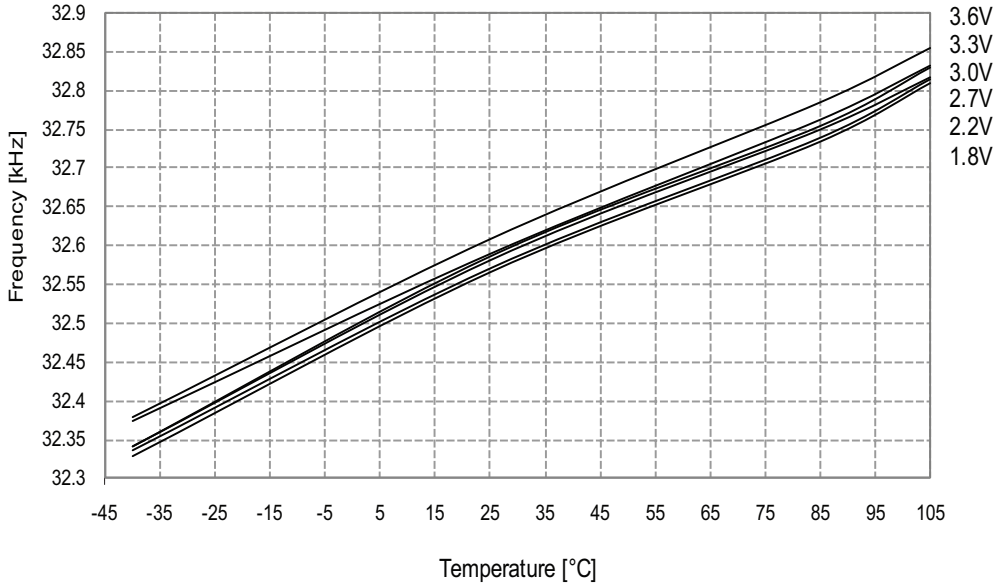
33.1.9.1 Ultra Low-Power Internal Oscillator

Figure 33-65. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



33.1.9.2 32.768kHz Internal Oscillator

Figure 33-66. 32.768kHz Internal Oscillator Frequency vs. Temperature



33.2.4 Analog Comparator Characteristics

Figure 33-126. Analog Comparator Hysteresis vs. V_{CC}

High speed, small hysteresis

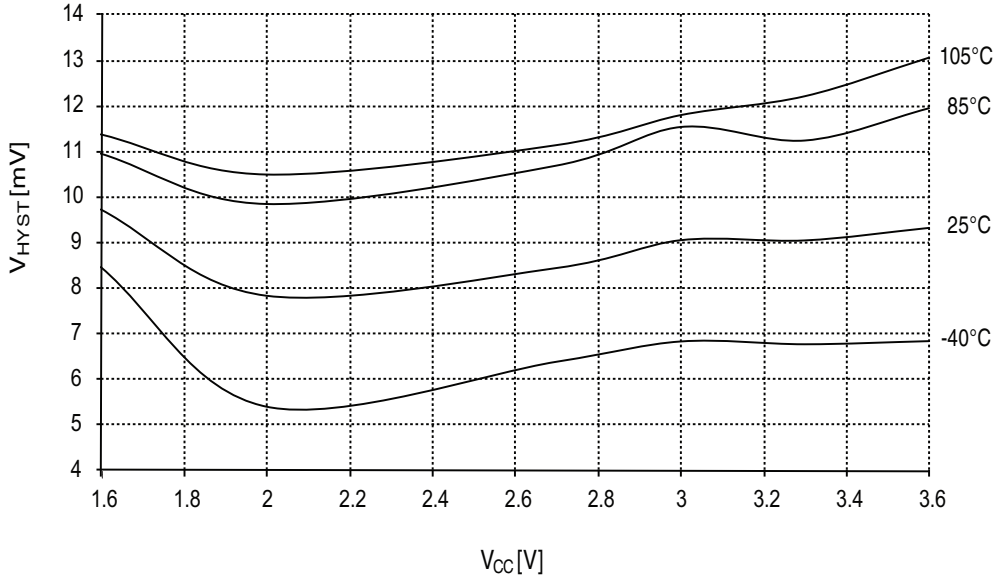


Figure 33-127. Analog Comparator Hysteresis vs. V_{CC}

High speed, large hysteresis

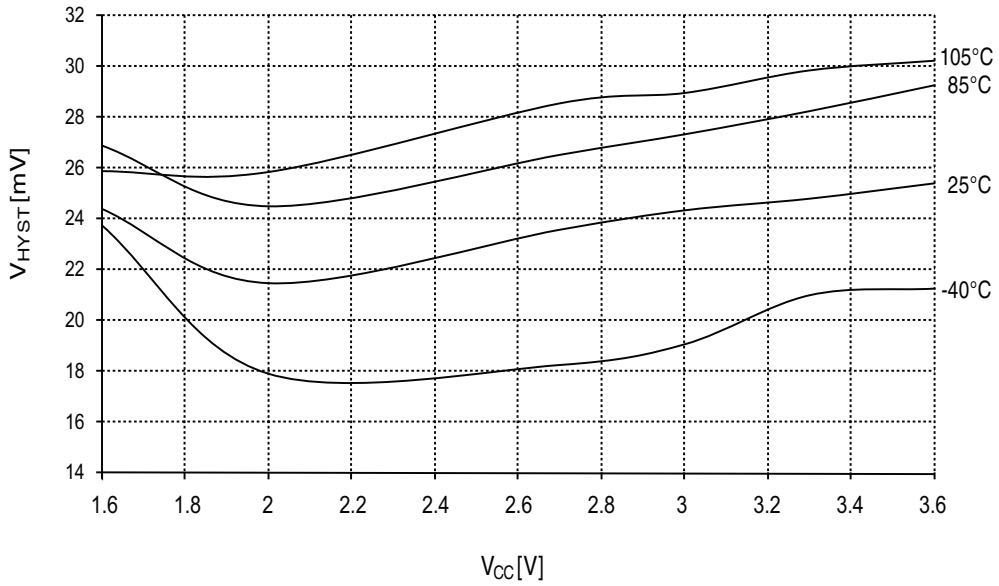


Figure 33-140. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

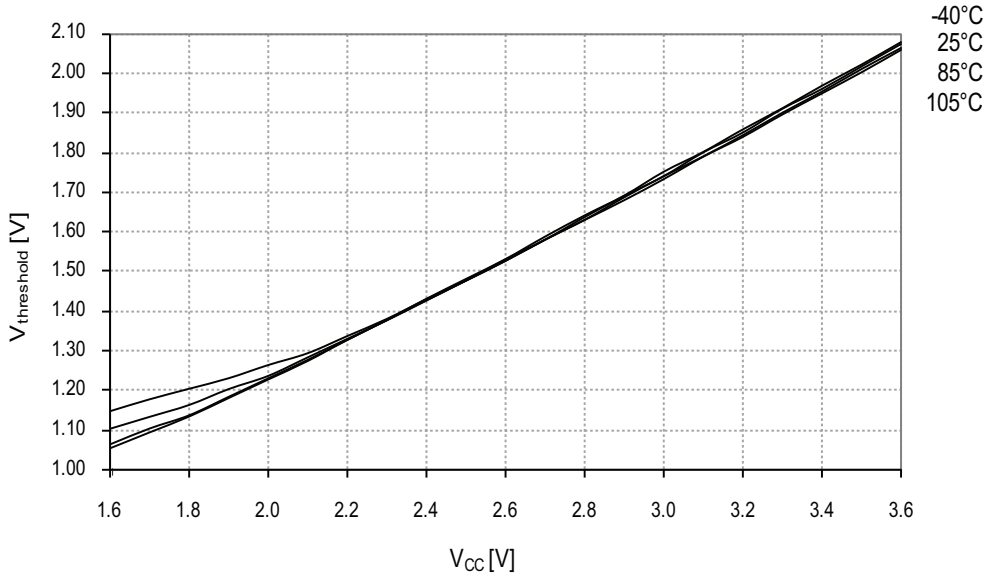


Figure 33-141. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - Reset pin read as "0"

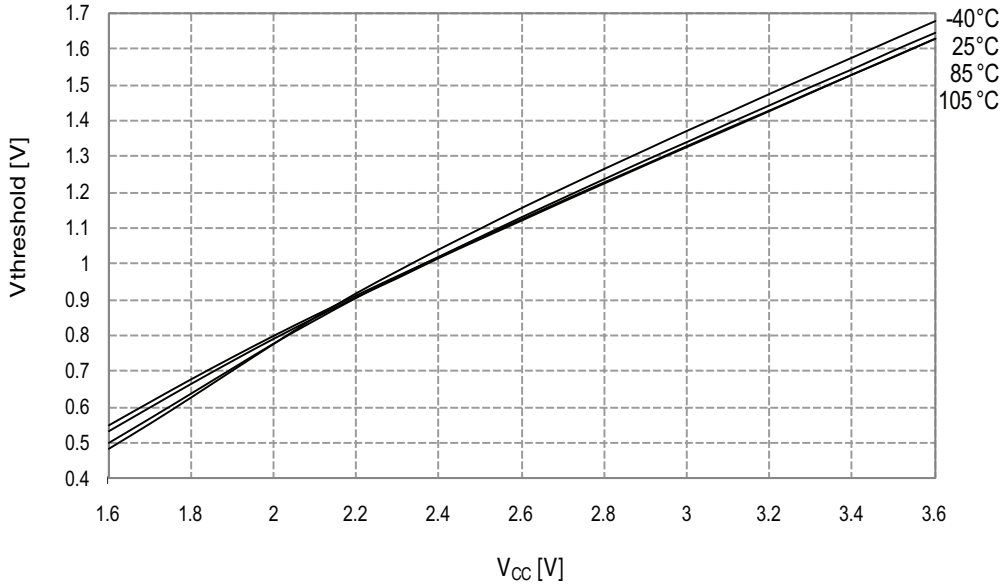
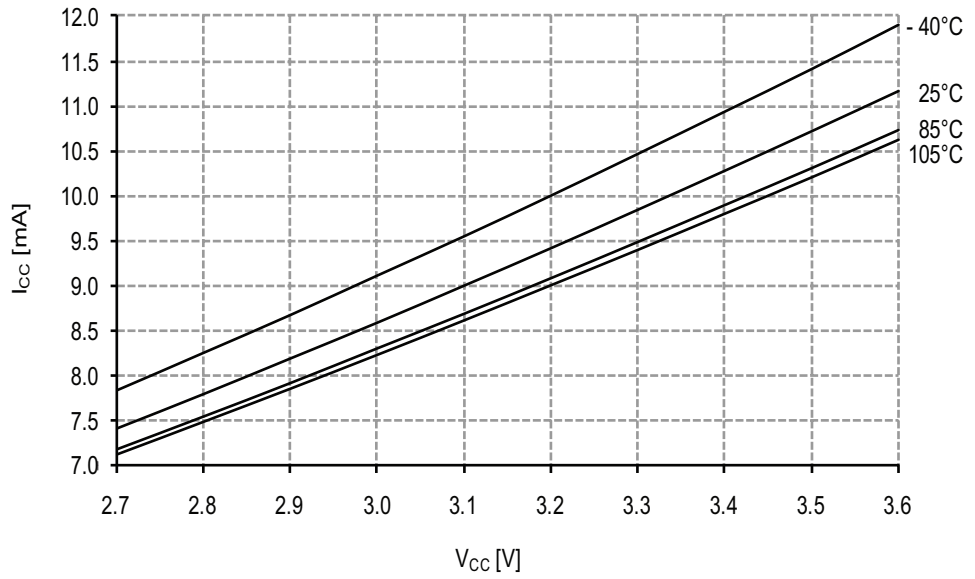


Figure 33-165. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.3.1.2 Idle Mode Supply Current

Figure 33-166. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

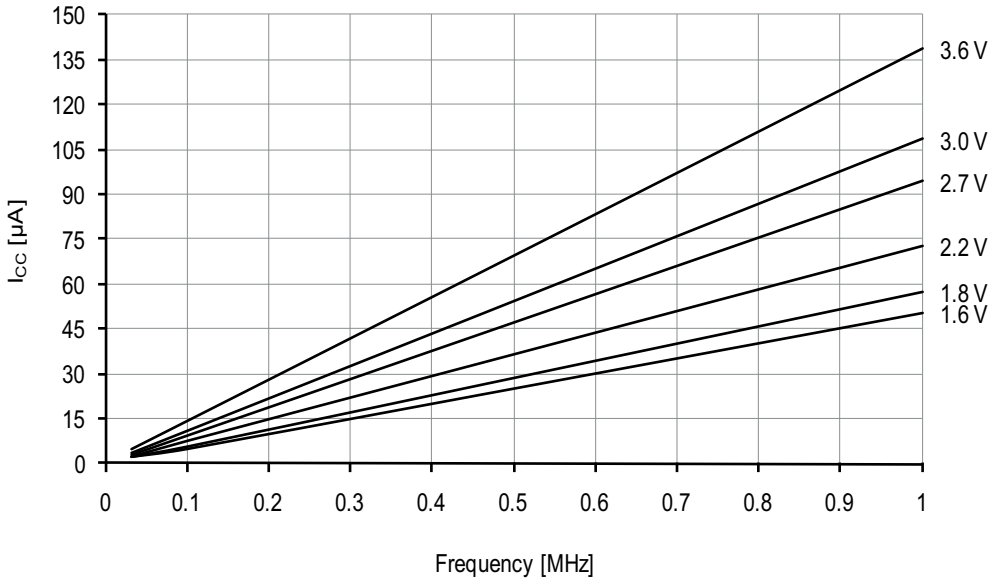


Figure 33-183. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

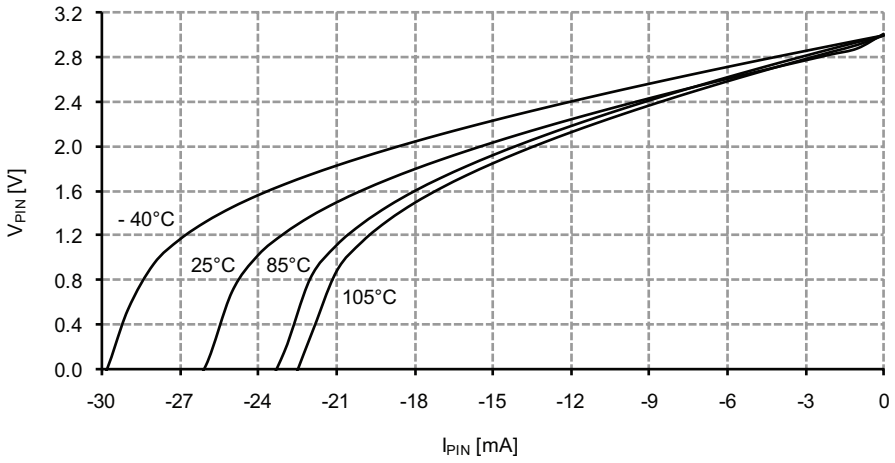


Figure 33-184. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

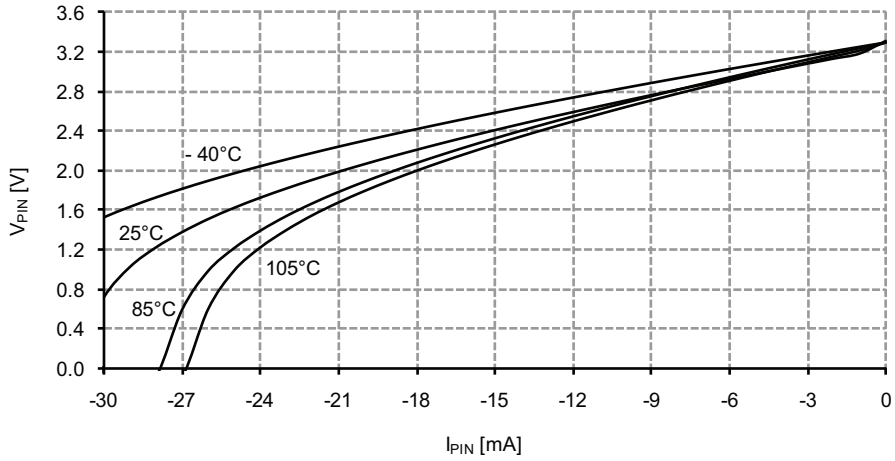


Figure 33-255. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

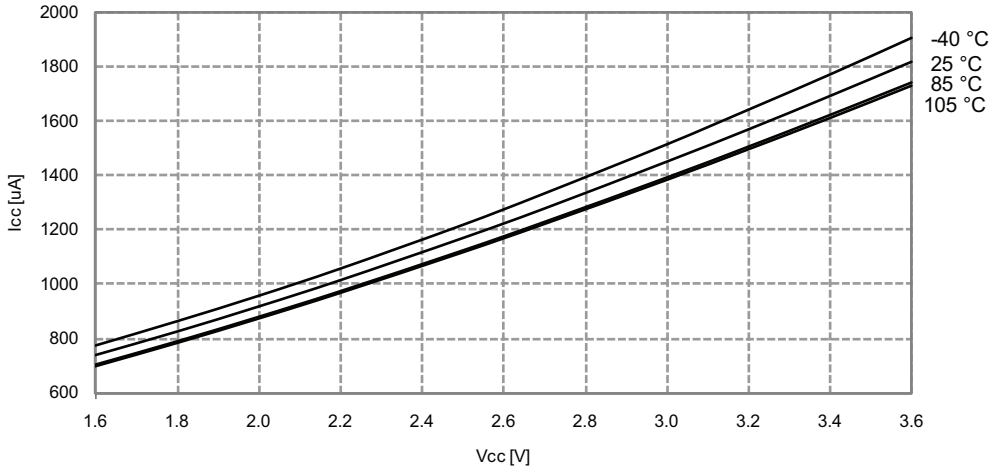


Figure 33-256. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

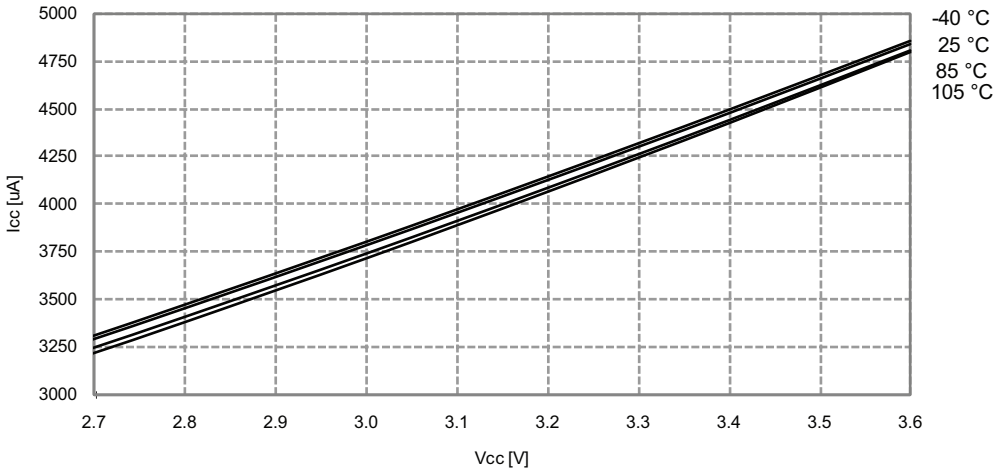


Figure 33-283. DNL Error vs. Input Code

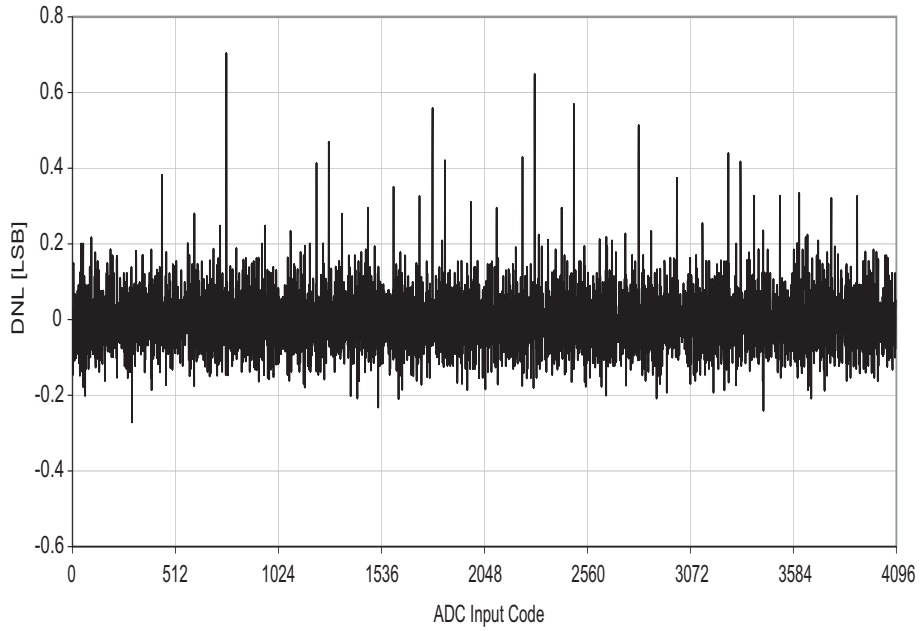
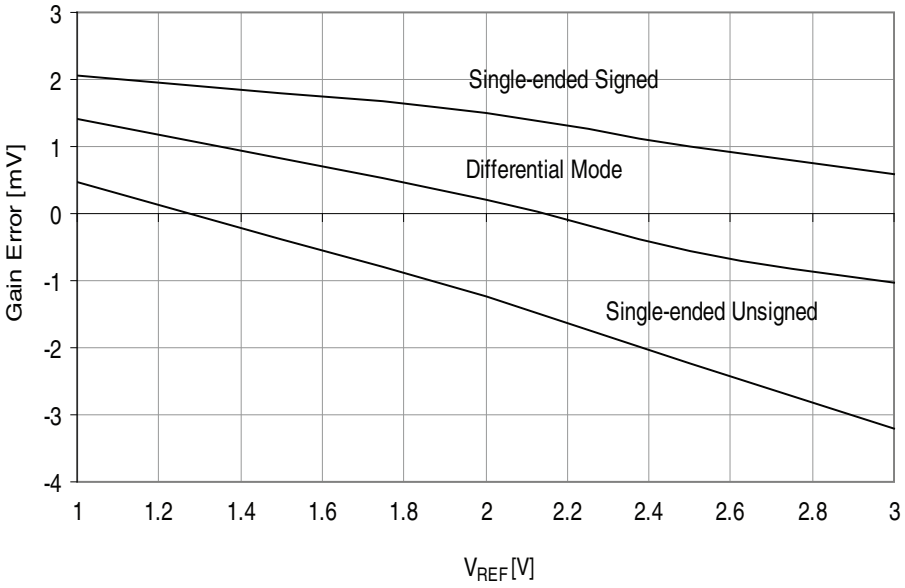


Figure 33-284. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps



34.2 ATxmega64D4

34.2.1 Rev. D

- Temperature sensor not calibrated

1. **Temperature sensor not calibrated**

   Temperature sensor factory calibration not implemented.

   Problem fix/Workaround

   None.

34.2.2 Rev. B/C

Not sampled.

34.2.3 Rev. A

- ADC may have missing codes in SE unsigned mode at low temp and low V_{CC}
- Temperature sensor not calibrated

1. **ADC may have missing codes in SE unsigned mode at low temp and low V_{CC}**

   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   Problem fix/Workaround

   Use the ADC in SE signed mode.

2. **Temperature sensor not calibrated**

   Temperature sensor factory calibration not implemented.

   Problem fix/Workaround

   None.

34.3 ATxmega128D4

34.3.1 Rev. A

- Temperature sensor not calibrated

1. **Temperature sensor not calibrated**

   Temperature sensor factory calibration not implemented.

   Problem fix/Workaround

   None.

Table of Contentsi